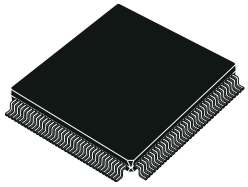
SPC560P50L3, SPC560P50L5
SPC560P44L3, SPC560P44L5

32-bit Power Architecture™ based MCU for chassis & safety applications

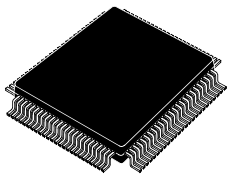
Data Brief

Features

- High performance 60MHz e200z0h CPU
  - 32bit *Power Architecture™ Book E* CPU
  - Variable Length Encoding (VLE)
- Memory Available
  - 512KByte on-chip Flash memory, with ECC, with erase/program controller
  - 4x16KByte on-chip Flash memory with ECC for EEPROM emulation
  - 40KByte on-chip RAM with ECC
- Fail safe protection
  - programmable watchdog timer
  - junction temperature sensor
  - Non maskable interrupt
  - fault collection Unit
- Nexus L2+ interface
- Interrupts
  - 16 channel eDMA controller
  - 16 priority level controller
- Two general purpose eTimer units
  - 6 timers each with up / down capabilities
  - 16bit resolution, cascadeable counters
  - quadrature decode with rotation direction flag
  - double buffer input capture and output compare
- Communications Interfaces
  - Two LINFlex channels
  - Four DSPI channels with automatic chip select generation
  - One FlexCAN interface (2.0B Active) with 32 message objects
  - One safety port based on FlexCAN with 32 message objects and up to 7.5Mbit/s capability; usable as 2nd CAN when not used as safety port
  - FlexRay module (V2.1) with dual or single channel



LQFP-144



LQFP-100

- Two 10-bit A/D Converter
  - 2 x 13 input channels
  - conversion time < 1us including sampling time at full precision
  - programmable ADC Cross Triggering Unit (CTU)
  - 4 analog watchdog with interrupt capability
- On chip CAN/UART/Flexray Bootstrap loader with Boot Assist Module (BAM)
- One FlexPWM Unit
  - 8 complementary or independent outputs with ADC synchronisation signals
  - integrated configurable dead time unit and inverter fault input pins
  - 16bit resolution, up to 2x f_{CPU}
- Clock generation
  - 4-40MHz main oscillator
  - 16MHz internal RC-oscillator
  - software controlled FMPLL
- Voltage supply
  - 3.3V or 5V supply for I/Os and ADC
  - on chip single supply voltage regulator with external ballast transistor
- Temperature Range
  - Operating temperature range -40 to 125°C or -40 to 105°C

Contents

1 Introduction

The 32-bit SPC560Px automotive microcontroller is a System-on-Chip (SoC) device designed to be central to the development of the next wave of airbag/steering applications.

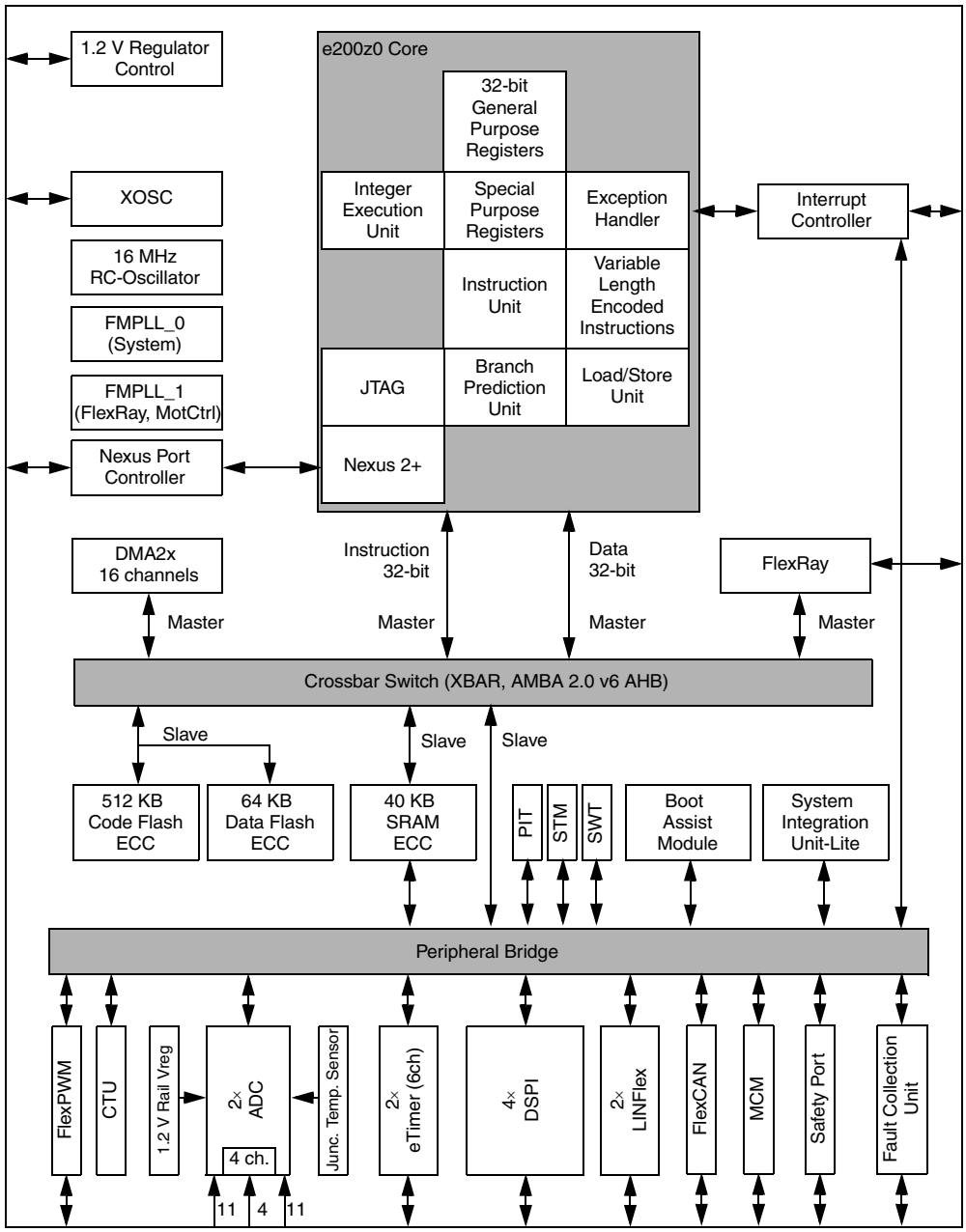
The SPC560Px is one of a series of next-generation automotive microcontrollers based on the Power Architecture™ Book E architecture and designed specifically for embedded applications.

This document describes the features of the SPC560Px and highlights important electrical and physical characteristics of the device.

2 Block diagram

Figure 1 shows a top-level block diagram of the SPC560Px microcontroller.

Figure 1. SPC560Px block diagram



CANController Area Network (FlexCAN)
DSPIDeserial Serial Peripheral Interface
LINFlexSerial Communication Interface (LIN support)
FMPLLFrequency-Modulated Phase-Locked Loop
SRAMStatic Random-Access Memory
FlexPWMFlexible Pulse Width Modulation
eTimerEnhanced Timer
PITPeriodic Interrupt Timer

3 Overview of the SPC560Px

The following sections provide high-level descriptions of the features found on the SPC560Px.

3.1 Device summary

Table 1. SPC560Px device summary

Feature	SPC560P44	SPC560P50
Flash memory size with ECC (KB)	384	576
RAM size with ECC (KB)	32	40
Processor core	32-bit e200z0	
CPU performance	Static – 60 MHz	
Analog-to-digital converters (ADC)	2 (10-bit, 13-channel)	
DSPI (deserial serial peripheral interface) modules	4	
Enhanced DMA (direct memory access) channels	16	
eTimer modules	2 (6 channel)	
FlexCAN (controller area network)	Yes(1)	
FlexPWM (pulse-width modulation) channels	8	
FlexRay	—	Yes(2)
FMPLL (frequency-modulated phase-locked loop) modules	1	2
INTC (interrupt controller) channels	100	144
JTAG interface	Yes	
Junction temperature sensor	Yes	
LINFlex modules	2	
Nexus port controller (NPC)	Yes (Level 2+)	
PIT (periodic interrupt timer)	Yes	
Packages	LQFP100 LQFP144	

1. 32 message buffers
2. 32 message buffers, dual-channel

3.2 Feature list

- Single issue, 32-bit Power Architecture™ CPU core complex (e200z0) with harvard architecture:
  - Provides variable length encoding (VLE) instruction set encoding for code size footprint reduction.
  - With the encoding of mixed 16-bit and 32-bit instructions, it is possible to achieve significant code size footprint reduction over conventional Book E compliant code.
- Up to 512 KB on-chip code flash memory with ECC plus 64 KB on-chip data flash with ECC
- Up to 40 KB SRAM on-chip with ECC
- INTC - Interrupt controller capable of handling 144 selectable-priority interrupt sources
- Up to two FMPLL modules
- Clock Monitor Unit (CMU) to monitor the integrity of the main crystal oscillator and the PLL and act as a frequency meter, measuring the frequency of one clock source and comparing it to a reference clock
- RCOSC - 16 MHz internal RC Oscillator (trimmable)
- PIT - Four Periodic Interrupt Timers with 32-bit counter resolution
- SWT - Windowed software watchodog
- STM - output compare system timer to support AUTOSAR task protection
- XBAR - Crossbar switch architecture for concurrent access to peripherals, flash memory or RAM from multiple bus masters (AMBA 2.0 v6 AHB)
- eDMA - 16 channel Enhanced Direct Memory Access controller with multiple transfer request sources using DMA MUX
- SIU-Lite - System Integration Unit Lite; controls the GPIO mode of the pads, the pads alternate function, and the pads configuration
- BAM - Boot assist module supports downloading operation to internal SRAM via serial link (FlexCAN or LINFlex or FlexRay)
- FlexPWM - Motor Control PWM module (1 x 8PWM channels)
- eTimer - Two enhanced timer modules (6 channels each) with dedicated motor control and quadrature decode features integrated
- Safety Port - To support functional safety architectures on the ECU level. Can be optionally used as a second FlexCAN module with 32 message buffers.
- ADC - Two 10-bit analog-to-digital converters, conversion time <1 µs
- CTU - FlexPWM to ADC and eTimer Cross Triggering Unit
- FCU - Fault Collection Unit for functional safety
- DSPI - Four Serial Peripheral Interface modules
- LINFlex - Two Serial Communication Interface modules with LIN support
- FlexCAN - Controller Area Network module with 32 message buffers
- FlexRay - Dual channel FlexRay Controller with 32 message buffers
- GPIO
  - 144-pin package: 82 general-purpose pins supporting input/output operations plus 26 general-purpose pins supporting input operations (108 in total). Out of these 108 pins, 32 have external interrupt capability.

  - 100-pin package: 51 general-purpose pins supporting input/output operations plus 16 general-purpose pins supporting input operations (67 in total). Out of these 67 pins, 25 have external interrupt capability.
- NDI - Nexus development interface per IEEE-ISTO 5001-2003 standard Class 2+
- IEEE 1149.7 class 4 (narrow pin interface) to allow optimized device I/O count
  - Backward compatible to JTAG (IEEE 1149.1)
- JTAG (IEEE 1149.1) 4 pin interface
- VREG - Voltage regulator for regulation into 3.3V input down to 1.2V nominal core logic level with external transistor
- Embedded junction temperature sensor

3.3 Feature details

3.3.1 High performance e200z0 core processor

The e200z0 Power Architecture™ core provides the following features:

- High performance e200z0 core processor for managing peripherals and interrupts
- Single issue 4-stage pipeline in-order execution 32-bit Power Architecture™ CPU
- Harvard architecture
- Variable length encoding (VLE), allowing mixed 16-bit and 32-bit instructions
  - Results in smaller code size footprint
  - Minimizes impact on performance
- Branch processing acceleration using lookahead instruction buffer
- Load/store unit
  - 1-cycle load latency
  - Misaligned access support
  - No load-to-use pipeline bubbles
- Thirty-two 32-bit general purpose registers (GPRs)
- Separate instruction bus and load/store bus Harvard architecture
- Hardware vectored interrupt support
- Reservation instructions for implementing read-modify-write constructs
- Long cycle time instructions, except for guarded loads, do not increase interrupt latency
- Extensive system development support through Nexus debug port
- Non maskable Interrupt support

3.3.2 Crossbar switch (XBAR)

The XBAR multi-port crossbar switch supports simultaneous connections between 4 master ports and 3 slave ports. The crossbar supports a 32-bit address bus width and a 32-bit data bus width.

The crossbar allows for two concurrent transactions to occur from any master port to any slave port; but one of those transfers must be an instruction fetch from internal flash memory. If a slave port is simultaneously requested by more than one master port, arbitration logic will select the higher priority master and grant it ownership of the slave port. All other masters requesting that slave port will be stalled until the higher priority master

completes its transactions. Requesting masters will be treated with equal priority and will be granted access to a slave port in round-robin fashion, based upon the ID of the last master to be granted access.

The crossbar provides the following features:

- 4 master ports:
  - e200z0 core complex Instruction port
  - e200z0 core complex Load/Store Data port
  - eDMA
  - FlexRay
- 3 slave ports:
  - Flash memory (code flash and data flash)
  - SRAM
  - Peripheral bridge
- 32-bit internal address, 32-bit internal data paths
- Fixed Priority Arbitration based on Port Master
- Temporary dynamic priority elevation of masters

3.3.3 Enhanced Direct Memory Access (eDMA)

The enhanced direct memory access (eDMA) controller is a second-generation module capable of performing complex data movements via 16 programmable channels, with minimal intervention from the host processor. The hardware micro architecture includes a DMA engine which performs source and destination address calculations, and the actual data movement operations, along with an SRAM-based memory containing the transfer control descriptors (TCD) for the channels. This implementation is utilized to minimize the overall block size.

The eDMA module provides the following features:

- 16 channels support independent 8, 16 or 32 bit single value or block transfers
- Supports variable sized queues and circular queues
- Source and destination address registers are independently configured to post-increment or remain constant
- Each transfer is initiated by a peripheral, CPU, or eDMA channel request
- Each eDMA channel can optionally send an interrupt request to the CPU on completion of a single value or block transfer
- DMA transfers possible between system memories, DSPI's, ADC, FlexPWM, eTimer and CTU
- Programmable DMA Channel Mux allows assignment of any DMA source to any available DMA channel with up to a total of 30 potential request sources.
- eDMA abort operation through software

3.3.4 On-chip flash memory with ECC

The SPC560Px provides up to 576 KB of programmable, non-volatile, flash memory. The non-volatile memory (NVM) can be used for instruction and/or data storage. The flash memory module interfaces the system bus to a dedicated flash memory array controller. It supports a 32-bit data bus width at the system bus port, and a 128-bit read data interface to

flash memory. The module contains a four-entry, 4x128-bit prefetch buffers. Prefetch buffer hits allow no-wait responses. Normal flash memory array accesses are registered and are forwarded to the system bus on the following cycle, incurring 3 wait-states.

The flash memory module provides the following features:

- Up to 576 KB flash memory
  - 8 blocks (32KB + 2×16KB + 32KB + 32KB + 3x128KB) Code Flash
  - 4 blocks (16KB + 16KB + 16KB + 16KB) Data Flash
  - Full Read While Write capability between Code and Data Flash
- Four 128-bit wide prefetch buffers to provide single cycle in-line accesses (prefetch buffers can be configured to prefetch code or data or both)
- Typical flash memory access time: 0 wait-state for buffer hits, 3 wait-states for page buffer miss at 60 MHz
- Hardware managed flash memory writes handled by 32-bit RISC Krypton engine
- Hardware and software configurable read and write access protections on a per-master basis.
- Configurable access timing allowing use in a wide range of system frequencies.
- Multiple-mapping support and mapping-based block access timing (0–31 additional cycles) allowing use for emulation of other memory types.
- Software programmable block program/erase restriction control.
- Erase of selected block(s)
- Read page size of 128 bits (4 words)
- 64-bit ECC with single-bit correction, double-bit detection for data integrity
- Embedded hardware program and erase algorithm
- Erase suspend, program suspend and erase-suspended program
- Censorship protection scheme to prevent flash memory content visibility
- Hardware support for EEPROM emulation

3.3.5 On-chip SRAM with ECC

The SPC560Px SRAM module provides a general-purpose memory of up to 40 KB in total.

ECC handling is done on a 32-bit boundary and is completely software compatible with SPC560Px family devices with an e200z6 core and 64-bit wide ECC.

The SRAM module provides the following features:

- Supports read/write accesses mapped to the SRAM memory from any master
- 40 KB general purpose RAM
- Supports byte (8-bit), half word (16-bit), and word (32-bit) writes for optimal use of memory
- Typical SRAM access time: 0 wait-state for reads and 32-bit writes; 1 wait-state for 8- and 16-bit writes if back to back with a read to same memory block

3.3.6 Interrupt Controller (INTC)

The INTC (interrupt controller) provides priority-based preemptive scheduling of interrupt requests, suitable for statically scheduled hard real-time systems.

For high priority interrupt requests, the time from the assertion of the interrupt request from the peripheral to when the processor is executing the interrupt service routine (ISR) has been minimized. The INTC provides a unique vector for each interrupt request source for quick determination of which ISR needs to be executed. It also provides an ample number of priorities so that lower priority ISRs do not delay the execution of higher priority ISRs. To allow the appropriate priorities for each source of interrupt request, the priority of each interrupt request is software configurable.

When multiple tasks share a resource, coherent accesses to that resource need to be supported. The INTC supports the priority ceiling protocol for coherent accesses. By providing a modifiable priority mask, the priority can be raised temporarily so that all tasks which share the resource can not preempt each other.

The INTC provides the following features:

- Unique 9-bit vector for each separate interrupt source
- 8 software triggerable interrupt sources
- 16 priority levels with fixed hardware arbitration within priority levels for each interrupt source
- Ability to modify the ISR or task priority.
  - Modifying the priority can be used to implement the Priority Ceiling Protocol for accessing shared resources.
- Two external high priority interrupts directly accessing the main core and IOP critical interrupt mechanism

3.3.7 System clocks and clock generation

The following list summarizes the system clock and clock generation on the SPC560Px:

- Lock detect circuitry continuously monitors lock status
- Loss of clock (LOC) detection for PLL outputs
- Programmable output clock divider (÷1, ÷2, ÷4, ÷8)
- FlexPWM module and eTimer module can run on an independent clock source
- On-chip oscillator with automatic level control (tbc)
- Internal 16-MHz RC-Oscillator for rapid start-up and safe mode
  - Supports frequency trimming by user application

3.3.8 Frequency modulated PLL (FMPLL)

The FMPLL allows the user to generate high speed system clocks from an 4MHz to 40MHz input clock. Further, the FMPLL supports programmable frequency modulation of the system clock. The PLL multiplication factor, output clock divider ratio are all software configurable.

The PLL has the following major features:

- Input clock frequency from an 4MHz to 40MHz
- Voltage controlled oscillator (VCO) range from 256MHz to 512MHz
- Reduced frequency divider (RFD) for reduced frequency operation without forcing the PLL to relock
- Frequency modulated PLL
  - Modulation enabled/disabled through software

  - Triangle wave modulation
- Programmable modulation depth (±0.25% to ±4% deviation from center frequency)
  - Programmable modulation frequency dependent on reference frequency
- Self-clocked mode (SCM) operation

3.3.9 Main oscillator

The main oscillator provides these features:

- Input frequency range 4 MHz - 40 MHz
- Crystal input mode or Oscillator input mode
- PLL reference

3.3.10 Internal RC-oscillator

This device has an RC ladder phase-shift oscillator. The architecture uses constant current charging of a capacitor. The voltage at the capacitor is compared by the stable bandgap reference voltage.

The RC Oscillator provides these features:

- Nominal frequency 16MHz
- +/-5% variation over voltage and temperature after process trim
- Clock output of the RC oscillator serves as system clock source in case loss of lock or loss of clock is detected by the PLL
- RC-Oscillator is used as the default system clock during startup

3.3.11 Periodic Interrupt Timer Module (PIT)

The PIT module implements these features:

- Up to four general purpose interrupt timers
- 32-bit counter resolution
- Clocked by system clock frequency
- Each channel can be used as trigger for a DMA request

3.3.12 System Timer Module

The STM module implements these features:

- One 32-bit up counter with 8-bit prescaler
- Four 32-bit compare channels
- Independent interrupt source for each channel
- Counter can be stopped in debug mode

3.3.13 Software Watchdog Timer

The SWT has the following features:

  - 32-bit time-out register to set the time-out period
  - Programmable selection of system or oscillator clock for timer operation
  - Programmable selection of window mode or regular servicing
  - Programmable selection of reset or interrupt on an initial time-out

  - Master access protection
  - Hard and soft configuration lock bits
  - Reset configuration inputs allow timer to be enabled out of reset

3.3.14 Fault Collection Unit

The FCU provides an indipendent fault reporting mechanism even in case the CPU is misbehaving.

The FCU module has the following features:

- FCU status register reporting the device status
- Continuous monitoring of critical fault signals
- User selection of critical signals from different fault sources inside the device
- Critical fault events trigger 2 external pins (user selected signal protocol) that can be used externally to reset the device and/or other circuitry (ex: safety relay, Flexray transceiver)
- Faults are latched into a register

3.3.15 System Integration Unit (SIU-Lite)

The SPC560Px SIU-Lite controls MCU pad configuration, external interrupt, general purpose I/O (GPIO), internal peripheral multiplexing.

The pad configuration block controls the static electrical characteristics of I/O pins. The GPIO block provides uniform and discrete input/output control of the I/O pins of the MCU.

The SIU provides the following features:

- Centralized general purpose input output (GPIO) control of up to 82 input/output pins and 26 analog input only pads (package dependent)
- All GPIO pins can be independently configured to support pull-up, pull down, or no pull
- Reading and writing to GPIO supported both as individual pins and 16-bit wide ports
- All peripheral pins, except ADC channels, can be alternatively configured as both general purpose input or output pins
- ADC channels support alternative configuration as general purpose inputs
- Direct readback of the pin value is supported on all pins through the SIU
- Configurable digital input filter that can be applied to some general purpose input pins for noise elimination
  - Up to four internal functions can be multiplexed onto 1 pin

3.3.16 Boot and censorship

Different booting modes are available in the SPC560Px: booting from internal flash memory and booting via a serial link.

The default booting scheme is the one which uses the internal flash memory (an internal pull-down is used to select this mode). The alternate option allows the user to boot via FlexCAN or LINFlex (using the boot assist module software) or via FlexRay.

A censorship scheme is provided to protect the content of the flash memory and offer increased security for the entire device.

A password mechanism is designed to grant the legitimate user access to the non volatile memory.

Boot Assist Module (BAM)

The BAM is a block of read-only one-time programmed memory and is identical for all SPC560Px devices that are based on the e200z0h core. The BAM program is executed every time the device is powered-on if the alternate boot mode has been selected by the user.

The BAM provides the following features:

- Serial bootloading via FlexCAN or LINFlex or FlexRay.
- BAM can accept a password via the used serial communication channel to grant the legitimate user access to the non volatile memory.

3.3.17 Miscellaneous Control Module (MCM)

The MCM on this device features the following:

- Platform configuration & revision
- ECC error reporting for flash memory and SRAM
- ECC error injection for RAM

3.3.18 CAN (FlexCAN)

The SPC560Px MCU contains one controller area network (FlexCAN) module. This module is a communication controller implementing the CAN protocol according to Bosch Specification version 2.0B. The CAN protocol was designed to be used primarily as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness and required bandwidth. FlexCAN module contains 32 message buffers.

The FlexCAN module provides the following features:

- Full implementation of the CAN protocol specification, Version 2.0B
  - Standard data and remote frames
  - Extended data and remote frames
  - Zero to eight bytes data length
  - Programmable bit rate up to 1Mbit/s
- 32 message buffers of zero to eight bytes data length
- Each message buffer configurable as Rx or Tx, all supporting standard and extended messages
- Programmable loop-back mode supporting self-test operation
- Three programmable mask registers
- Programmable transmit-first scheme: lowest ID or lowest buffer number
- Time stamp based on 16-bit free-running timer
- Global network time, synchronized by a specific message
- Maskable interrupts
- Independent of the transmission medium (an external transceiver is assumed)
- High immunity to EMI
- Short latency time due to an arbitration scheme for high-priority messages

- Transmit features
  - Supports configuration of multiple mailboxes to form message queues of scalable depth
  - Arbitration scheme according to message ID or message buffer number
  - Internal arbitration to guarantee no inner or outer priority inversion
  - Transmit abort procedure and notification
- Receive features
  - Individual programmable filters for each mailbox
  - Eight mailboxes configurable as a six-entry receive FIFO
  - Eight programmable acceptance filters for receive FIFO
- Programmable clock source
  - system clock
  - Direct oscillator clock to avoid PLL jitter

3.3.19 Safety port (FlexCAN)

The SPC560Px MCU has a second CAN controller synthesized to run at high bit rates to be used as a safety port. The CAN module of the safety port provides the following features:

- Identical to the FlexCAN module
- Bit rate up to 7.5 Mb at 60 MHz CPU clock using direct connection between CAN modules (no physical transceiver required)
- 32 Message Buffers of zero to eight bytes data length
- Can be used as a second independent CAN module

3.3.20 FlexRay

The FlexRay module provides the following features:

- Full implementation of FlexRay Protocol Specification 2.1
- 32 configurable message buffers can be handled
- Dual channel or single channel mode of operation, each at up to 10Mbit/s data rate
- Message buffers configurable as Tx, Rx or RxFIFO
- Message buffer size configurable
- Message filtering for all message buffers based on FrameID, cycle count and message ID
- Programmable acceptance filters for RxFIFO message buffers

3.3.21 Serial communication interface module (LINFlex)

The LINFlex on the SPC560Px features the following:

- Supports LIN Master mode, LIN Slave mode and UART mode
- LIN state machine compliant to LIN1.3, 2.0 and 2.1 Specifications
- Handles LIN frame transmission and reception without CPU intervention
- LIN features
  - Autonomous LIN frame handling
  - Message buffer to store Identifier and up to eight data bytes

  - Supports message length of up to 64 bytes
  - Detection and flagging of LIN errors: Sync field; Delimiter; ID parity; Bit, Framing; Checksum and Time-out errors
  - Classic or extended checksum calculation
  - Configurable Break duration of up to 36-bit times
  - Programmable Baud rate prescalers (13-bit mantissa, 4-bit fractional)
  - Diagnostic features: Loop back; Self Test; LIN bus stuck dominant detection
  - Interrupt-driven operation with 16 interrupt sources
- LIN slave mode features
  - Autonomous LIN header handling
  - Autonomous LIN response handling
- UART mode
  - Full-duplex operation
  - Standard non return-to-zero (NRZ) mark/space format
  - Data buffers with 4-byte receive, 4-byte transmit
  - Configurable word length (8-bit or 9-bit words)
  - Error detection and flagging
  - Parity, Noise and Framing errors
  - Interrupt-driven operation with four interrupt sources
  - Separate transmitter and receiver CPU interrupt sources
  - 16-bit programmable baud-rate modulus counter and 16-bit fractional
  - Two receiver wake-up methods

3.3.22 Deserial serial peripheral interface (DSPI) module

The deserial serial peripheral interface (DSPI) module provides a synchronous serial interface for communication between the SPC560Px MCU and external devices.

The DSPI modules provide these features:

- Full duplex, synchronous transfers
- Master or slave operation
- Programmable master bit rates
- Programmable clock polarity and phase
- End-of-transmission interrupt flag
- Programmable transfer baud rate
- Programmable data frames from 4 to 16 bits
- Up to 4 chip select lines available, depending on package and pin multiplexing, enable 12 external devices to be selected using external muxing from a single DSPI
- 8 clock and transfer attributes registers
- Chip select strobe available as alternate function on one of the chip select pins for de-glitching
- FIFOs for buffering up to 4 transfers on the transmit and receive side
- Queueing operation possible through use of the I/O processor or eDMA
- General purpose I/O functionality on pins when not used for SPI

3.3.23 FlexPWM

The pulse width modulator module (PWM) contains four PWM submodules each of which is set up to control a single half-bridge power stage. There are also four fault channels.

This PWM is capable of controlling most motor types: AC induction motors (ACIM), Permanent Magnet AC motors (PMAC), both brushless (BLDC) and brush DC motors (BDC), switched (SRM) and variable reluctance motors (VRM), and stepper motors.

The FlexPWM block implements the following features:

- 16 bits of resolution for center, edge aligned, and asymmetrical PWMs
- PWM outputs can operate as complimentary pairs or independent channels
- Can accept signed numbers for PWM generation
- Independent control of both edges of each PWM output
- Synchronization to external hardware or other PWM supported
- Double buffered PWM registers
  - Integral reload rates from 1 to 16
  - Half cycle reload capability
- Multiple ADC trigger events can be generated per PWM cycle via hardware
- Write protection for critical registers
- Fault inputs can be assigned to control multiple PWM outputs
- Programmable filters for fault inputs
- Independently programmable PWM output polarity
- Independent top and bottom deadtime insertion
- Each complementary pair can operate with its own PWM frequency and deadtime values
- Individual software-control for each PWM output
- All outputs can be programmed to change simultaneously via a "Force Out" event
- PWMX pin can optionally output a third PWM signal from each submodule
- Channels not used for PWM generation can be used for buffered output compare functions
- Channels not used for PWM generation can be used for input capture functions
- Enhanced dual edge capture functionality
- eDMA support with automatic reload

3.3.24 eTimer

Six 16-bit general purpose up/down timer/counter per module are implemented with the following features:

- Individual channel capability
  - Input capture trigger
  - Output compare
  - Double buffer (to capture rising edge and falling edge)
  - Separate prescaler for each counter
  - Selectable clock source
  - 0% - 100% pulse measurement

  - Rotation direction flag (Quad decoder mode)
- Maximum count rate
- Counters are cascadeable
- Programmable count modulo
- Quadrature decode capabilities
- Counters can share available input pins
- Count once or repeatedly
- Counters are pre-loadable
- Pins available as GPIO when timer functionality not in use

3.3.25 Analog to digital converter module

The ADC module provides the following features:

Analog part:

- Two on-chip AD converters
  - 10 Bit AD resolution
  - one sample and hold unit per ADC
  - Conversion time, including sampling time, less than 1 µs (at full precision)
  - Typical sampling time is 150 ns min. (at full precision)
  - DNL/INL ±1LSB
  - TUE <1.5LSB
  - Single-ended input signal range from 0 to 3.3V -
  - The ADC and its reference can be supplied with a voltage independent from V_{DDIO}
  - The ADC supply can be equal or higher than V_{DDIO}
  - The ADC supply and the ADC reference are not independent from each other (they are internally bonded to the same pad)
  - Sample times of 2 (default), 8, 64 or 128 ADC clock cycles

Digital part:

- 2x13 input channels
  - the total 26 channels includes 4 channels shared among the two converters
- Four analog watchdogs comparing ADC results against predefined levels (low, high, range) before results are stored in the appropriate ADC result location,
- 2 modes of operation: Motor Control Mode or Regular Mode
- Regular mode features
  - register based interface with the CPU: control reg., status reg., 1 result register per channel
  - ADC state machine managing 3 request flows: regular command, hardware injected command, software injected command
  - selectable priority between software and hardware injected commands
  - 4 analog watchdogs comparing ADC results against predefined levels (low, high, range)
  - DMA compatible interface
- Motor control mode features

- Triggered mode only
- Four independent result queues (1x16 entries, 2x8 entries, 1x4 entries)
- Result alignment circuitry (left justified; right justified)
- 32-bit read mode allows to have channel ID on one of the 16-bit part
- DMA compatible interfaces

3.3.26 Cross Triggering Unit (CTU)

The Cross Triggering Unit (CTU) allows automatic generation of ADC conversion requests on user selected conditions without CPU load during the PWM period and with minimized CPU load for dynamic configuration.

It implements the following features:

- Double buffered trigger generation unit with up to eight independent triggers generated from external triggers
- Trigger generation unit configurable in sequential mode or in triggered mode
- Each Trigger can be appropriately delayed to compensate the delay of external low pass filter
- Double buffered global trigger unit allowing eTimer synchronization and/or ADC command generation
- Double buffered ADC command list pointers to minimize ADC-trigger unit update
- Double buffered ADC conversion command list with up to 24 ADC commands
- Each trigger has the capability to generate consecutive commands
- ADC conversion command allows to control ADC channel from each ADC, single or synchronous sampling, independent result queue selection

3.3.27 Junction temperature sensor

The SPC560Px has a junction temperature sensor to allow to measure, by the ADC, the temperature of the silicon.

These are the key parameters of the junction temperature sensor:

- Nominal temperature range from -40°C to +150°C
- Accuracy of the sensor +/- 5°C (tbc)

3.3.28 Nexus Development Interface (NDI)

The NDI (Nexus Debug Interface) block provides real-time development support capabilities for the SPC560Px Power Architecture based MCU in compliance with the IEEE-ISTO 5001-2003 standard. This development support is supplied for MCUs without requiring external address and data pins for internal visibility. The NDI block is an integration of several individual Nexus blocks that are selected to provide the development support interface for this device. The NDI block interfaces to the host processor and internal busses to provide development support as per the IEEE-ISTO 5001-2003 Class 2+ standard. The development support provided includes access to the MCUs internal memory map and access to the processors internal registers during run time.

The Nexus Interface provides the following features:

- Configured via the IEEE 1149.1
- All Nexus port pins operate at V_{DDIO} (no dedicated power supply)

- Nexus 2+ features supported
  - Static debug
  - Watchpoint messaging
  - Ownership trace messaging
  - Program trace messaging
  - Real time read/write of any internally memory mapped resources through JTAG pins
  - Overrun control, which selects whether to stall before Nexus overruns or keep executing and allow overwrite of information
  - Watchpoint triggering, watchpoint triggers program tracing
- Auxiliary Output Port
  - 4 MDO (Message Data Out) pins
  - 1 MCKO (Message Clock Out) pin
  - 2 $\overline{\text{MSEO}}$ (Message Start/End Out) pins
  - 1 $\overline{\text{EVTO}}$ (Event Out) pin
- Auxiliary Input Port
  - 1 $\overline{\text{EVTI}}$ (Event In) pin

3.3.29 IEEE 1149.1 JTAG controller

The JTAG controller (JTAGC) block provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode. All data input to and output from the JTAGC block is communicated in serial format. The JTAGC block is compliant with the IEEE standard.

The JTAG controller provides the following features:

- IEEE Test Access Port (TAP) interface 4 pins (TDI, TMS, TCK, TDO)
- Selectable modes of operation include JTAGC/debug or normal system operation.
- A 5-bit instruction register that supports the following IEEE 1149.1-2001 defined instructions:
  - BYPASS, IDCODE, EXTEST, SAMPLE, SAMPLE/PRELOAD
- A 5-bit instruction register that supports the additional following public instructions:
  - ACCESS_AUX_TAP_NPC, ACCESS_AUX_TAP_ONCE
- Three test data registers: a bypass register, a boundary scan register, and a device identification register. The size of the boundary scan register is parameterized to support a variety of boundary scan chain lengths.
- A TAP controller state machine that controls the operation of the data registers, instruction register and associated circuitry.

3.3.30 On-chip Voltage Regulator (VREG)

The on-chip voltage regulator module provides the following features:

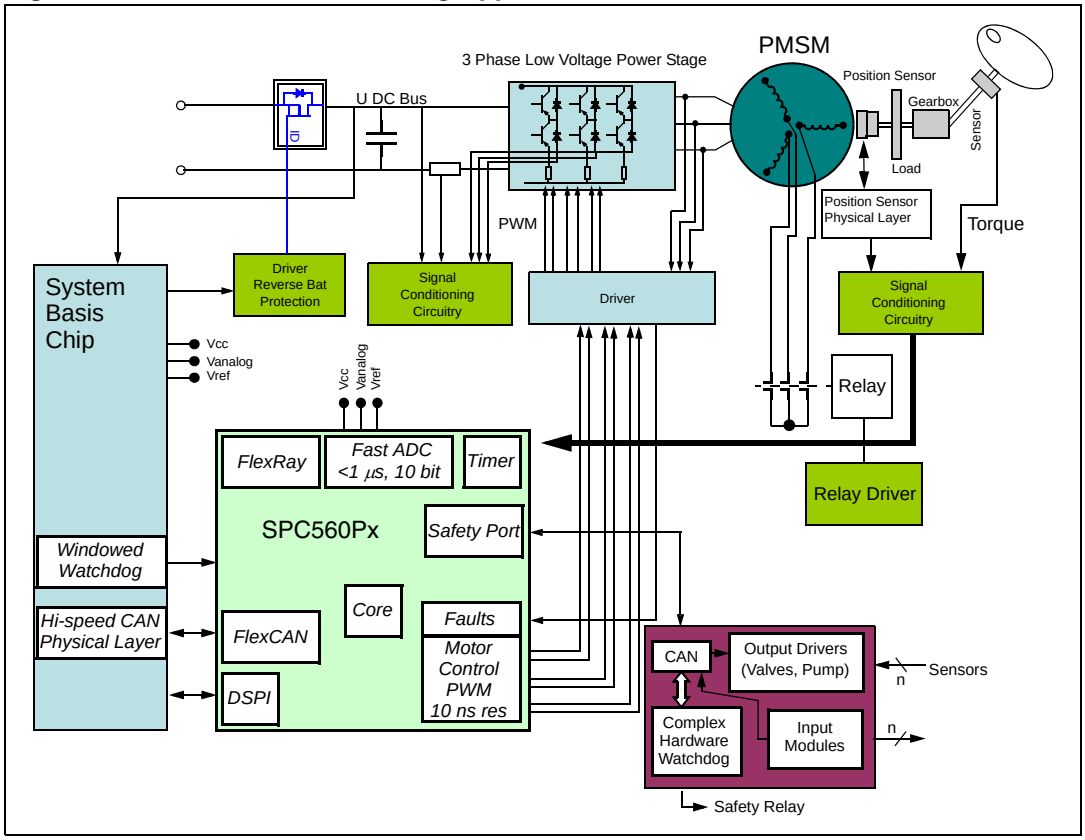
- Uses external NPN transistor
- Regulates external 3.3V down to 1.2V for the core logic
- Low voltage detection on the internal 1.2V and I/O voltage 3.3V

4 Application Examples

4.1 Electric power steering

Figure 2 outlines a typical electric power steering application built around the SPC560Px microcontroller.

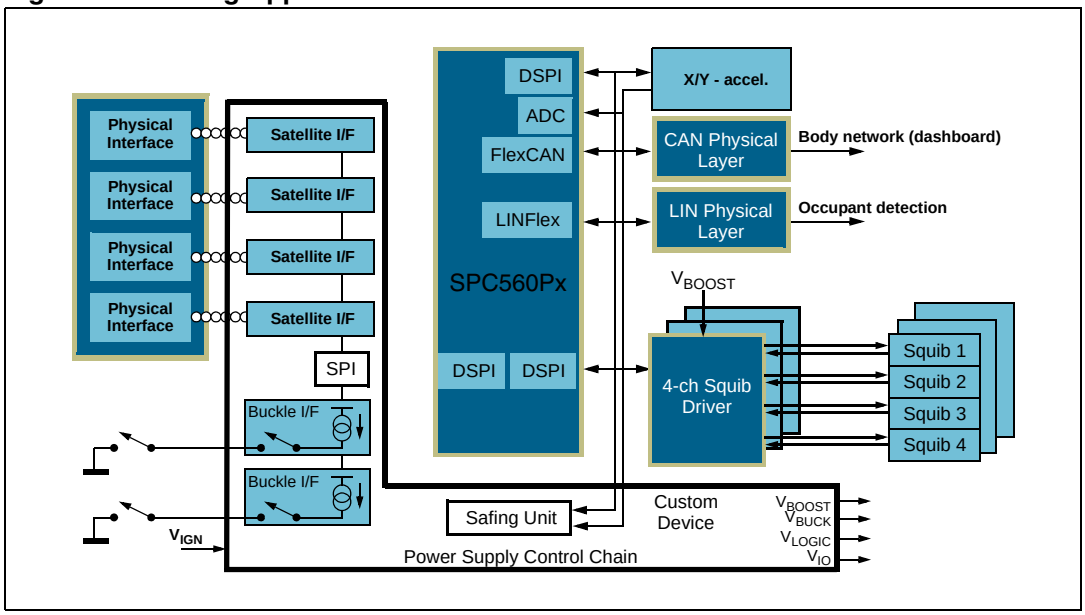
Figure 2. Electric Power Steering Application



4.2 Airbag

Figure 3 outlines a typical airbag application built around the SPC560Px microcontroller.

Figure 3. Airbag Application



5 Developer environment

The following development support will be available:

- Automotive Evaluation Boards (EVB) featuring CAN, LIN interfaces and more
- Compilers
- Debuggers
- JTAG and Nexus interfaces
- Autocode generation tools
- Initialization tools

The following software support will be available:

- Core and peripheral self tests

Note: 1 LBGA208 available only as development package for Nexus2+

6 Ordering information

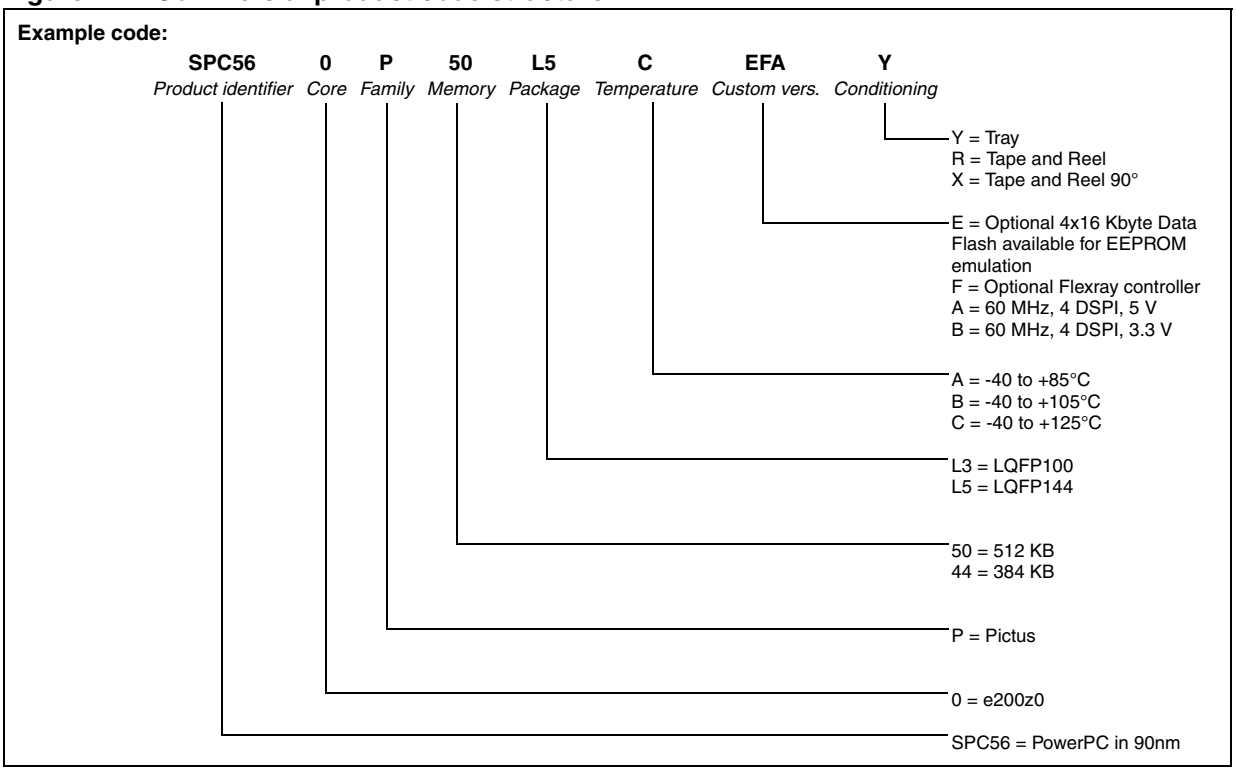
In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at *http://www.st.com*.

Table 2. Order codes(1)

Order Code	Flash (KB)	SRAM (KB)	Package	Characteristics
SPC560P50L5CEFA	576	40	LQFP144	Data flash; FlexRay; 5 V
SPC560P50L5CEFB	576	40	LQFP144	Data flash; FlexRay; 3.3 V
SPC560P50L3CEFA	576	40	LQFP100	Data flash; FlexRay; 5 V
SPC560P50L3CEFB	576	40	LQFP100	Data flash; FlexRay; 3.3 V
SPC560P44L5CEFA	384	32	LQFP144	Data flash; FlexRay; 5 V
SPC560P44L5CEFB	384	32	LQFP144	Data flash; FlexRay; 3.3 V
SPC560P44L3CEFA	384	32	LQFP100	Data flash; FlexRay; 5 V
SPC560P44L3CEFB	384	32	LQFP100	Data flash; FlexRay; 3.3 V

1. All parts support a maximum speed of 60 MHz and a temperature range of -40 °C to +125 °C.

Figure 4. Commercial product code structure



7 Document revision history

Table 3. Revision history

Date	Revision	Changes
12-Nov-2007	1	Initial release
16-May-2008	2	Added 64-pin in pin muxing, pin mapping and mechanical data
13-Jun-2008	3	Removed 64-pin, changed the contents and added new RPNs.

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