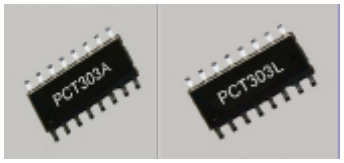
PCT2303N for AMR & MDC

The Leader in Host Signal Processing (HSP) Modem Technology



Codec/DAA Features

- AC'97 Rev 2.1 compliant
- 86dB dynamic range TX/RX paths
- 2-4-wire hybrid
- Integrated ring detector
- High voltage isolation of 2000V
- Support for "Caller ID"
- Compliant with FCC Part15B/Part 68
- Low power standby
- Low profile SOIC package 10x3x1.55mm
- Low power consumption
  10mA @ 3.3V operation
  1mA @ 3.3V power down
- Integrated modem codec

Standard Features

Data

- ITU-T V.90, V.34, V.32bis, V.32, V.22bis, V.22, V.21, V.23, Bell 212A, Bell 103
- Data Compression
  ITU-T V.42bis
  MNP Class 5
- Error Correction
  ITU-T V.42 LAPM
  MNP 2-4

Fax

- ITU-T V. 17, V.29, V.27ter, V.21
  Channel 2
  Group 3
  EIA Class I

Operating Systems

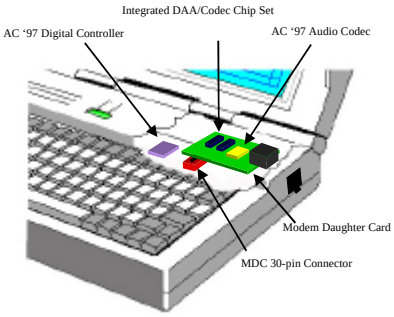
- Windows 95/98, NT 4.0, Windows 2000, and Linux

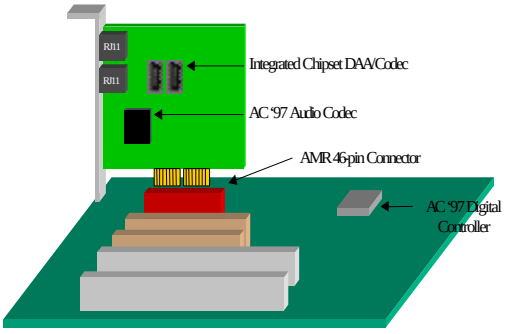
Motherboard integration of the modem subsystem has been problematic to date, in large part due to FCC and other international telecom certification processes that delay the introduction of a motherboard when the modem's analog I/O (codec and DAA) circuitry was physically soldered to the board. Resolving homologation/ certification issues for OEMs is one of the key objectives of the AMR/MDC specification.

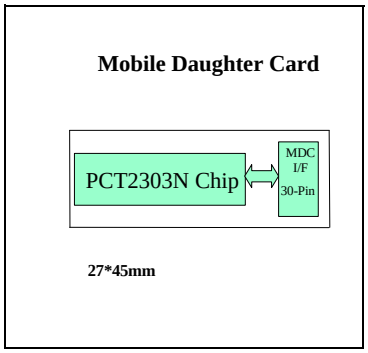
With an open, Industry-standard riser solution, a system manufacturer is free to implement audio and/or modem functions on the motherboard at a lower bill of materials (BOM) cost than would be possible by deploying these functions in either industry-standard expansion slots or in a proprietary method.

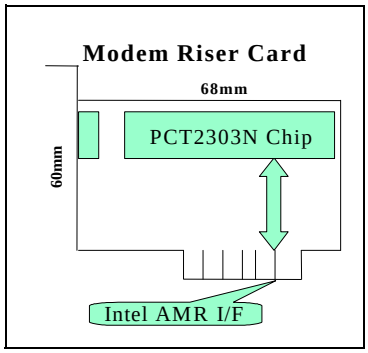
PC-TEL has streamlined the traditional modem into the Host Signal Processing (HSP) solution. Operating with the Pentium class processors, HSP becomes part of the host computer's system software. It requires less power to operate and less physical space than standard modem solutions. PC-TEL's HSP modem is an easily integrated, cost-effective communications solution that is flexible enough to carry you into the future.

The PCT2303N chip set is an integrated direct access arrangement (DAA) and CODEC that provides a programmable line interface to meet requirements. ThePCT 2303N chip set is available in two 16-pin small outline packages (AC'97 interface on PCT303A and phone-line interface on PCT303L). The chip set eliminates the need for an AFE, an isolation transformer, relays, opto-isolators, and 2- to 4-wire hybrid. The PCT2303N chip set dramatically reduces the number of discrete components and cost required to achieve compliance with regulatory requirements. The PCT303A complies with AC'97 Interface specification Rev. 2.1.









FEATURES

Complete DAA includes:

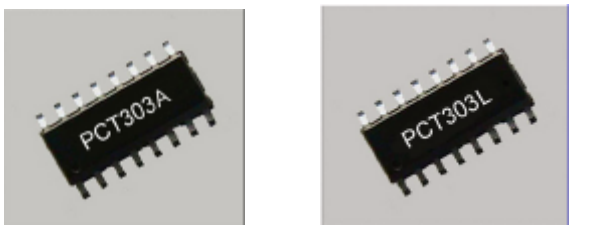
- AC'97 2.1 compliant
- International line interface
- Compliant with FCC Part 68
- 86 dB dynamic range TX/RX paths
- 3.3 to 5 V power supply
- Integrated ring detector
- 2000 V isolation
- Low profile SOIC packages
- Integrated analog front end (AFE)
- Low-power standby mode
- Support for caller ID

APPLICATIONS

- Audio/Modem Riser Card (AMR)
- Mobile Daughter Card (MDC)
- Mini PCI

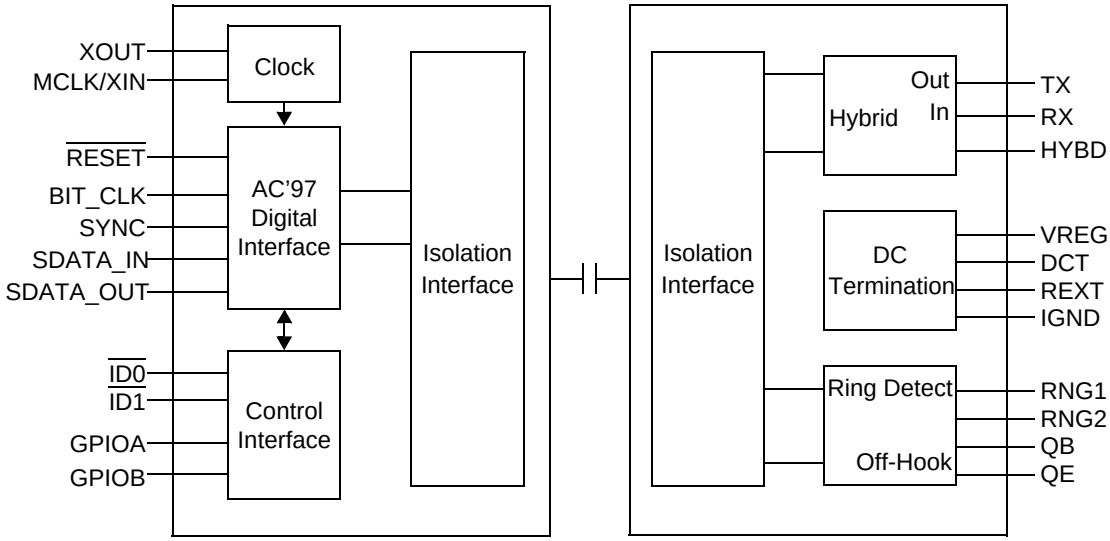
FUNCTIONAL DESCRIPTION

The PCT2303N is an Integrated Direct Access Arrangement (DAA) chipset that provides a digital, low-cost, solid-state interface to a telephone line. The PCT2303N chipset is available in two 16-pin small outline packages (AC'97 interface on PCT303A and phone-line interface on PCT303L). The chipset eliminates the need for an AFE, an isolation transformer, relays, opto-isolators, and 2- to 4-wire hybrid. The PCT2303N chipset dramatically reduces the number of discrete components and cost required to achieve compliance with FCC Part 68. The PCT303A complies with AC'97/MC'97 Interface specification Rev. 2.1.



PCT2303N Chip Set

FUNCTIONAL BLOCK DIAGRAM



PCT303A **PCT303L**

CONTENTS

FIGURES

TABLES

PINOUTS

PCT303A Pinout

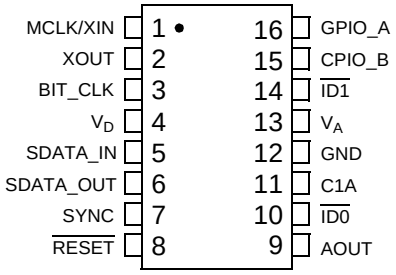


Figure 1 PCT303A 16-Pin SOIC

PCT303L Pinout

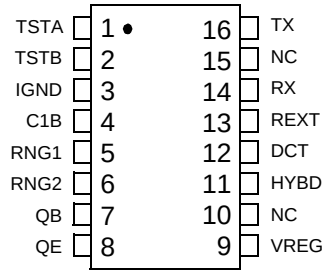


Figure 2 PCT303L 16-Pin SOIC

PIN DESCRIPTIONS

PCT303A Pin Description

Table 1 PCT303A Pin Description

Name	Number	I/O	Description
Serial Interface			
BIT_CLK	3	I/O	Serial port bit clock output/input. Controls the serial data on SDATA_IN and latches the data on SDATA_OUT. Output when configured as primary device. Input when configured as secondary device.
SDATA_IN	5	O	Serial port data out. Serial communication and status data that is provided by the PCT303A to the AC'97 digital controller.
SDATA_OUT	6	I	Serial port data in. Serial communication and control data that is generated by the AC'97 digital controller and presented as an input to the PCT303A.
SYNC	7	I	Frame sync input. Data framing signal that is used to indicate the start and stop of a communication data frame.
$\overline{\text{RESET}}$	8	I	Reset input. An active-low input that is used to reset all control registers to a defined, initialized state. Also used to bring the PCT2303N out of sleep mode.
Miscellaneous Signals			
$\overline{\text{ID0}}$	10	I	Device ID bit 0. Bit 0 of the device configuration.
$\overline{\text{ID1}}$	14	I	Device ID bit 1. Bit 1 of the device configuration.
AOUT	9	O	Analog speaker output. Provides an analog output signal for driving a call progress speaker.
C1A	11	I/O	Isolation capacitor 1A. Connects to one side of the isolation capacitor C1.
MCLK/XIN	1	I	Master clock input/crystal input.
XOUT	2	O	Crystal output.
GPIO_A	16	I/O	General-purpose I/O A. Programmable through registers 4Ch–54h. Default input.
GPIO_B	15	I/O	General-purpose I/O B. Programmable through registers 4Ch–54h. Default input.
Power Signals			
V_D	4	I	Digital supply voltage. Provides the digital supply voltage to the PCT303A. Nominally either 3.3V or 5V.
V_A	13	I	Analog supply voltage. Provides the analog supply voltage to the PCT303A. Nominally 5V.
GND	12	I	Ground. Connects to the system digital ground. Also connects to capacitor C2.

PCT303L Pin Descriptions

Table 2 PCT303L Pin Descriptions

Name	Number	I/O	Description
Line Interface			
TX	16	O	Transmit output. Provides the output, through an AC termination impedance, to the telephone network.
RX	14	I	Receive input. Serves as the receive side input from the telephone network.
DCT	12		DC termination. Provides DC termination to the telephone network.
REXT	13		External resistor. Connects to an external resistor.
RNG1	5	I	Ring 1 input. Connects through a capacitor to the “Tip” lead of the telephone line. Provides the ring and caller ID signals to the PCT2303N.
RNG2	6	I	Ring 2 input. Connects through a capacitor to the “Ring” lead of the telephone line. Provides the ring and caller ID signals to the PCT2303N.
QB	7		Transistor base. Connects to the base of the hookswitch transistor.
QE	8		Transistor emitter. Connects to the emitter of the hookswitch transistor.
HYBD	11	O	Hybrid node output. Balancing capacitor connection used for JATE out-of-band noise support.
Isolation			
C1B	4		Isolation capacitor 1B. Connects to one side of isolation capacitor C1.
IGND	3		Isolated ground. Connects to ground on the line-side interface. Also connects to capacitor C2.
Miscellaneous Signals			
VREG	9		Voltage regulator. Connects to an external capacitor to provide bypassing for an internal voltage regulator.
TSTA	1	I	Test input A. Allows access to test modes, which are reserved for factory use. This pin has an internal pull-up and should be left as a no-connect for normal operation.
TSTB	2	I	Test input B. Allows access to test modes, which are reserved for factory use. This pin has an internal pull-up and should be left as a no-connect for normal operation.
NC	10,15		No connection. This is an unused pin and must be left floating.

FUNCTIONAL DESCRIPTION

The PCT2303N is an integrated chipset that provides a low-cost, isolated, silicon-based MC97-compliant interface to the telephone line. The PCT2303N saves cost and board area by eliminating the need for a modem AFE or serial CODEC. It also eliminates the need for an isolation transformer, relays, opto-isolators, and a 2- to 4-wire hybrid. The PCT2303N solution complies with AC'97/MC'97 Interface specification Rev. 2.1. See AC-Link

AC-link is a bidirectional, fixed rate, serial PCM digital stream. It handles multiple input and output audio streams and control register accesses employing a time division multiplexed (TDM) scheme. The AC-link architecture divides each audio frame into 12 outgoing and 12 incoming data streams, each with 20-bit sample resolution.

The AC-link serial interconnect defines a digital data and control pipe between the controller and the CODEC. The AC-link supports 12 20-bit slots at 48 kHz on SDATA_IN and SDATA_OUT. The TDM "slot-based" architecture supports a per-slot valid tag infrastructure that is the source of each slot's data sets or clears to indicate the validity of the slot data within the current audio frame. For modem AFE, data streams at a variety of required sample rates can be supported.

Isolation Barrier

The PCT2303N achieves an isolation barrier through a low-cost, high-voltage capacitor in conjunction with PC-TEL's proprietary signal processing techniques. These techniques eliminate any signal degradation due to capacitor mismatches, common mode interference, or noise coupling. All transmit, receive, and control data are communicated through this barrier.

Off-Hook

The communication system generates an off-hook command by writing a logic 1 to bit 0 (line 1) or bit 10 (line 2) of slot 12. The off-hook state is used to seize the line for an outgoing call and can also be used for pulse dialing. When the part is not in the off-hook state, negligible DC current flows through the hookswitch. In the off-hook state, the hookswitch transistor pair, Q1 & Q2, turn on.

Ring Detect

The ring signal enters the PCT303L through low-value capacitors connected to Tip and Ring.

The integrated ring detect of the PCT2303N allows it to present the ring signal to the AC'97 controller through the serial port with no additional signaling required. The signal sent to the AC'97 controller is a clipped version of the original ring signal.

The system can detect a ring occurring by the status of the RDT bit of slot 12. This bit is a read-only bit that is set when the line-side device detects a ring signal at RNG1 and RNG2. When this state occurs, the line-side chip draws a small amount of DC current from the line to provide the digitized line data to the AC'97 controller. This bit clears either when the system goes off-hook or four to eight seconds after the last ring is detected.

Lightning Test

The PCT2303N meets the lightning test requirements of FCC part 68.

Safety and Isolation

The PCT2303N meets the requirements of FCC part 68 and UL.

Digital Interface

The ID pins configure the PCT303A as a primary or secondary AC'97 device as shown in Table 3.

Table 3 Device ID Configuration

ID1	ID0	Description
1	1	Primary device
1	0	Secondary device #1
0	1	Secondary device #2
0	0	Factory test

The following sections describe PCT303A operation.

PCT303A as Secondary Device

The PCT303A can operate as a secondary device, which allows up to two PCT303As to exist on the AC-link along with a primary device. The primary device can be an AC'97 Rev. 2.1-compatible CODEC or a PCT303A configured as the primary device. When configured as a secondary device, the PCT303A's BIT_CLK becomes an input and is used as the master clock. Therefore, XIN is not used and should be grounded.

PCT303A as Primary MC'97 CODEC

The PCT2303N can operate as a primary AC'97 Rev 2.1 compatible CODEC. However, when there is an audio AC'97 CODEC present on the AC-link, the PCT2303N should be configured as a secondary CODEC, and the audio AC'97 CODEC should be configured as the primary.

When the PCT303A is configured as a primary device, it requires a 24.576 MHz crystal across the XIN and XOUT pins. An external 24.576 MHz master clock can also be applied to XIN.

PCT303A Connection to AC'97 Controller

The PCT303A communicates with its companion AC'97 controller through a digital serial link called the AC-link. All digital audio streams, optional modem line CODEC streams, and command/status information is communicated over this point to point serial interconnect. Figure 3 illustrates the breakout of the connecting signals.

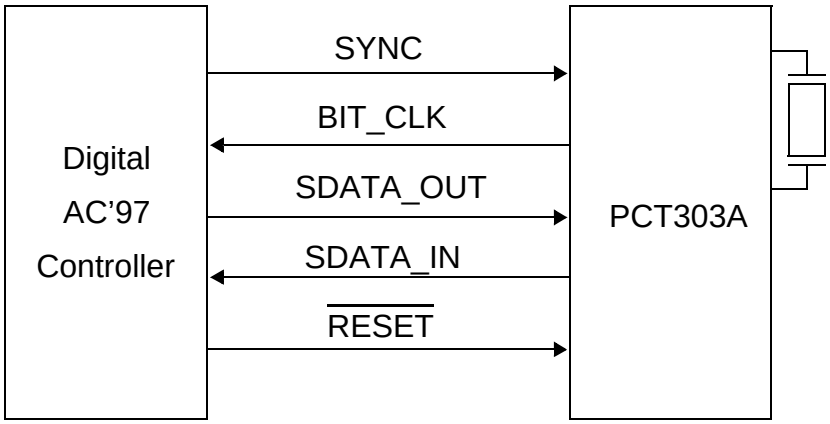


Figure 3 PCT2303N Chipset Connection to AC'97 Controller (Primary Device Configuration)

Clocking

The PCT303A derives its internal clock, when primary, from the 24.576 MHz clock and drives a buffered and divided down (1/2) clock to its digital companion controller over the AC-link through the BIT_CLK signal. Clock jitter at the DACs and ADCs is a fundamental impediment to high quality output, and the internally generated clock provides the PCT303A with a clean clock that is independent of the physical proximity of the PCT303A's companion AC'97 controller.

The beginning of all audio sample packets, or audio frames, transferred over the AC-link is synchronized to the rising edge of the SYNC signal. SYNC is driven by the AC'97 controller. The AC'97 controller takes BIT_CLK as an input and generates SYNC by dividing BIT_CLK by 256 and applying some conditioning to tailor its duty cycle. This yields a 48-kHz SYNC signal whose period defines an audio frame. Data is transitioned on the AC-link on each rising edge of BIT_CLK, and subsequently sampled on the receiving side of the AC-link on each immediately following falling edge of BIT_CLK.

Resetting the PCT2303N

There are three types of reset:

- **Cold reset**—Initializes all PCT2303N logic (registers included) to its default state. Initiated by bringing RESET low at least 1 µs when BIT_CLK is inactive.
- **Warm reset**—Leaves the register contents unaltered. Initiated by bringing SYNC high for at least 1 µs in the absence of BIT_CLK.
- **Register reset**—Initializes only the registers to their default states. Initiated by a write to register 3Ch.

After signaling a reset to the PCT2303N, the AC'97 controller should not attempt to play or capture modem data until it has sampled a CODEC ready indication from the PCT2303N.

AC-Link Digital Serial Interface Protocol

The PCT303A incorporates a 5-pin digital serial interface that links it to the AC'97 controller. The AC-link is a bidirectional, fixed rate, serial PCM digital stream. It handles multiple input and output audio streams (including modems), as well as control register

accesses employing a TDM scheme. The AC-link architecture divides each audio frame into 12 outgoing and 12 incoming data streams, each with 20-bit sample resolution. In primary device mode, the PCT303A data streams are as follows:

- **Control**—Control register write port; two output slots.
- **Status**—Control register read port; two input slots.
- **Modem Line Codec Output**—Modem line CODEC DAC input stream; one output slot per line.
- **Modem Line Codec Input**—Modem line CODEC ADC output stream; one input slot per line.
- **I/O Control**—DAA control and GPIO; one output slot.
- **I/O Status**—DAA status and GPIO; one input slot.

Synchronization of all AC-link data transactions is signaled by the AC'97 controller. The PCT303A drives the serial bit clock onto the AC-link, which the AC'97 controller then qualifies with a synchronization signal to construct audio frames.

The SYNC signal, fixed at 48 kHz, is derived by dividing down the serial bit clock (BIT_CLK). BIT_CLK, fixed at 12.288 MHz, provides the necessary clocking granularity to support 12 20-bit outgoing and incoming time slots. AC-link serial data is transitioned on each rising edge of BIT_CLK. The receiver of AC-link data, the PCT303A for outgoing data and the AC'97 controller for incoming data, samples each serial bit on the falling edges of BIT_CLK.

The AC-link protocol provides for a special 16-bit time slot (Slot 0) wherein each bit conveys a valid tag for its corresponding time slot within the current audio frame. A 1 in a given bit position of slot 0 indicates that the corresponding time slot within the current audio frame has been assigned to a data stream and contains valid data. If a slot is tagged invalid, it is the responsibility of the data source (the PCT303A for the input stream, the AC'97 controller for the output stream) to populate all bit positions with 0s during that slot's active time.

SYNC remains high for a total duration of 16 BIT_CLKs at the beginning of each audio frame. The portion of the audio frame where SYNC is high is called the Tag Phase. The remainder of the audio frame where SYNC is low is called the Data Phase.

Additionally, for power savings, all clock, sync, and data signals can be halted. The PCT2303N maintains its register contents intact when entering a power-savings mode.

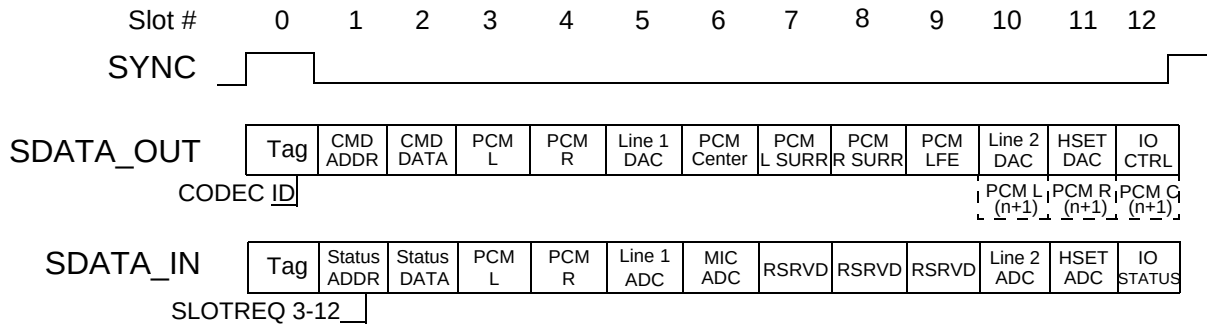


Figure 4 Standard Bidirectional Audio Frame

Audio Output Frame (SDATA_OUT)

The audio output frame data streams correspond to the multiplexed bundles of all digital output data targeting the PCT2303N's DAC inputs and control registers. Each audio output frame supports up to 12 20-bit outgoing data time slots. Slot 0 is a special reserved time slot containing 16 bits used for AC-link protocol infrastructure.

Within slot 0, the first bit is a global bit (SDATA_OUT slot 0, bit 15) which flags the validity for the entire audio frame. If the valid frame bit is a 1, the current audio frame contains at least one slot time of valid data. The next 12 bit positions sampled by the PCT303A indicate which of the corresponding 12 time slots contain valid data. In this way, data streams of differing sample rates can be transmitted across the AC-link at its fixed 48-kHz audio frame rate. Figure 5 illustrates the time slot-based AC-link protocol.

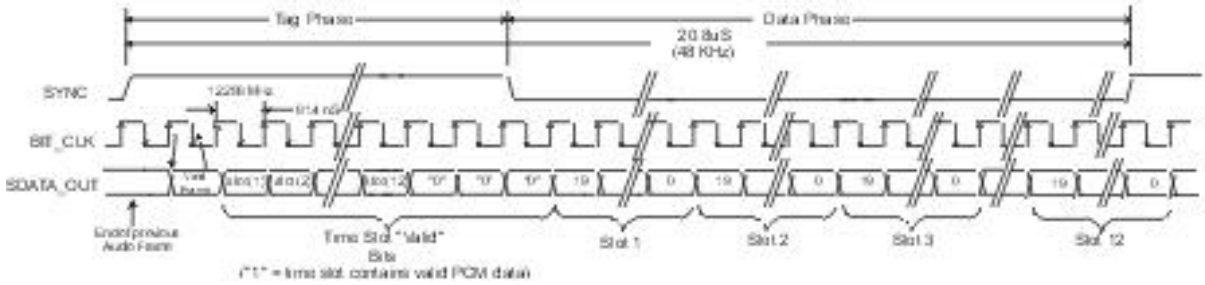


Figure 5 AC-Link Audio Output Frame

A new audio output frame begins with a low to high transition of SYNC. SYNC is synchronous to the rising edge of BIT_CLK. On the immediately following falling edge of BIT_CLK, the PCT303A samples the assertion of SYNC. This falling edge marks the time when both sides of the AC-link are aware of the start of a new audio frame. On the next rising of BIT_CLK, the AC'97 controller transitions SDATA_OUT into the first bit position of slot 0 (valid frame bit). Each new bit position is presented to the AC-link on a rising edge of BIT_CLK, and subsequently sampled by the PCT303A on the following falling edge of BIT_CLK. This sequence ensures that data transitions and subsequent sample points for both incoming and outgoing data streams are time aligned. See Figure 6.

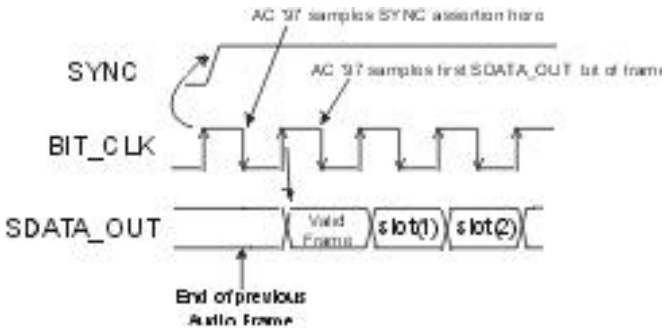


Figure 6 Start of an Audio Output Frame

SDATA_OUT's composite stream is MSB justified (MSB first) with all non-valid slots' bit positions padded with 0s by the AC'97 controller.

In the event that there are less than 20 valid bits within an assigned and valid time slot, the AC'97 controller always pads all trailing non-valid bit positions of the 20-bit slot with 0s.

Variable Sample Rate Signaling Protocol

For variable sample rate output, the CODEC examines its sample rate control registers, the state of its FIFOs, and the incoming SDATA_OUT tag bits at the beginning of each audio output frame to determine which SLOTREQ bits (bit 4 or 9 in Input Slot 1) to set active (low). SLOTREQ bits asserted during the current audio input frame signal which *active output slots* require data from the AC'97 Digital Controller in the next audio output frame. An *active output slot* is defined as any slot supported by the CODEC that is not in a power-down state.

Slot 1: Command Address Port

The command address port controls features and monitors status (see Audio Input Frame Slots 1 and 2) for PCT2303N functions including, but not limited to, sample rate, AFE configuration, and power management.

The control interface architecture supports up to 64 16-bit read/write registers addressable on even byte boundaries. Only the even registers (00h, 02h, etc.) are valid; odd register (01h, 03h, etc.) writes are ignored and reads return 0. Note that shadowing of the control register file on the AC'97 controller is an option left open to the implementation of the AC'97 controller. The PCT2303N's control register file is readable as well as writable to provide more robust testability.

Audio output frame slot 1 communicates control register address and write/read command information to the PCT2303N.

Command Address Port bit assignments:

- Bit 19—Read/write command (1=read, 0=write)
- Bits 18:12—Control register index (64 16-bit locations, addressed on even byte boundaries)
- Bits 11:0—Reserved (padded with 0s)

The first bit (MSB) sampled by the PCT303A indicates whether the current control transaction is a read or a write operation. The following seven bit positions communicate the targeted control register address. The trailing 12 bit positions within the slot are reserved and must be padded with 0s by the AC'97 controller.

Slot 2: Command Data Port

The command data port delivers 16-bit control register write data in the event that the current command port operation is a write cycle as indicated by Slot 1, bit 19.

Command Data Port bit assignments:

- Bits 19:4—Control register write data (padded with 0s if the current operation is a read)
- Bits 3:0—Reserved (padded with 0s)

Slot 5: Modem Line 1 Codec

Modem output frame slot 5 contains the MSB justified modem DAC input data for phone line #1.

The PCT2303N's modem DAC input resolution is 16 bits.

Slot 10: Modem Line 2 DAC

Line 2 is assigned to slot 10. The leading 16 bits of each slot must contain valid sample data (MSB bit 19, LSB 4).

Slot 12: Modem GPIO Control

Slot 12 contains latency critical signals for the PCT303L and the GPIO of the PCT303A. See Table 4.

Slots 3, 4, 6–9, 11: Not Used

The PCT2303N always pads audio output frame slots 3, 4, 6–9, and 11 with 0s.

Table 4 Slot 12

GPIO	Name	Sense	Description
GPIO15	LINE2_GPIO_B	in/out	GPIO pin B, Line 2
GPIO14	LINE2_GPIO_A	in/out	GPIO pin A, Line 2
GPIO13	LINE2_DLCS	in	Delta loop current sense, Line 2
GPIO12	LINE2_CID	out	Caller ID path enable, Line 2
GPIO11	LINE2_RI	in	Ring detect, Line 2
GPIO10	LINE2_OH	out	Off hook, Line 2
GPIO[9:6]	Reserved		
GPIO5	LINE1_GPIO_B	in/out	GPIO pin B, Line 1
GPIO4	LINE1_GPIO_A	in/out	GPIO pin A, Line 1
GPIO3	LINE1_DLCS	in	Delta loop current sense, Line 1
GPIO2	LINE1_CID	out	Caller ID path enable, Line 1
GPIO1	LINE1_RI	in	Ring detect, Line 1
GPIO0	LINE1_OH	out	Off hook, Line 1
Vendor Optional			
Bit 3	Reserved		
Bit 2	LINE2_FDT	in	Frame detect, Line 2
Bit 1	LINE1_FDT	in	Frame detect, Line 1
Bit 0	GPIO_INT	in	GPIO state change

Audio Input Frame (SDATA_IN)

The audio input frame data streams correspond to the multiplexed bundles of all digital input data targeting the AC'97 controller. This is the case with the audio output frame; each AC-link audio input frame consists of 12 20-bit time slots. Slot 0 is a special reserved time slot containing 16 bits that are used by the AC-link protocol infrastructure.

Within slot 0, the first bit is a global bit (SDATA_IN slot 0, bit 15) that flags whether the PCT303A is in the CODEC ready state or not. If the CODEC ready bit is a 0, the PCT303A is not ready for normal operation. This condition is normal following the deassertion of reset (e.g., while the PCT303A's voltage references settle). When the AC-link CODEC ready indicator bit is a 1, the AC-link and PCT303A control and status registers are in a fully operational state. The AC'97 controller must further probe the power-down control/status register to determine exactly which subsections, if any, are ready.

Before any attempts to put the PCT2303N into operation, the AC'97 controller must poll the first bit in the audio input frame (SDATA_IN slot 0, bit 15) for an indication that the PCT303A is CODEC ready. When the PCT303A is sampled CODEC ready, then the next 12 bit positions sampled by the AC'97 controller indicate which of the corresponding 12 time slots are assigned to input data streams, and that they contain valid data. Figure 7 illustrates the time slot-based AC-link protocol.

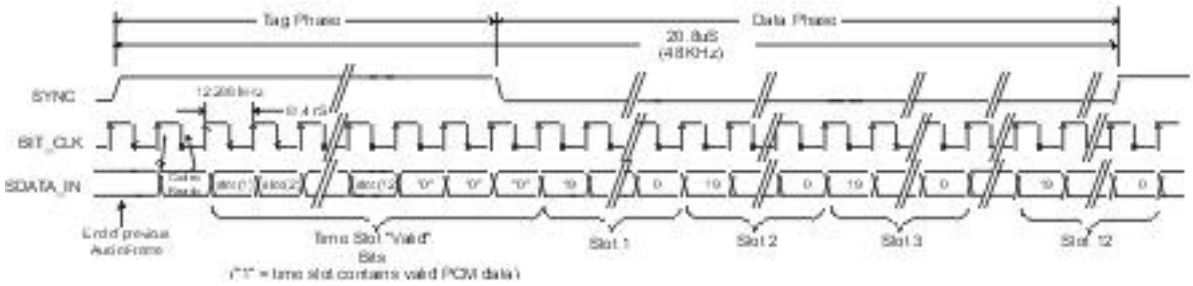


Figure 7 AC-Link Audio Input Frame

A new audio input frame begins with a low to high transition of SYNC. SYNC is synchronous to the rising edge of BIT_CLK. On the immediately following falling edge of BIT_CLK, the PCT303A samples the assertion of SYNC. This falling edge marks the time when both sides of the AC-link are aware of the start of a new audio frame. On the next rising of BIT_CLK, the PCT303A transitions SDATA_IN into the first bit position of slot 0 (CODEC ready bit). Each new bit position is presented to the AC-link on a rising edge of BIT_CLK and subsequently sampled by the AC'97 controller on the following falling edge of BIT_CLK. This sequence ensures that data transitions and subsequent sample points for both incoming and outgoing data streams are time aligned.

SDATA_IN's composite stream is MSB justified (MSB first) with all non-valid bit positions (for assigned and unassigned time slots) padded with 0s by the PCT303A. SDATA_IN data is sampled on the falling edges of BIT_CLK by the AC'97 controller.

Slot 1: Status Address Port

The status address port monitors status for PCT303A functions including, but not limited to, line-side configuration.

Audio input frame slot 1's stream echoes the control register index, for historical reference, for the data to be returned in slot 2. (Assuming that slots 1 and 2 had been tagged "valid" by the PCT303A during slot 0).

Status Address Port bit assignments:

- Bit 19—Reserved (padded with 0)
- Bits 18:12—Control register index (Echo of register index for which data is being returned)
- Bits 11:2—SLOTREQ bits, bit 9 for Line 1 and bit 4 for Line 2. (See "Variable Sample Rate Signaling Protocol" on page 11 for more details).
- Bits 1:0—Reserved (padded with 0s)

The first bit (MSB) generated by the PCT303A is always padded with a 0. The following seven bit positions communicate the associated control register address and the trailing 12 bit positions are padded with 0s by the PCT303A.

Slot 2: Status Data Port

The status data port delivers 16-bit control register read data.

Status Data Port bit assignments:

- Bits 19:4—Control register read data (padded with 0s if tagged Invalid by the PCT303A)
- Bits 3:0—Reserved (padded with 0s)

If Slot 2 is tagged Invalid by the PCT303A, then the entire slot is padded with 0s by the PCT303A.

Slot 5: Modem Line 1 Codec

Audio input frame slot 5 contains MSB-justified modem ADC output data for phone line #1 (ID = 0 or 1).

The modem ADC output resolution is 16 bits.

The PCT2303N ships out its ADC output data (MSB first), and pads any trailing non-valid bit positions with 0s to fill out its 20-bit time slot.

Slot 10: Modem Line 2 Code

Audio input frame for Line 2.

Slot 12: Modem GPIO Status

Slot 12 contains latency critical signals for PCT303L and the GPIO of the PCT303A. Slot 12 also reflects the status of the link between the PCT303A and PCT303L. Table 4 on page 12.

AC-Link Low Power Mode

The AC-link signals can be placed in a low-power mode. When AC'97's power-down register is programmed to the appropriate value, both BIT_CLK and SDATA_IN are brought to, and held, at a logic low voltage level.

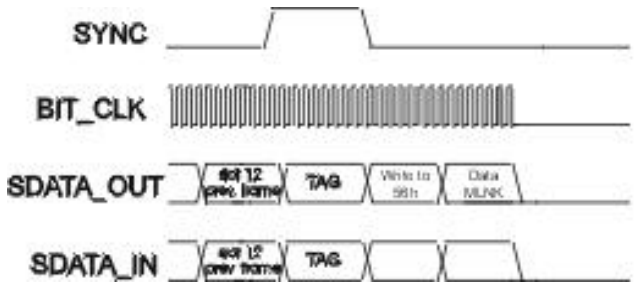


Figure 8 AC-Link Power-down Timing

BIT_CLK and SDATA_IN are transitioned low immediately following the decode of the write to the register 56h with MLNK. When the AC'97 controller driver is at the point where it is ready to program the AC-link into its low-power mode, slots 1 and 2 are assumed to be the only valid stream in the audio output frame.

The AC'97 controller should also drive SYNC and SDATA_OUT low after programming the PCT2303N to this low-power mode.

When the PCT2303N has been instructed to halt BIT_CLK, a special wake up protocol must be used to bring the AC-link to the active mode because normal audio output and input frames cannot be communicated in the absence of BIT_CLK.

NOTE: The PCT2303N's PLL must be initialized before being placed in sleep mode. PLL is initialized by writing a sample rate in register 40h (42h).

Waking Up the AC-Link

There are two methods for bringing the AC-link out of a low-power, halted mode. Regardless of the method, the AC'97 controller performs the wake-up task.

AC-link protocol provides for a cold reset and a warm reset. The current power down state ultimately dictates which form of reset is appropriate. Unless a cold or register reset (a write to the reset register) is performed, wherein the registers are initialized to their default values, registers are required to keep state during all power-down modes.

When powered down, reactivation of the AC-link through reassertion of the SYNC signal must not occur for a minimum of four audio frame times following the frame in which the power down was triggered. When the AC-link powers up, the PCT303A indicates readiness through the CODEC ready bit (input slot 0, bit 15).

The PCT2303N can be enabled to indicate a power management event has occurred (e.g., ring detection) while in low-power mode. See "GPIO Pin Wake-Up Mask (Register 52h, R/W)" on page 21 for more details.

PCT2303N Cold Reset

A cold reset is achieved by asserting $\overline{\text{RESET}}$ for the minimum specified time. By driving $\overline{\text{RESET}}$ low, BIT_CLK and SDATA_OUT are activated, or re-activated, and all PCT2303N control registers are initialized to their default power on reset values. It should be noted that while $\overline{\text{RESET}}$ is low, the PCT2303N remains active. Upon the rising edge of $\overline{\text{RESET}}$ the PCT303A performs a cold reset.

$\overline{\text{RESET}}$ is an asynchronous PCT303A input.

PCT2303N Warm Reset

A warm reset reactivates the AC-link without altering the current PCT2303N register values. A warm reset is signaled by driving SYNC high for a minimum of 1 µs in the absence of BIT_CLK.

Within normal audio frames, SYNC is a synchronous PCT303A input. However, in the absence of BIT_CLK, SYNC is treated as an asynchronous input used in the generation of a warm reset to the PCT2303N.

The primary AC'97 CODEC does NOT respond with the activation of BIT_CLK until SYNC has been sampled low again by AC'97. This precludes the false detection of a new audio frame.

Analog Output

The PCT303A supports an analog output (AOUT) for driving the call progress speaker found with most of today's modems. AOUT is an analog signal comprised of a mix of the transmit and receive signals. The receive portion of this mixed signal has a 0 dB gain while the transmit signal has a gain of –20 dB.

The transmit and receive portions of the AOUT signal have independent mute controls found in register 5Ch. Developer's kit application schematics illustrate a recommended application circuit. Note that in the configuration shown, the LM386 provides a gain of 26 dB. Make additional gain adjustments by varying R1.

On-hook Line Monitor (CID)

The PCT2303N allows the user to detect line activity when the device is in an on-hook state. When the system is on-hook, the line data can be passed to the AC'97 controller across the serial port while drawing a small amount of DC current from the line. This process is identical to the passing of line information while on-hook following a ring signal detection. To activate this feature, set the LINE1_CID/LINE2_CID bit in slot 12.

Loop Current Monitor

When the system is in an off-hook state, the LCS bits of register 5Ch indicate the approximate amount of DC loop current that is flowing in the loop. The LCS is a 4-bit value ranging from zero to fifteen. Each unit represents approximately 6 mA of loop current from LCS codes 1-14. The typical LCS transfer function is shown in Figure 9.

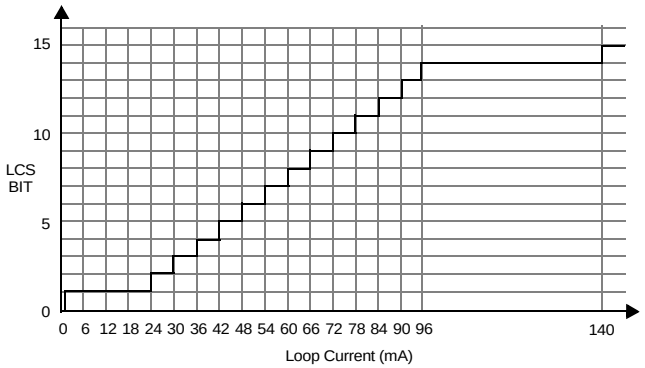


Figure 9 Typical LCS Transfer Function

An LCS value of zero means the loop current is less than required for normal operation and the system should be on-hook. Typically, an LCS value of 15 means the loop current is greater than 120mA.

The LCS detector has a built-in hysteresis of 2 mA of current. This allows for a stable LCS value when the loop current is near a transition level. The LCS value is a rough approximation of the loop current, and the designer is advised to use this value in a relative means rather than an absolute value.

This feature enables the modem to determine if an additional line has "picked up" while the modem is transferring information. In the case of a second phone going off-hook, the loop current falls approximately 50% and is reflected in the value of the LCS bits.

Gain Control

The PCT2303N supports multiple gain and attenuation settings in register 46h/48h for the receive and transmit paths, respectively. The receive path can support gains of 0, 3, 6, 9, and 12 dB. The gain is selected by bits 3:1 (ADC3:1). The receive path can also be muted by setting bit 7. The transmit path can support attenuations of 0, 3, 6, 9, and 12 dB. The attenuation is selected by bits 11:9 (DAC3:1). The transmit path can also be muted by setting bit 15.

Filter Selection

The PCT303A supports additional filter selections for the receive and transmit signals. The IIRE bit of register 5Ch, when set, enables the IIR filters. This filter provides a much lower, however non-linear, group delay than the default FIR filters.

Charge Pump

The PCT303A has an integrated charge pump for 3.3 V-only operation. The ISOcap requires a 5 V supply that can come from either the V_A pin or the internal charge pump. For 3.3 V-only operation, R3 must not be installed. The charge pump by default is set to be the 5 V supply after the sample rate register is programmed. To use a separate 5 V supply, connect 5 V through R3 and set register 5Eh, bit 10 (PDC) to 1. The PDC must be set before the sample rate register is written.

In-Circuit Testing

The PCT2303N's advanced design provides the modem manufacturer with increased ability to determine system functionality during production line tests, as well as user diagnostics. Several loopback modes exist allowing increased coverage of system components.

The loopback mode allows the data pump to provide a digital input test pattern on SDATA_IN and receive that digital test pattern back on SDATA_OUT. To enable this mode, set L1B2:0(L2B2:0)=101 in register 56h. In this mode, the isolation barrier is actually being tested. The digital stream is delivered across the isolation capacitors, C1 and C2 to the line-side device and returned across the same barrier.

The digital DAC loopback mode allows data to be sent on the digital path from SDATA_IN to the digital section of DAC to ADC to SDATA_OUT. This loopback mode is used when the line-side chip is in power-down mode. To enable this mode, set L1B2:0(L2B2:0) = 011 in register 56h.

The remote analog loopback mode allows an external device to drive the receive pins of the line-side chip and receive the signal from the transmit pins. This mode allows testing of external components connecting the RJ-11 jack (Tip and Ring) to the line side of the PCT303L. To enable this mode, set L1B2:0(L2B2:0) = 100 in register 56h.

The ADC loopback mode allows an external device to drive the receive pins of the PCT303L. The signal is then digitized on the PCT303L and sent to the PCT303A, which sends the data back to the PCT303L. The signal is then converted back to analog. The external device receives the signal on the transmit pins. This mode allows testing of the PCT2303N's converters and external devices between the PCT303L and RJ-11 jack. To enable this mode, set the L1B2:0(L2B2:0) = 001.

The final two testing modes, local analog loopback and external analog loopback, allow the system to test the basic operation of the converters on the line side and the functionality of the external components. In local analog loopback mode, the AC'97 controller provides a digital test waveform on SDATA_IN. This data is passed across the isolation barrier, converted to analog, internally looped to the receive path, converted to digital, passed back across the isolation barrier, and presented to the AC'97 controller. To enable local and analog loopback, set L1B2:0 (L2B2:0) = 010. External analog loopback mode allows the system to test external components by passing converted data (from SDATA_IN) to the transmit pin, which is looped externally to the receive pin. To enable external analog loopback, set L1B2:0 (L2B2:0) = 110. Both analog loopback modes require power, which is typically supplied by the loop current from Tip and Ring.

CONTROL REGISTERS

Any register not listed here is reserved and should not be written. Undefined/unimplemented registers return 0.

Extended Modem ID (Register 3Ch, R/W)

ID[1:0]		Reserved												LIN2	LIN1
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**

Reset settings (dependent on pins $\overline{ID1}$ and $\overline{ID0}$) = 0001h; 8002h; 4001h; Cxxxh

Bit Definitions:

Bits	Name	Description
15:14	ID[1:0]	Indicates CODEC configuration.

ID[1:0]	Description
00	Primary
01	Secondary
10	Secondary
11	Factory test

13:2	Reserved	Reserved.
1	LIN2	1 = 2nd line is supported; ID[1:0] = 10. CODEC data is transferred in slot 10.
0	LIN1	1 = 1st line is supported; ID[1:0] = 01. CODEC data is transferred in slot 5.

Extended Modem Status and Control (Register 3Eh, R/W)

Reserved		PRF	PRE	PRD	PRC	PRB	PRA	Reserved		DAC2	ADC2	DAC1	ADC1	MREF	GPIO
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**

Reset settings = FF00h

Bits 13:8 are read/write and control modem AFE subsystem power-down. When these bits are all set to 1, the PCT303L is powered down. Bits 7:0 are read-only; 1 indicates modem AFE subsystem readiness.

Bit Definitions:

Bits	Name	Description
15:14	Reserved	Reserved.
13	PRF	1 = Modem line 2 DAC off.
12	PRE	1 = Modem line 2 ADC off.
11	PRD	1 = Modem line 1 DAC off.
10	PRC	1 = Modem line 1 ADC off.
9	PRB	Reserved for future use.
8	PRA	1 = GPIO power-down.
7:6	Reserved	Reserved.
5	DAC2	Read-only. 1 = Modem line 2 DAC ready.
4	ADC2	Read-only. 1 = Modem line 2 ADC ready.
3	DAC1	Read-only. 1 = Modem line 1 DAC ready.
2	ADC1	Read-only. 1 = Modem line 1 ADC ready.
1	MREF	Read-only. 1 = Modem Vrefs up to nominal level.
0	GPIO	Read-only. 1 = GPIO ready.

Line 1 DAC/ADC Rate (Register 40h, R/W)

SR[15:0]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Reset settings = 0000h

Each DAC/ADC pair is governed by a read/write modem sample rate control register that contains a 16-bit unsigned value between 0 and 65535, representing the rate of operation in Hz. A number written over 2EE0h causes the sample rate to 13.714 kHz. For all rates, if the value written to the register is supported, that value is echoed back when read, otherwise the closest rate supported is returned.

When set to zero, the internal PLL is disabled. The PLL should be programmed before the line-side (PCT303L) is activated through clearing any PR bit in register 3Eh. Sleep mode is not supported when the PLL is disabled.

Table 5 Sample rates for Line 1 and Line 2

Sample Rate	D[15:0]
7200	1C20h
8000	1F40h
8228.57 (57600/7)	2024h
8400	20D0h
9000	2328h
9600	2580h
10285.71 (72000/7)	282Dh
12000	2EE0h
13714.28 (96000/7)	3592h

Line 2 DAC/ADC Rate (Register 42h, R/W)

SR[15:0]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Reset settings = 0000h

Sample rates for line 2 are the same as for line 1, refer to Table 5.

Line 1 DAC/ADC Level (Register 46h, R/W)

Mute	Reserved			DAC[3:1]			R	Mute	Reserved			ADC[3:1]			R
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**

Reset settings = 8080h

This read/write register controls the modem AFE DAC and ADC levels. The default value after cold register reset for this register (8080h) corresponds to 0 db DAC attenuation with mute on and 0 db ADC gain with mute on.

Bit Definitions:

Bits	Name	Description
15	Mute	Transmit mute. 1 = Mute on.
14:12	Reserved	Reserved.
11:9	DAC[3:1]	Analog transmit attenuation.

DAC[3:1]	Description
000	0db attenuation.
001	3db attenuation.
010	6db attenuation.
011	9db attenuation.
1xx	12db attenuation.

8	Reserved	Reserved.
7	Mute	Receive mute. 1 = Mute on.
6:4	Reserved	Reserved.
3:1	ADC[3:1]	Analog receive gain.

ADC[3:1]	Description
000	0dB gain.
001	3dB gain.
010	6dB gain.
011	9dB gain.
1xx	12dB gain.

0	Reserved	Reserved.

Line 2 DAC/ADC Level (Register 48h, R/W)

Mute	Reserved			DAC[3:1]			R	Mute	Reserved			ADC[3:1]			R
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Reset settings = 8080h

This read/write register controls the modem AFE DAC and ADC levels. The default value after cold register reset for this register (8080h) corresponds to 0 dB DAC attenuation with mute on and 0 dB ADC gain with mute on.

Bit Definitions:

Bits	Name	Description
15	Mute	Transmit mute. 1 = Mute on.
14:12	Reserved	Reserved.
11:9	DAC[3:1]	Analog transmit attenuation.

DAC[3:1]	Description
000	0dB attenuation.
001	3dB attenuation.
010	6dB attenuation.
011	9dB attenuation.
1xx	12dB attenuation.

8	Reserved	Reserved.
7	Mute	Receive mute. 1 = Mute on.
6:4	Reserved	Reserved.
3:1	ADC[3:1]	Analog receive gain.

ADC[3:1]	Description
000	0dB gain.
001	3dB gain.
010	6dB gain.
011	9dB gain.
1xx	12dB gain.

0	Reserved	Reserved. Read returns zero.

GPIO Pin Configuration (Register 4Ch, R/W)

GC[15:10]						Reserved				GC[5:0]					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Reset setting for line 1 device = 003Fh
Reset setting for line 2 device = FC00h

The GPIO pin configuration register is read/write for configuring slot 12 I/O. These pins are digital commands (virtual pins). This register specifies whether a GPIO pin is configured for input (1) or output (0). The digital controller sends the desired GPIO pin value over output slot 12 in the outgoing stream of the AC-link before configuring any of these bits for output.

GPIO Pin Polarity and Type (Register 4Eh, R/W)

GP[15:10]						Reserved				GP[5:0]					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**

Reset settings = FFFFh

The GPIO pin polarity and type register is read/write for selecting the polarity and type for slot 12 I/O. This register defines GPIO input polarity (0 = low; 1 = high active) when a GPIO pin is configured as an input. It defines GPIO output type (0 = CMOS; 1 = OPEN-DRAIN) when a GPIO pin is configured as an output. The default value after soft reset (FFFFh) is all pins active-high. Unimplemented GPIO pins always return 1s.

GPIO Pin Sticky (Register 50h, R/W)

GS[15:13]			R	GS11	Reserved					GS[5:3]			R	GS1	R
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**

Reset settings = 0000h

The GPIO pin sticky register is a read/write register. It defines the GPIO input type (0 = non-sticky; 1 = sticky) when a GPIO pin (defined in slot 12 I/O) is configured as an input. This applies to ring detect, delta loop current sense, and GPIO_A bits.

GPIO inputs configured as sticky are cleared only by writing a 0 to the corresponding bit of the GPIO pin status register 54h, and by reset. The default value after cold register reset (0000h) is all pins non-sticky. Unimplemented GPIO pins always return zeros. Sticky is defined as edge-sensitive; non-sticky is defined as level-sensitive.

GPIO Pin Wake-Up Mask (Register 52h, R/W)

GW[15:10]						Reserved				GW[5:0]					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**

Reset settings = 0000h

The GPIO pin wake-up mask register is a read/write register that provides a mask for determining if an input GPIO change will generate a wake-up or GPIO_INT (0 = No; 1 = Yes). When the AC-link is powered down, a wake-up event triggers the assertion of SDATA_IN. When the AC-link is powered up, a wake-up event appears as GPIO_INT = 1 on bit 0 of input slot 12. Ring-detection wake-up can be enabled or disabled.

An AC-Link wake-up interrupt is defined as a 0-to-1 transition on SDATA_IN when the AC-link is powered down. GPIO bits that have been programmed as inputs, sticky, and pin wake-up, upon transition (either high-to-low or low-to-high) depending on pin polarity, cause an AC-link wake-up event, if the AC-link was powered down.

The default value after cold register reset (0000h) defaults to all 0s specifying no wake-up event. This applies to ring detect, delta loop current sense, GPIO_A, and GPIO_B bits. Unimplemented GPIO pins always return 0s.

GPIO Pin Status (Register 54h, R/W)

GI[15:10]						Reserved				GI[5:0]					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**

Reset settings = xxxxh

The GPIO status register is a read/write register that reflects the state of all GPIO pins (inputs and outputs) on slot 12. The value of all GPIO pin inputs and outputs comes from each frame on slot 12, but is also available for reading as GPIO pin status through the standard slot 1 and 2 command address/data protocols. GPIO inputs configured as sticky are cleared by writing a 0 to the corresponding bit of this register. This should be the last event before setting the AC'97 MLNK bit.

Bits corresponding to unimplemented GPIO pins should be forced to zero in this register and input slot 12.

GPIO bits that have been programmed as inputs and sticky, upon transition (high-to-low or low-to-high), cause the individual GI bit to go asserted to 1, and remain asserted until a write of 0 to that bit. The only way to set the desired value of a GPIO output pin is to set the control bit in output slot 12.

If configured as an input, the default value after register reset is always the state of the GPIO pin.

Miscellaneous Modem AFE Status and Control (Register 56h, R/W)

Reserved			MLNK	Reserved					L2B[2:0]			R	L1B[2:0]		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**

Reset settings = 0000h

This read/write register defines the loopback modes available for the modem line ADCs/DACs. The default value after cold register reset (0000h) is all loopbacks disabled.

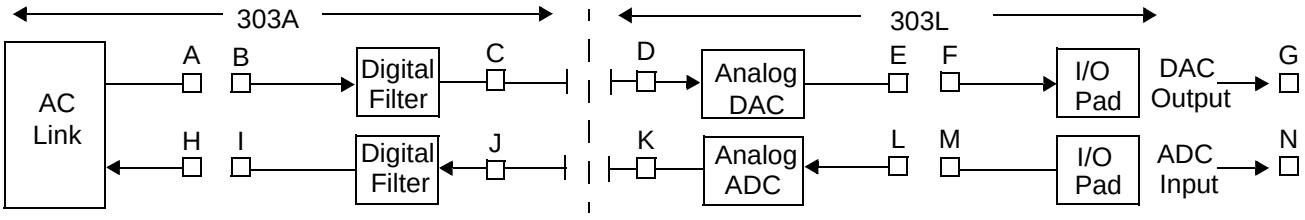
Bit Definitions:

Bits	Name	Description
15:13	Reserved	Reserved. Read returns zero.
12	MLNK	Controls an MC'97's AC-link status. 1 = Sets the MC'97 AC-link to off (sleep). 0 = Sets the MC'97 AC-link to on (active).
11:7	Reserved	Reserved. Read returns zero.
6:4	L2B[2:0]	Line 2 loopback modes.

L2B[2:0]	Description
000	Disabled (default).
001	ADC loopback (I'B).
010	Local analog loopback (F'M).
011	Digital DAC loopback (C'J).
100	Remote analog loopback (M''F).
101	Isolation Cap loopback (D'K).
110	External analog loopback (G'N).
111	Reserved.

3	Reserved	Reserved. Read returns zero.
2:0	L1B[2:0]	Line 1 loopback modes.

L1B[2:0]	Description
000	Disabled (default).
001	ADC loopback (I'B).
010	Local analog loopback (F'M).
011	Digital DAC loopback (C'J).
100	Remote analog loopback (M'F).
101	Isolation Cap loopback (D'K).
110	External analog loopback (G'N).
111	Reserved.



NOTE: For all loopback modes except 011, line side must be powered on and off-hook.

Figure 10 Loopback Points

Chip ID and Revision (Register 5Ah, R)

Reserved							CBID	REVB[3:0]				REVA[3:0]			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Reset settings = N/A

NOTE: The line side must be activated through the PR bits before valid read.

Bit Definitions:

Bits	Name	Description
15:9	Reserved	Reserved. Read returns zero.
8	CBID	Chip B (line-side) ID. 1 = Line side has international support. 0 = Line side is domestic.
7:4	REVB[3:0]	Chip revision. Four-bit value indicates the PCT303L (line-side) silicon revision.
3:0	REVA[3:0]	Chip revision. Four-bit value indicates the PCT303A silicon revision.

Line-Side Configuration 1 (Register 5Ch, R/W)

ARM[1:0]		ATM[1:0]		IIRE	Resereved								Reserved		RT
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Reset settings = F010h

Shaded bit descriptions are for international line-side support only.

Bit Definitions:

Bits	Name	Description
15:14	ARM[1:0]	Analog (call progress) receive path mute.

ARM[1:0]	Description
00	0dB
01	–6dB
10	–12dB
11	Mute

Bits	Name	Description
13:12	ATM[1:0]	Analog (call progress) transmit path mute.

ARM[1:0]	Description
00	0dB
01	–6dB
10	–12dB
11	Mute

11	IIRE	IIR filter enable. 1 = Transmit and receive filters are realized with an IIR filter characteristic.
2:1	Reserved	Reserved. Read returns zero.

Line-Side Configuration 2 (Register 5Eh, R/W)

Reserved					PDC	Reserved		CLE	FDT	LCS[3:0]				Reserved	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**

Reset settings = 0000h

NOTE: The line side must be activated through the PR bits before valid read/write.

Shaded bit descriptions are for international line-side support only.

Bit Definitions:

Bits	Name	Description
15:11	Reserved	Reserved. Read returns zero.
10	PDC	Charge pump disable. This bit disables the internal charge pump when set.
7	CLE	Com link error. 1 = A communication problem exists between the PCT303A and the PCT303L. When this bit goes high, it remains high until a logic 0 is written to it.
6	FDT	Frame detect. 1 = Isolation Cap frame lock has been established. 0 = Isolation Cap communication has not established frame lock.
5:2	LCS[3:0]	Loop current sense. Four-bit value returning the loop current in 6 mA increments.

LCS[3:0]	Description
0	Loop current < 6 mA.
1111	Loop current >120 mA.

Vendor ID (Register 7Ch, R/W)

F[7:0]								S[7:0]							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**

Vendor ID (Register 7Eh, R/W)

T[7:0]								REV[7:0]							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**

Reset settings = N/A

These registers are for specific vendor identification. The ID method is Microsoft's Plug and Play Vendor ID code with F7..0 being the first character of that ID, S7..0 being the second character, and T7..0 the third character. These three characters are ASCII encoded.

ELECTRICAL CHARACTERISTICS

Recommended Operating Conditions

Table 6 Recommended Operating Conditions

Parameter [a]	Symbol	Test Condition	Min [b]	Typ	Max [b]	Unit
Ambient temperature	T_A	K-grade	0	25	70	°C
Ambient temperature	T_A	B-grade	0	25	90	°C
PCT303A supply voltage, analog	V_A		4.50	5.0	5.50	V
PCT303A supply voltage, digital [c]	V_D		3.0	3.3/5.0	5.50	V

a. The PCT2303N chipset specifications are guaranteed when the typical application circuit (including component tolerance) and any PCT303A and PCT303L are used.
b. All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25°C unless otherwise stated.
c. The digital supply, V_D, can operate from either 3.3V or 5.0V. The PCT303A supports interface to 3.3V logic when operating from 3.3V. The 3.3V operation applies to both the serial port and the digital signals $\overline{\text{RESET}}$, ID0, and ID1.

Absolute Maximum Ratings

Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 7 Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
DC supply voltage	V_D, V_A	–0.5 to +6.0	V
Input current, PCT303A digital input pins	I_{IN}	±10	mA
Digital input voltage	V_{IND}	–0.3 to (V_D+0.3)	V
Operating temperature range	T_A	–10 to +100	°C
Storage temperature range	T_{STG}	–40 to +150	°C

Loop Characteristics

Given values are: V_A = charge pump, V_D = +3.3 V ± 5%; T_A = 0 °C to 70 °C for K-grade, –40 °C to +85 °C for B-grade; refer to Figure 18 on page 34.

Table 8 Loop Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DC termination voltage	V_{DCT}	I_L = 20mA			7.7	V
DC termination voltage	V_{DCT}	I_L = 120mA	12			V
DC ring current	I_{RDC}				720	µA
AC termination impedance	Z_{ACT}			600		Ω
Operating loop current	I_{LP}		8		120	mA
Ring voltage detect	V_{RD}		13	18	26	V_{RMS}
Ring frequency	F_R		15		68	Hz
On-hook leakage current	I_{LK}	V_{BAT} = –48V			1	µA
Ringer equivalence number	REN				1.2	

DC Characteristics

V_D = 5V

Given values are: V_A = +5 V ± 5%; V_D = +3.3 V ± 5%; T_A = 0 °C to 70 °C for K-grade, –40 °C to +85 °C for B-grade.

Table 9 DC Characteristics, V_D = +5V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High-level input voltage	V_{IH}		3.2			V
Low-level input voltage	V_{IL}				0.8	V
High-level output voltage	V_{OH}	I_O = –2mA	2.4			V
Low-level output voltage	V_{OL}	I_O = +2mA			0.4	V
Input leakage current	I_L				±10	µA
Power supply current, analog	I_A	V_A pin		3	6	mA
Power supply current, digital	I_D	V_D pin		13	17	mA
Total supply current, sleep mode					1.5	mA

V_D = 3.3V

Given values are: V_A = charge pump; V_D = +3.3 V ± 5%; T_A = 0 °C to 70 °C for K-grade, –40 °C to +85 °C for B-grade.

Table 10 DC Characteristics, V_D = +3.3V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High-level input voltage	V_{IH}		2.4			V
Low-level input voltage	V_{IL}				0.8	V
High-level output voltage	V_{OH}	I_O = –2mA	2.4			V
Low-level output voltage	V_{OL}	I_O = +2mA			0.35	V
Input leakage current	I_L				±10	µA
Power supply current, analog	I_A	V_A pin		1	6	mA
Power supply current, digital	I_D	V_D pin		8	11	mA
Total supply current, sleep mode					1.5	mA

AC Characteristics

Given values are: V_A = charge pump, V_D = +3.3 V ± 5%; T_A = 0 °C to 70 °C for K-grade, –40 °C to +85 °C for B-grade.

Table 11 AC Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Freq response, transmit [a,b]	F_{RT}	Low –3dB corner		33		Hz
Freq response, transmit [a,b]	F_{RT}	300Hz	–0.2		0	dB
Freq response, transmit [b]	F_{RT}	3400Hz	–0.2		0	dB
Transmit full scale level [c] (0dB gain)	V_{TX}			0.98		V_{peak}
Freq response, receive [a,b]	F_{RR}	Low –3dB corner		33		Hz
Freq response, receive [a,b]	F_{RR}	300Hz	–0.01		0	dB
Freq response, receive [b]	F_{RR}	3400Hz	–0.2		0	dB
Receive full scale level [c,d] (0dB gain)	V_{RX}			0.98		V_{peak}
Dynamic range [e]	DR	VIN = 1kHz, –60dB		84		dB
Total harmonic distortion [f]	THD	VIN = 1kHz, –3dB			–84	dB
Gain drift	AT	VIN = 1kHz		0.002		dB/°C
Dynamic range (call progress AOUT)	DR_{AO}	VIN = 1kHz	60			dB
THD (call progress AOUT)	THD_{AO}	VIN = 1kHz			1.0	%
AOUT full scale level				$0.75V_D$		V_{p-p}
AOUT output impedance				10		kΩ
Mute level (call progress AOUT)			–90			dB
Dynamic range (Caller ID mode)	DR_{CID}	VIN = 1kHz, –60dB		60		dB
Caller ID full scale level (0dB gain) [c]	V_{CID}			0.8		V_{peak}

a. These characteristics are determined by external components.
b. Sample rate = 8 kHz.
c. Parameter measured at Tip and Ring.
d. Receive full scale level produces –0.9dBFS at SDATA_IN.
e. DR = 60dB + 20 log (RMS signal/RMS noise). Applies to both the transmit and receive paths. Measurement bandwidth is 10Hz to 3400Hz. Valid sample rate range is between 7200Hz and 11025Hz.
f. THD = 20 log (RMS distortion/RMS signal). Applies to both the transmit and receive paths. Valid sample rate range is between 7200Hz and 11025Hz.

AC-LINK CHARACTERISTICS

Cold Reset

Given values are: V_A = charge pump, V_D = +3.3V ± 5%; T_A = 25 °C; C_L = 50 pF.

Table 12 Timing Characteristics—Cold Reset

Parameter	Symbol	Min	Typ	Max	Unit
$\overline{\text{RESET}}$ active-low pulse width	t_{rst_low}	1.0			µs
$\overline{\text{RESET}}$ inactive to BIT_CLK startup delay	$t_{rst2clk}$	162.8			ns

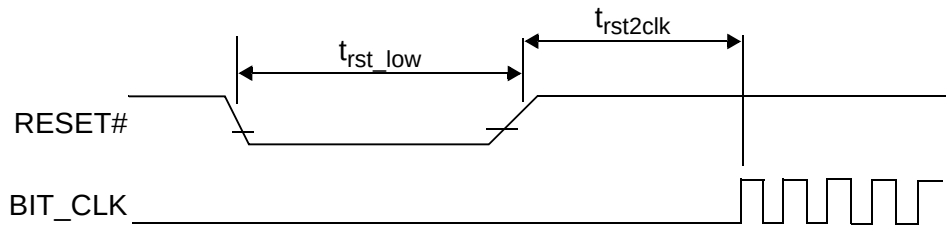


Figure 11 Cold Reset Timing Diagram

Warm Reset

Given values are: V_A = charge pump, V_D = +3.3V ± 5%; T_A = 25 °C; C_L = 50 pF.

Table 13 Timing Characteristics—Warm Reset

Parameter	Symbol	Min	Typ	Max	Unit
SYNC active-high pulse width	t_{sync_high}	1.0			µs
SYNC inactive to BIT_CLK startup delay	$t_{sync2clk}$	162.8			ns

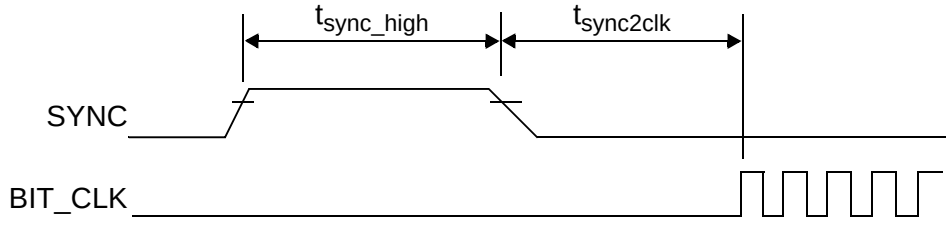


Figure 12 Warm Reset Timing Diagram

Clocks

Given values are: V_A = charge pump, V_D = +3.3V ± 5%; T_A = 25 °C; C_L = 50 pF.

Table 14 Timing Characteristics—Clocks

Parameter	Symbol	Min	Typ	Max	Unit
BIT_CLK frequency			12.288		MHz
BIT_CLK period	t_{clk_period}		81.4		ns
BIT_CLK output jitter				750	ps
BIT_CLK high pulse width [a]	t_{clk_high}	36	40.7	45	ns
BIT_CLK low pulse width [a]	t_{clk_low}	36	40.7	45	ns
SYNC frequency			48.0		kHz
SYNC period	t_{sync_period}		20.8		µs
SYNC high pulse width	t_{sync_high}		1.3		µs
SYNC low pulse width	t_{sync_low}		19.5		µs

a. Worst case duty cycle restricted to 45/55.

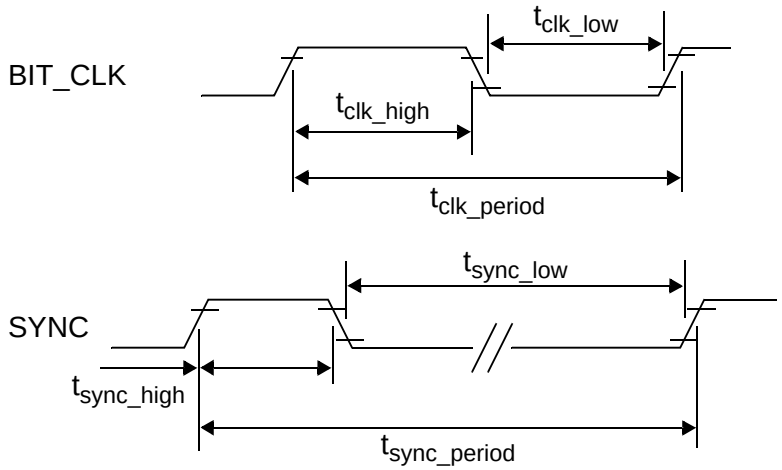


Figure 13 Clocks Timing Diagram

Data Setup and Hold

Given values are: V_A = charge pump, V_D = +3.3V ± 5%; T_A = 25 °C; C_L = 50 pF.

Table 15 Timing Characteristics—Data Setup and Hold

Parameter	Symbol	Min	Typ	Max	Unit
Setup to falling edge of BIT_CLK	t_{setup}	15.0			ns
Hold from falling edge of BIT_CLK	t_{hold}	5.0			ns

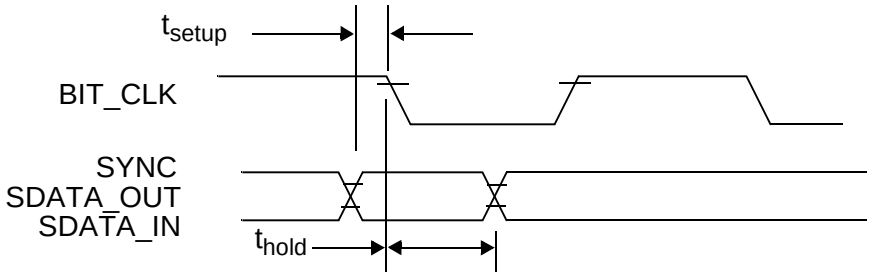


Figure 14 Data Setup and Hold Timing Diagram

Rise and Fall Times

Given values are: V_A = charge pump, V_D = +3.3V ± 5%; T_A = 25 °C; C_L = 50 pF.

Table 16 Timing—Rise and Fall Times

Parameter	Symbol	Min	Typ	Max	Unit
BIT_CLK rise time	$trise_{clk}$	2		6	ns
BIT_CLK fall time	$tfall_{clk}$	2		6	ns
SYNC rise time	$trise_{sync}$	2		6	ns
SYNC fall time	$tfall_{sync}$	2		6	ns
SDATA_IN rise time	$trise_{din}$	2		6	ns
SDATA_IN fall time	$tfall_{din}$	2		6	ns
SDATA_OUT rise time	$trise_{dout}$	2		6	ns
SDATA_OUT fall time	$tfall_{dout}$	2		6	ns

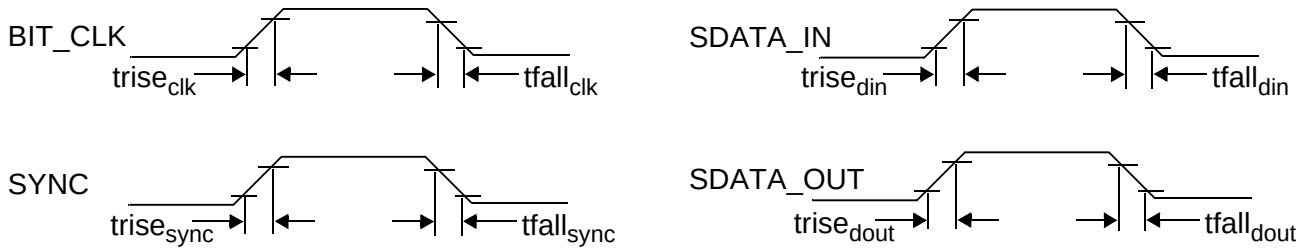


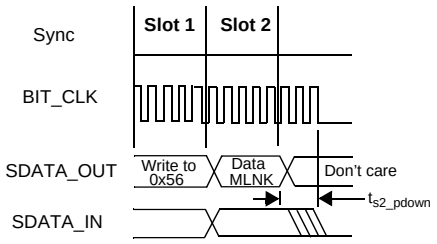
Figure 15 Signal Rise and Fall Timing Diagram

Low Power Mode

Given values are: V_A = charge pump, V_D = +3.3V ± 5%; T_A = 25 °C; C_L = 50 pF.

Table 17 Timing Characteristics—Low Power Mode

Parameter	Symbol	Min	Typ	Max	Unit
End of slot 2 to BIT_CLK, SDATA_IN low	t_{s2_pdown}			1.0	µs



Note: BIT_CLK not to scale

Figure 16 Low Power Mode Timing Diagram

ATE Test Mode

Given values are: V_A = charge pump, V_D = +3.3V ± 5%; T_A = 25 °C; C_L = 50 pF.

Table 18 Timing Characteristics—ATE Test Mode

Parameter [a, b]	Symbol	Min	Typ	Max	Unit
Setup to rising edge of $\overline{\text{RESET}}$ (also applies to SYNC)	$t_{setup2rst}$	15.0			ns
Rising edge of $\overline{\text{RESET}}$ to Hi-Z delay	t_{off}			25.0	ns

a. All AC-link signals are normally low through the trailing edge of $\overline{\text{RESET}}$. Bringing SDATA_OUT high for the trailing edge of RESET causes AC'97 AC-link outputs to go high impedance, which is suitable for ATE in circuit testing.
b. When the test mode has been entered, AC'97 must be issued another $\overline{\text{RESET}}$ with all AC-link signals low to return to the normal operating mode.

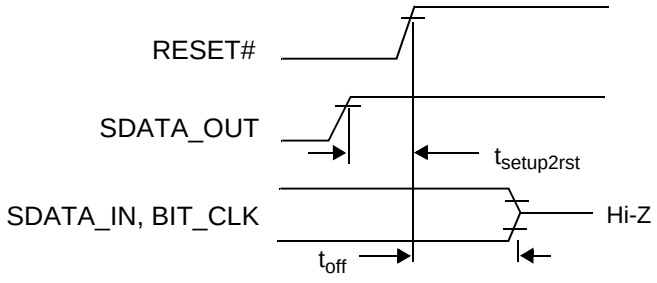


Figure 17 ATE Test Mode Timing Diagram

DIGITAL FILTER CHARACTERISTICS

Digital FIR Filter Characteristics

Given values are: V_A = charge pump, V_D = +3.3 V ± 5%; sample rate = 8 kHz; T_A = 70 °C for K-grade, 85 °C for B-grade.

Typical FIR filter characteristics for Fs = 8000Hz are shown in Figures 19, 20, 21, and 22.

Table 19 Digital FIR Filter Characteristics—Transmit and Receive

Parameter	Symbol	Min	Typ	Max	Unit
Passband (0.1dB)	$F_{(0.1dB)}$	0		3.3	kHz
Passband (3dB)	$F_{(3dB)}$	0		3.6	kHz
Passband ripple peak-to-peak		–0.1		0.1	dB
Stopband			4.4		kHz
Stopband attenuation		–74			dB
Group delay	t_{gd}		12/Fs		sec

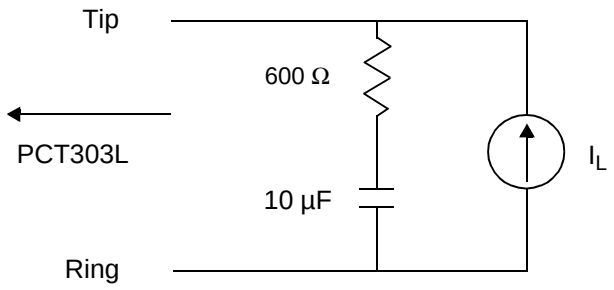
Digital IIR Filter Characteristics

Given values are: V_A = charge pump, V_D = +3.3 V ± 5%; sample rate = 8 kHz; T_A = 70 °C for K-grade, 85 °C for B-grade.

Typical IIR filter characteristics for Fs = 8000 Hz are shown in Figures 23, 24, 25, and 26. Figures 27 and 28 show group delay versus input frequency.

Table 20 Digital IIR Filter Characteristics—Transmit and Receive

Parameter	Symbol	Min	Typ	Max	Unit
Passband (3dB)	$F_{(3dB)}$	0		3.6	kHz
Passband ripple peak-to-peak		–0.2		0.2	dB
Stopband			4.4		kHz
Stopband attenuation		–40			dB
Group delay	t_{gd}		1.6/Fs		sec



Note: The remainder of the circuit is identical to the one shown in the Application Program.

Figure 18 Test Circuit For Loop Characteristics

Filter Plot Diagrams

For Figures 19, 20, 21, and 22, all filter plots apply to a sample rate of Fs = 8 kHz. The filters scale with the sample rate as follows:

$F_{(0.1\ dB)} = 0.4125\ Fs$

$F_{(-3\ dB)} = 0.45\ Fs$

where Fs is the sample frequency.

s

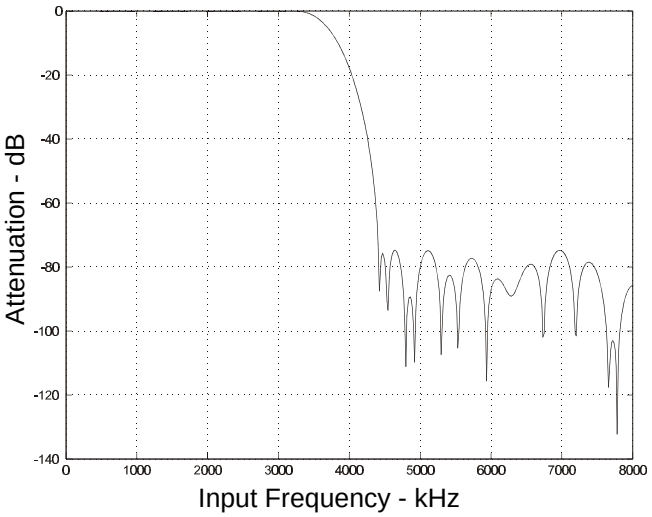


Figure 19 FIR Receive Filter Response

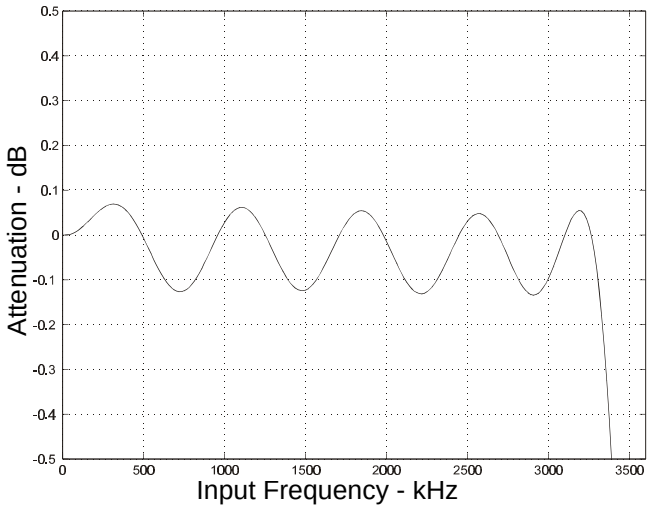


Figure 20 FIR Receive Filter Passband Ripple

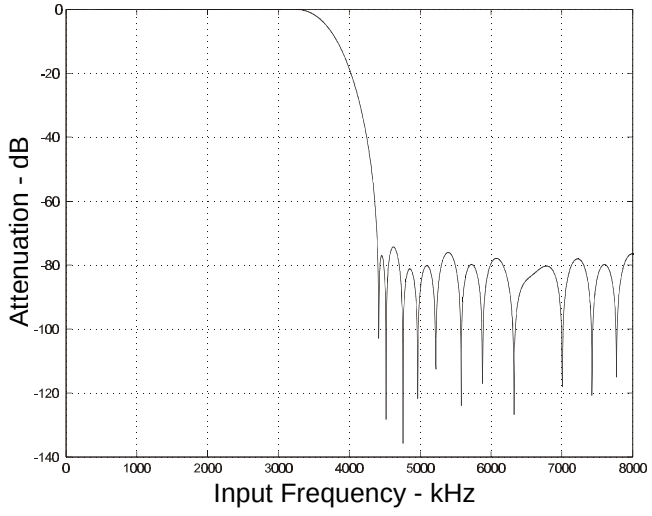


Figure 21 FIR Transmit Filter Response

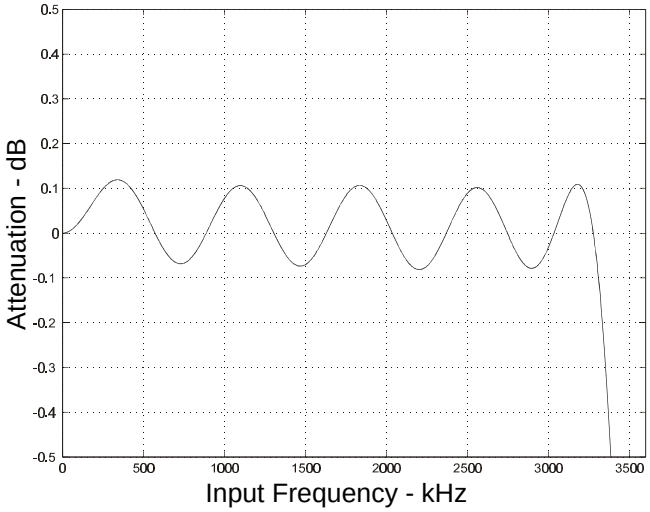


Figure 22 FIR Transmit Filter Passband Ripple

For Figures 23, 24, 25, and 26, all filter plots apply to a sample rate of Fs = 8 kHz. The filters scale with the sample rate as follows:

$F_{(-3\ dB)} = 0.45\ Fs$

where Fs is the sample frequency.

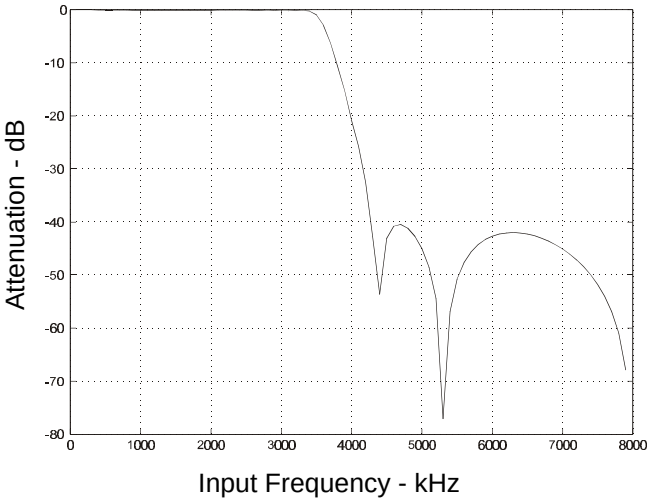


Figure 23 IIR Receive Filter Response

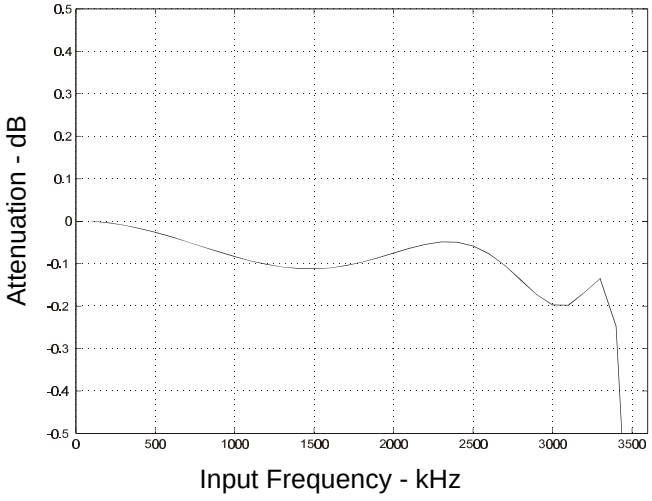


Figure 24 IIR Receive Filter Passband Ripple

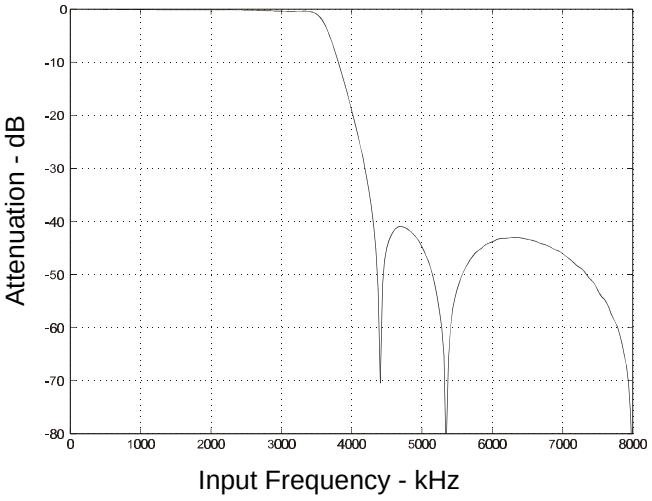


Figure 25 IIR Transmit Filter Response

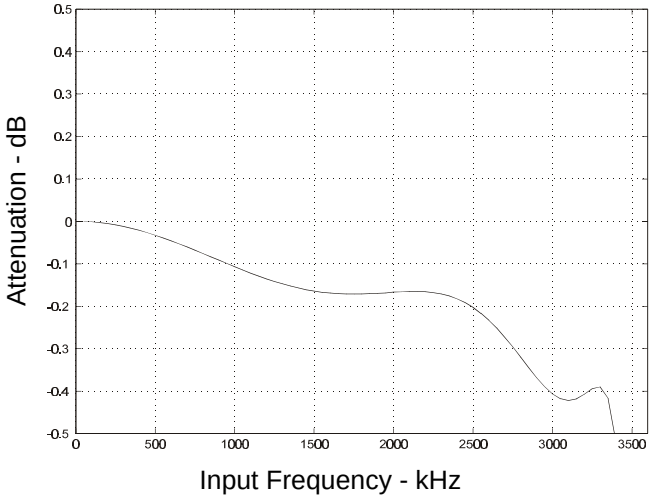


Figure 26 IIR Transmit Filter Passband Ripple

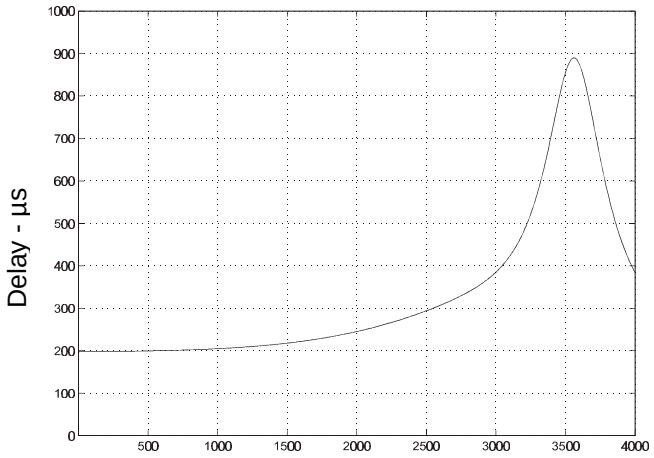


Figure 27 IIR Receive Group Delay

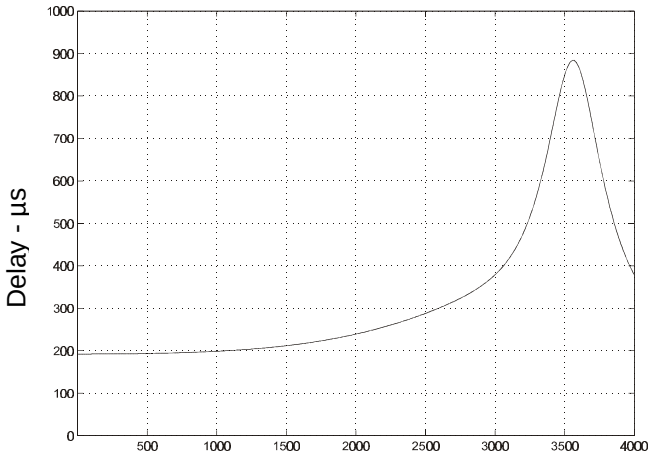


Figure 28 IIR Transmit Group Delay

MECHANICAL DIMENSIONS

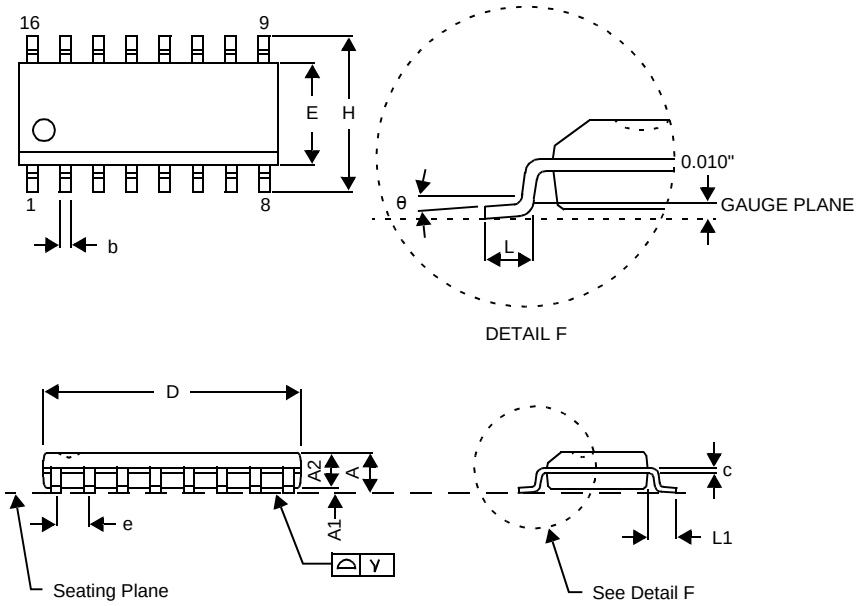


Figure 29 16-pin SOIC Package

Table 21 SOIC Mechanical Dimensions
(Controlling dimension: millimeters)

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
A2	1.30	1.50	0.051	0.059
b	0.330	0.51	0.013	0.020
c	0.19	0.25	0.007	0.010
D	9.80	10.01	0.386	0.394
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
L	0.40	1.27	0.016	0.050
L1	1.07 BSC		0.042 BSC	
g		0.10		0.004
q	0°	8°	0°	8°

MANUFACTURED UNDER ONE OR MORE OF THE FOLLOWING PATENTS:

4,290,139
4,471,489
4,394,767
4,694,450
4,817,147
4,922,534
4,827,431
4,856,031
4,811,360
4,841,561
4,809,300
4,845,735
4,891,823
5,146,472
5,048,056
5,113,412
5,260,971
5,265,151
5,317,594
5,291,520
5,394,440
5,486,825
5,465,273
5,822,371
5,787,305
5,721,830
5,765,021
5,825,816
5,825,823
5,838,724
5,862,184

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ORDERING INFORMATION

Kit P/N	Driver	Parts
K2303N-D-01	V.90/K56Flex	PCT303A, PCT303L
K2303N-V-01	V.90	PCT303A, PCT303L