

LC82293**Image Memory Controller****Preliminary****Overview**

The LC82293 is an image memory controller that supports a wide range of applications such as video printers and video capture systems. It features a simple configuration and low cost.

Features

- Can directly be connected to a YUV422 video bus, so that direct connection to various video decoders and video encoders is possible.
- Has a built-in horizontal sampling rate converter (SCR), so that reduction and enlargement by any factor is possible. (Example: 14.318 MHz → 13.5 MHz, etc.)
- 4Mbits DRAM/16Mbits DRAM directly connectable as image memories
- Built-in memory compression function for storing image data in compressed form in DRAM. NTSC and PAL images can be captured and displayed with an external 4Mbits DRAM. Of course, the memory compression function can be switched ON/OFF.
- Image captured to DRAM can be directly accessed from the CPU. In addition to PIO transfer, DMA transfer is also supported, and high-speed transfer is enabled by built-in FIFO.
- DMA supports both DRQ control mode and WAIT control mode. Connection to various DMA controllers is possible.

- Built-in IrDA 1.0 interface.
- Maximum operating clock of 18 MHz (Example: NTSC: 14.318 MHz, REC601:13.5 MHz)
- Internal supply voltage = 3.3 V, pin supply voltage = 5 V
- SQFP100 package

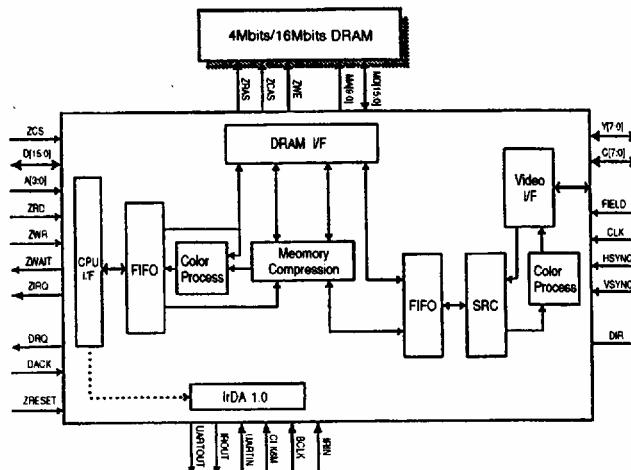
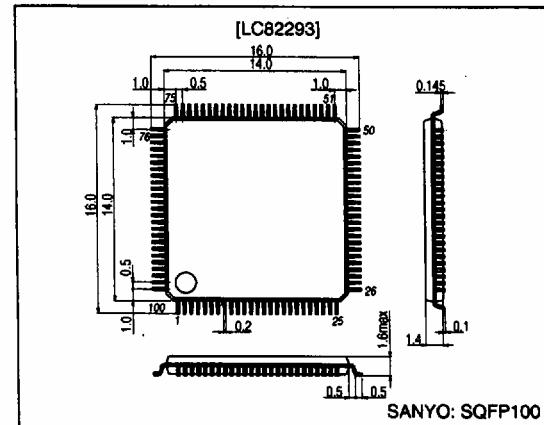
Applications

Video printers, video capture systems, etc.

Package Dimensions

unit: mm

3181B-SQFP100



DC Characteristics**Absolute Maximum Ratings at $V_{SS} = 0$ V**

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage (5 V system)	V_{DD5} max	$T_a = 25^\circ C$	-0.3 to +7.0	V
Maximum supply voltage (3 V system)	V_{DD3} max	$T_a = 25^\circ C$	-0.3 to +4.6	V
Input/output voltage	V_I, V_O	$T_a = 25^\circ C$	-0.3 to $V_{DD} + 0.3$	V
Allowable power dissipation	P_d max	$T_a \leq 70^\circ C$	450	mW
Operating temperature	T_{opr}		-30 to +70	°C
Storage temperature	T_{stg}		-55 to +125	°C
Soldering temperature		10 s	235	°C
Input/output current	I_I, I_O		±20	mA/cell

Allowable Operating Ranges at $T_a = -30$ to $+70^\circ C$, $V_{SS} = 0$ V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage (5 V system)	V_{DD5}		4.5	5.0	5.5	V
Supply voltage (3.3 V system)	V_{DD3}		3.0	3.3	3.6	V
Input voltage range	V_{IN}		0		V_{DD5} (V_{DD3})	V

DC Characteristics at $T_a = -30$ to $+70^\circ C$, $V_{SS} = 0$ V, $V_{DD5} = 4.5$ to 5.5 V

Parameter	Symbol	Conditions	Ratings			Unit	Applicable pins
			min	typ	max		
High-level input voltage	V_{IH}	TTL levels	2.0			V	(1)
Low-level input voltage	V_{IL}				0.5	V	
High-level input voltage	V_{IH}	TTL levels Schmitt	2.4			V	(2)
Low-level input voltage	V_{IL}				0.3	V	
High-level input voltage	V_{IH}	CMOS levels	0.7 V_{DD5}			V	(3)
Low-level input voltage	V_{IL}				0.2 V_{DD5}	V	
High-level output voltage	V_{OH}	$I_{OH} = -2$ mA	$V_{DD5} - 0.8$			V	(4) (7) (8) (9)
Low-level output voltage	V_{OL}	$I_{OL} = 2$ mA			0.4	V	
High-level output voltage	V_{OH}	$I_{OH} = -4$ mA	$V_{DD5} - 0.8$			V	(5)
Low-level output voltage	V_{OL}	$I_{OL} = 4$ mA			0.4	V	
High-level output voltage	V_{OH}	$I_{OH} = -8$ mA	$V_{DD5} - 0.8$			V	(6)
Low-level output voltage	V_{OL}	$I_{OL} = 8$ mA			0.4	V	
Input leak current	I_{IL}	$V_I = V_{DD}, V_{SS}$	-10		+10	µA	(1) (2) (3) (9)
Output leak current	I_{OZ}	During high-impedance output	-10		+10	µA	(7) (9)
Pull-up resistance	R_{UP}		70	140	280	kΩ	(8)

The applicable pin sets are as follows.

(1: TTL input) A3[3:0], FIELD, VSYNC, HSYNC, UARTIN, CLK6M, BCLK, IRIN

(2: TTL Schmitt input) ZCS, DACK, ZHRESET, ZRD, ZWR

(3: CMOS input) CLK

(4: Output 2 mA drive) MA[9:0], DRQ, IRQ, DIR, UAROUT, IROUT

(5: Output 4 mA drive) ZWE

(6: Output 8 mA drive) ZRAS, ZCAS

(7: 3-state output 2 mA drive) ZWAIT

(8: Pull-up resistor built-in, bidirectional 2 mA drive) Y[7:0], C[7:0], MD[15:0]

(9: Bidirectional 2 mA drive) D[15:0]