

Features

- This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- 0MHz to 25.6MHz Sample Rate
- Eight Filter Cells
- 8-Bit Coefficients and Signal Data
- Low Power CMOS Operation
 - I_{CCSB} 500 μ A Maximum
 - I_{CCOP} 160mA Maximum at 20MHz
- 26-Bit Accumulator Per Stage
- Filter Lengths Up to 1032 Taps
- Expandable Coefficient Size, Data Size and Filter Length
- Decimation by 2, 3 or 4

Applications

- 1-D and 2-D FIR Filters
- Radar/Sonar
- Adaptive Filters
- Echo Cancellation
- Complex Multiply-Add
- Sample Rate Converters

Description

The HSP43881/883 is a video speed Digital Filter (DF) designed to efficiently implement vector operations such as FIR digital filters. It is comprised of eight filter cells cascaded internally and a shift and add output stage, all in a single integrated circuit. Each filter cell contains a 8 x 8-bit multiplier, three decimation registers and a 26-bit accumulator. The output stage contains an additional 26-bit accumulator which can add the contents of any filter cell accumulator to the output stage accumulator shifted right by 8-bits. The HSP43881/883 has a maximum sample rate of 25.6MHz. The effective multiply accumulate (mac) rate is 204MHz.

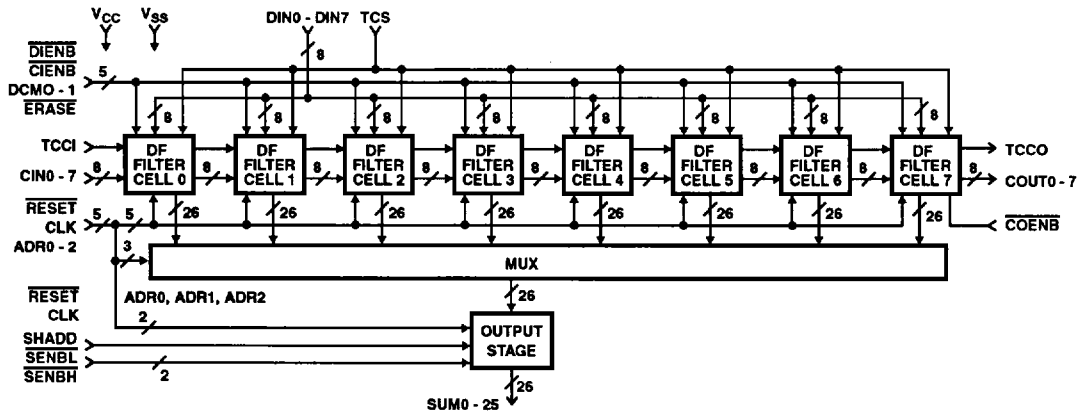
The HSP43881/883 DF can be configured to process expanded coefficient and word sizes. Multiple DFs can be cascaded for larger filter lengths without degrading the sample rate or a single DF can process larger filter lengths at less than 25.6MHz with multiple passes. The architecture permits processing filter lengths of over 1000 taps with the guarantee of no overflows. In practice, most filter coefficients are less than 1.0, making even larger filter lengths possible. The DF provides for 8-bit unsigned or two's complement arithmetic, independently selectable for coefficients and signal data.

Each DF filter cell contains three resampling or decimation registers which permit output sample rate reduction at rates of $1/2$, $1/3$ or $1/4$ the input sample rate. These registers also provide the capability to perform 2-D operations such as matrix multiplication and N x N spatial correlations/convolutions for image processing applications.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HSP43881GM-20/883	-55°C to +125°C	85 Lead PGA
HSP43881GM-25/883	-55°C to +125°C	85 Lead PGA

Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.
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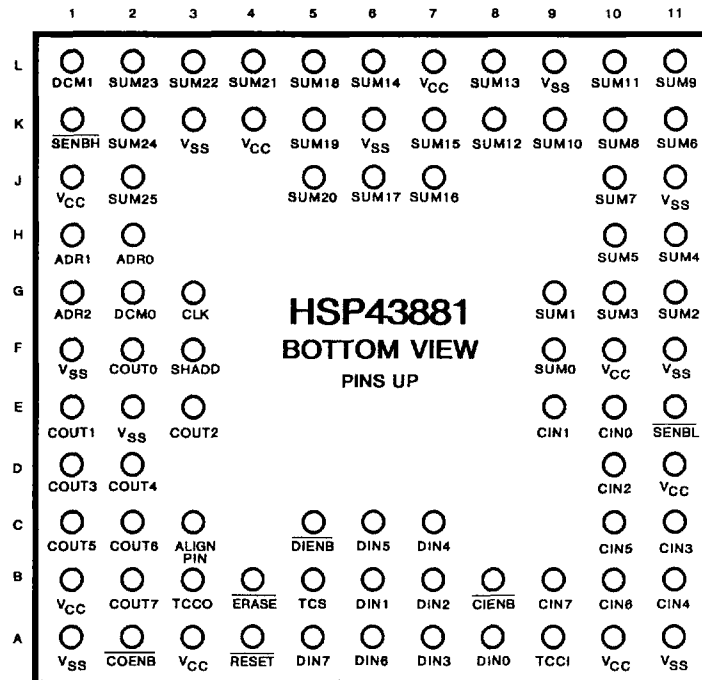
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HSP43881/883

Pinouts

85 PIN GRID ARRAY (PGA)

	1	2	3	4	5	6	7	8	9	10	11						
A	V _{SS}	$\overline{\text{COENB}}$	V _{CC}	$\overline{\text{RESET}}$	DIN7	DIN6	DIN3	DIN0	TCCI	V _{CC}	V _{SS}						
B	V _{CC}	COUT7	TCCO	$\overline{\text{ERASE}}$	TCS	DIN1	DIN2	$\overline{\text{CIENB}}$	CIN7	CIN6	CIN4						
C	COUT5	COUT6	ALIGN PIN		$\overline{\text{DIENB}}$	DIN5	DIN4			CIN5	CIN3						
D	COUT3	COUT4		HSP43881/883 TOP VIEW PINS DOWN							CIN2	V _{CC}					
E	COUT1	V _{SS}	COUT2												CIN1	CIN0	$\overline{\text{SENBL}}$
F	V _{SS}	COUT0	SHADD												SUM0	V _{CC}	V _{SS}
G	ADR2	DCM0	CLK												SUM1	SUM3	SUM2
H	ADR1	ADR0								SUM5	SUM4						
J	V _{CC}	SUM25			SUM20	SUM17	SUM16			SUM7	V _{SS}						
K	$\overline{\text{SENBH}}$	SUM24	V _{SS}	V _{CC}	SUM19	V _{SS}	SUM15	SUM12	SUM10	SUM8	SUM6						
L	DCM1	SUM23	SUM22	SUM21	SUM18	SUM14	V _{CC}	SUM13	V _{SS}	SUM11	SUM9						



Note: An overbar on a signal name represents an active LOW signal.

Specifications HSP43881/883

Absolute Maximum Ratings

Supply Voltage +8.0V
 Input, Output Voltage Applied GND-0.5V to V_{CC}+0.5V
 Storage Temperature Range -65°C to +150°C
 Junction Temperature +175°C
 Lead Temperature (Soldering, Ten Seconds) +300°C
 ESD Classification Class 1

Reliability Information

Thermal Resistance θ_{ja} θ_{jc}
 Ceramic PGA Package 34.66°C/W 7.78°C/W
 Maximum Package Power Dissipation at +125°C
 Ceramic PGA Package 1.44 Watt
 Gate Count 17762 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range +4.5V to +5.5V
 Operating Temperature Range -55°C to +125°C

TABLE 1. HSP43881/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Devices Guaranteed and 100% Tested

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Logical One Input Voltage	V _{IH}	V _{CC} = 5.5V	1, 2, 3	-55°C ≤ T _A ≤ +125°C	2.2	-	V
Logical Zero Input Voltage	V _{IL}	V _{CC} = 4.5V	1, 2, 3	-55°C ≤ T _A ≤ +125°C	-	0.8	V
Output HIGH Voltage	V _{OH}	I _{OH} = -400µA V _{CC} = 4.5V (Note 1)	1, 2, 3	-55°C ≤ T _A ≤ +125°C	2.6	-	V
Output LOW Voltage	V _{OL}	I _{OL} = +2.0mA V _{CC} = 4.5V (Note 1)	1, 2, 3	-55°C ≤ T _A ≤ +125°C	-	0.4	V
Input Leakage Current	I _I	V _{IN} = V _{CC} or GND V _{CC} = 5.5V	1, 2, 3	-55°C ≤ T _A ≤ +125°C	-10	+10	µA
Output Leakage Current	I _O	V _{OUT} = V _{CC} or GND V _{CC} = 5.5V	1, 2, 3	-55°C ≤ T _A ≤ +125°C	-10	+10	µA
Clock Input High	V _{IHC}	V _{CC} = 5.5V	1, 2, 3	-55°C ≤ T _A ≤ +125°C	3.0	-	V
Clock Input Low	V _{ILC}	V _{CC} = 4.5V	1, 2, 3	-55°C ≤ T _A ≤ +125°C	-	0.8	V
Standby Power Supply Current	I _{CCSB}	V _{IN} = V _{CC} or GND V _{CC} = 5.5V, Outputs Open	1, 2, 3	-55°C ≤ T _A ≤ +125°C	-	500	µA
Operating Power Supply Current	I _{CCOP}	f = 20.0MHz V _{CC} = 5.5V (Note 2)	1, 2, 3	-55°C ≤ T _A ≤ +125°C	-	160.0	mA
Functional Test	FT	(Note 3)	7, 8	-55°C ≤ T _A ≤ +125°C	-	-	

NOTES:

- Interchanging of force and sense conditions is permitted.
- Operating Supply Current is proportional to frequency, typical rating is 8.0mA/MHz.
- Tested as follows: f = 1MHz, V_{IH} = 2.6, V_{IL} = 0.4, V_{OH} ≥ 1.5V, V_{OL} ≤ 1.5V, V_{IHC} = 3.4V, and V_{ILC} = 0.4V.

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1D FILTERS

Specifications HSP43881/883

TABLE 2. HSP43881/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	-20 (20MHz)		-25 (25.6MHz)		UNITS
					MIN	MAX	MIN	MAX	
Clock Period	T _{CP}	Note 1	9, 10, 11	-55°C ≤ T _A ≤ +125°C	50	-	39	-	ns
Clock Low	T _{CL}	Note 1	9, 10, 11	-55°C ≤ T _A ≤ +125°C	20	-	16	-	ns
Clock High	T _{CH}	Note 1	9, 10, 11	-55°C ≤ T _A ≤ +125°C	20	-	16	-	ns
Input Setup	T _{IS}	Note 1	9, 10, 11	-55°C ≤ T _A ≤ +125°C	20	-	17	-	ns
Input Hold	T _{IH}	Note 1	9, 10, 11	-55°C ≤ T _A ≤ +125°C	0	-	0	-	ns
CLK to Coefficient Output Delay	T _{ODC}	Note 1	9, 10, 11	-55°C ≤ T _A ≤ +125°C	-	24	-	20	ns
Output Enable Delay	T _{OED}	Note 1	9, 10, 11	-55°C ≤ T _A ≤ +125°C	-	20	-	15	ns
CLK to SUM Output Delay	T _{ODS}	Note 1	9, 10, 11	-55°C ≤ T _A ≤ +125°C	-	31	-	25	ns

NOTE: 1. A.C. Testing: V_{CC} = 4.5V and 5.5V. Inputs are driven at 3.0V for a Logic "1" and 0.0V for a Logic "0". Input and output timing measurements are made at 1.5V for both a Logic "1" and "0". CLK is driven at 4.0V and 0V and measured at 2.0V.

TABLE 3. HSP43881/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	-20		-25		UNITS
					MIN	MAX	MIN	MAX	
Input Capacitance	C _{IN}	V _{CC} =Open, f=1MHz All measurements are referenced to device GND.	1	T _A = +25°C	-	15	-	15	pF
Output Capacitance	C _{OUT}		1	T _A = +25°C	-	15	-	15	pF
Output Disable Delay	T _{ODD}		1, 2	-55°C ≤ T _A ≤ +125°C	-	20	-	15	ns
Output Rise Time	T _{OR}		1, 2	-55°C ≤ T _A ≤ +125°C	-	7	-	6	ns
Output Fall Time	T _{OF}		1, 2	-55°C ≤ T _A ≤ +125°C	-	7	-	6	ns

NOTES:

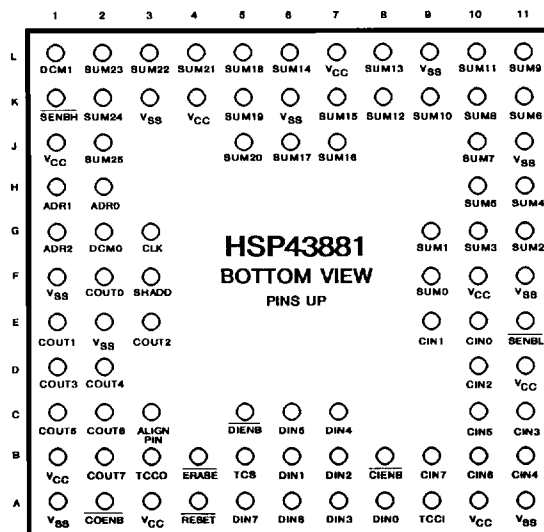
1. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.
2. Loading is as specified in the test load circuit, C_L = 40pF.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	-
PDA	100%	1
Final Test	100%	2, 3, 8A, 8B, 10, 11
Group A	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

Burn-In Circuit

HSP43881/883 PIN GRID ARRAY (PGA)



PGA PIN	PIN NAME	BURN-IN SIGNAL	PGA PIN	PIN NAME	BURN-IN SIGNAL	PGA PIN	PIN NAME	BURN-IN SIGNAL	PGA PIN	PIN NAME	BURN-IN SIGNAL
A1	VSS	GND	C1	COU5	VCC/2	F10	VCC	VCC	K4	VCC	VCC
A2	COENB	F10	C2	COU6	VCC/2	F11	VSS	GND	K5	SUM19	VCC/2
A3	VCC	VCC	C3	ALIGN	NC	G1	ADR2	F2	K6	VSS	GND
A4	RESET	F11	C5	DIENB	F10	G2	DCM0	F5	K7	SUM15	VCC/2
A5	DIN7	F8	C6	DIN5	F5	G3	CLK	F0	K8	SUM12	VCC/2
A6	DIN6	F6	C7	DIN4	F4	G9	SUM1	VCC/2	K9	SUM10	VCC/2
A7	DIN3	F3	C10	CIN5	F5	G10	SUM3	VCC/2	K10	SUM8	VCC/2
A8	DIN0	F0	C11	CIN3	F3	G11	SUM2	VCC/2	K11	SUM6	VCC/2
A9	CIN8/TCCI	F8	D1	COU3	VCC/2	H1	ADR1	F1	L1	DCM1	F6
A10	VCC	VCC	D2	COU4	VCC/2	H2	ADR0	F0	L2	SUM23	VCC/2
A11	VSS	GND	D10	CIN2	F2	H10	SUM5	VCC/2	L3	SUM22	VCC/2
B1	VCC	VCC	D11	VCC	VCC	H11	SUM4	VCC/2	L4	SUM21	VCC/2
B2	COU7	VCC/2	E1	COU1	VCC/2	J1	VCC	VCC	L5	SUM18	VCC/2
B3	COU8/TCC0	VCC/2	E2	VSS	GND	J2	SUM25	VCC/2	L6	SUM14	VCC/2
B4	ERASE	F10	E3	COU2	VCC/2	J5	SUM20	VCC/2	L7	VCC	VCC
B5	DIN8/TCS	F7	E9	CIN1	F1	J6	SUM17	VCC/2	L8	SUM13	VCC/2
B6	DIN1	F1	E10	CIN0	F0	J7	SUM16	VCC/2	L9	VSS	GND
B7	DIN2	F2	E11	SENB	F10	J10	SUM7	VCC/2	L10	SUM11	VCC/2
B8	CIENB	F10	F1	VSS	GND	J11	VSS	GND	L11	SUM9	VCC/2
B9	CIN7	F7	F2	COU0	VCC/2	K1	SENBH	F10			
B10	CIN6	F6	F3	SHADD	F9	K2	SUM24	VCC/2			
B11	CIN4	F4	F9	SUM0	VCC/2	K3	VSS	GND			

NOTES:

- VCC/2 (2.7V ± 10%) used for outputs only.
- 47KΩ (±20%) resistor connected to all pins except VCC and GND.
- VCC = 5.5V ± 0.5V.
- 0.1µF (min) capacitor between VCC and GND per device.
- F0 = 100kHz ± 10%, F1 = F0/2, F2 = F1/2, ..., F11 = F10/2, 40% - 60% Duty Cycle.
- Input voltage Limits: V_{IL} = 0.8V Max, V_{IH} = 4.5V ± 10%

Die Characteristics

DIE DIMENSIONS:

328 x 283 x 19 ±1 mils

METALLIZATION:

Type: Si-Al or Si-Al-Cu
 Thickness: 8kÅ

GLASSIVATION:

Type: Nitrox
 Thickness: 10kÅ

WORST CASE CURRENT DENSITY: 1.2 x 10⁵A/cm²

Metallization Mask Layout

HSP43881/883

