DDR3 SDRAM
Unbuffered SODIMMs
Based on 1Gb A version

HMT164S6AFP(R)6C
HMT112S6AFP(R)6C
HMT125S6AFP(R)8C

** Contents are subject to change without prior notice.

Revision History

Revision No.	History	Draft Date	Remark
0.01	Initial draft	Sep. 2007	preliminary
0.02	Added IDD, corrected typos	Mar. 2008	preliminary
0.03	Halogen-free added	May. 2008	preliminary
0.1	Initial Specification Release	May 2008	
0.2	Added outline: DIMMs with thermal sensor, corrected typos	Jul. 2008	

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1. Description

This Hynix unbuffered Small Outline Dual In-Line Memory Module(SODIMM) series consists of 1Gb A version. DDR3 SDRAMs in Fine Ball Grid Array(FBGA) packages on a 204 pin glass-epoxy substrate. This DDR3 Unbuffered SODIMM series based on 1Gb A version provide a high performance 8 byte interface in 67.60mm width form factor of industry standard. It is suitble for easy interchange and addition.

1.1 Device Features & Ordering Information

1.1.1 Features

- VDD=VDDQ=1.5V
- VDDSPD=3.0V to 3.6V
- Fully differential clock inputs (CK, /CK) operation
- Differential Data Strobe (DQS, /DQS)
- On chip DLL align DQ, DQS and /DQS transition with CK transition
- DM masks write data-in at the both rising and falling edges of the data strobe
- All addresses and control inputs except data, data strobes and data masks latched on the rising edges of the clock
- Programmable CAS latency 5, 6, 7, 8, 9, 10, and (11) supported
- Programmable additive latency 0, CL-1 and CL-2 supported
- Programmable CAS Write latency (CWL) = 5, 6, 7, 8
- Programmable burst length 4/8 with both nibble sequential and interleave mode
- BL switch on the fly
- 8 banks
- 8K refresh cycles /64ms
- DDR3 SDRAM Package : JEDEC standard 82ball FBGA(x4/x8) , 100ball FBGA(x16) with support balls
- Driver strength selected by EMRS
- Dynamic On Die Termination supported
- Asynchronous RESET pin supported
- ZQ calibration supported
- TDQS (Termination Data Strobe) supported (x8 only)
- Write Levelization supported
- Auto Self Refresh supported
- 8 bit pre-fetch

1.1.2 Ordering Information

Part Name	Density	Organization	# of DRAMs	# of ranks	Materials
HMT164S6AFP6C-S6/S5/G8/G7/H9/H8	512MB	64Mx64	4	1	Lead free
HMT164S6AFR6C-S6/S5/G8/G7/H9/H8	512MB	64Mx64	4	1	Halogen free
HMT112S6AFP6C-S6/S5/G8/G7/H9/H8	1GB	128Mx64	8	2	Lead free
HMT112S6AFR6C-S6/S5/G8/G7/H9/H8	1GB	128Mx64	8	2	Halogen free
HMT125S6AFP8C-S6/S5/G8/G7/H9/H8	2GB	256Mx64	16	2	Lead free
HMT125S6AFR8C-S6/S5/G8/G7/H9/H8	2GB	256Mx64	16	2	Halogen free

Two types, with integrated thermal sensor and with no thermal sensor, exist, in each configuration.

1.2 Speed Grade & Key Parameters

MT/S	DDR3-800		DDR3-1066		DDR3-1333		Unit
Grade	-S6	-S5	-G8	-G7	-H9	-H8	
tCK(min)	2.5		1.875		1.5		ns
CAS Latency	6	5	8	7	9	8	tCK
tRCD(min)	15	12.5	15	13.125	13.5	12	ns
tRP(min)	15	12.5	15	13.125	13.5	12	ns
tRAS(min)	37.5	37.5	37.5	37.5	36	36	ns
tRC(min)	52.5	50	52.5	50.625	49.5	48	ns
CL-tRCD-tRP	6-6-6	5-5-5	8-8-8	7-7-7	9-9-9	8-8-8	tCK

1.3 Address Table

	512MB	1GB	2GB
Organization	64M x 64	128M x 64	256M x 64
Refresh Method	8K/64ms	8K/64ms	8K/64ms
Row Address	A0-A12	A0-A12	A0-A13
Column Address	A0-A9	A0-A9	A0-A9
Bank Address	BA0-BA2	BA0-BA2	BA0-BA2
Page Size	2KB	2KB	1KB
# of Rank	1	2	2
# of Device	4	8	16

2. Pin Architecture

2.1 Pin Definition

Pin Name	Description		Pin Name	Description	
CK[1:0]	Clock Inputs, positive line	2	DQ[63:0]	Data Input/Output	64
$\overline{CK}$[1:0]	Clock Inputs, negative line	2	DM[7:0]	Data Masks	8
CKE[1:0]	Clock Enables	2	DQS[7:0]	Data strobes	8
$\overline{RAS}$	Row Address Strobe	1	$\overline{DQS}$[7:0]	Data strobes complement	8
$\overline{CAS}$	Column Address Strobe	1	$\overline{RESET}$	Reset pin	1
$\overline{WE}$	Write Enable	1	TEST	Logic Analyzer specific test pin (No connect on SODIMM)	1
$\overline{S}$[1:0]	Chip Selects	2	$\overline{EVENT}$	Temeprature event pin	1
A[9:0], A11, A[15:13]	Address Inputs	14	V_{DD}	Core and I/O power	18
A10/AP	Address Input/Autoprecharge	1	V_{SS}	Ground	52
A12/$\overline{BC}$	Address Input/Burst Stop	1	V_{REF}DQ	Input/Output Reference	2
BA[2:0]	SDRAM Bank Address	3	V_{REF}CA		
$\overline{ODT}$[1:0]	On-die termination control	2	V_{DD}SPD	SPD and Temp sensor power	1
SCL	Serial Presence Detect(SPD) Clock input	1	Vtt	Termination voltage	2
SDA	SPD Data Input/Output	1	NC	Reserved for future use	2
$\overline{SA}$[1:0]	SPD address	2		Total	204

2.2 Input/Output Functional Description

Symbol	Type	Polarity	Function
CK0/$\overline{CK}$0 CK1/$\overline{CK}$1	Input	Cross point	The system clock inputs. All address and command lines are sampled on the cross point of the rising edge of CK and falling edge of $\overline{CK}$. A Delay Locked Loop (DLL) circuit is driven from the clock inputs and output timing for read operations is synchronized to the input clock.
CKE[1:0]	Input	Active High	Activates the DDR3 SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode or the Self Refresh mode.
$\overline{S}$[1:0]	Input	Active Low	Enables the associated DDR3 SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. Rank 0 is selected by $\overline{S}$0; Rank 1 is selected by $\overline{S}$1.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	Active Low	When sampled at the cross point of the rising edge of CK and falling edge of $\overline{CK}$, signals $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ define the operation to be executed by the SDRAM.
BA[2:0]	Input	-	Selects which DDR3 SDRAM internal bank of eight is activated.
ODT[1:0]	Input	Active High	Asserts on-die termination for DQ, DM, DQS, and $\overline{DQS}$ signals if enabled via the DDR3 SDRAM mode register.
A[9:0], A10/$\overline{AP}$, A11, A12/$\overline{BC}$, A[15:13]	Input	-	During a Bank Activate command cycle, defines the row address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{CK}$. During a Read or Write command cycle, defines the column address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{CK}$. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0-BAn defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0-BAn to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0-BAn inputs. If AP is low, then BA0-BAn are used to define which bank to precharge. A12($\overline{BC}$) is sampled during READ and WRITE commands to determine if burst chop (on-thefly) will be performed (HIGH, no burst chop; LOW, burst chopped)
DQ[63:0]	In/Out	-	Data Input/Output pins.
DM[7:0]	Input	Active High	The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if it is high. In Read mode, DM lines have no effect.
DQS[7:0], $\overline{DQS}$[7:0]	In/Out	Cross Point	The data strobes, associated with one data byte, sourced with data transfers. In Write mode, the data strobe is sourced by the controller and is centered in the data window. In Read mode, the data strobe is sourced by the DDR3 SDRAMs and is sent at the leading edge of the data window. $\overline{DQS}$ signals are complements, and timing is relative to the crosspoint of respective DQS and $\overline{DQS}$.

Symbol	Type	Polarity	Function
V_{DD},V_{DD}SPD, V_{SS},	Supply		Power supplies for core, I/O, Serial Presence Detect, Temp sensor, and ground for the module.
V_{REF}DQ, V_{REF}CA	Supply		Reference voltage for SSTL15 inputs.
SDA	In/Out		This is a bidirectional pin used to transfer data into or out of the SPD EEPROM and Temp sensor. A resistor must be connected from the SDA bus line to V_{DD}SPD on the system planar to act as a pull up.
SCL	Input		This signal is used to clock data into and out of the SPD EEPROM and Temp sensor.
SA[1:0]	Input		Address pins used to select the Serial Presence Detect and Temp sensor base address.
TEST	In/Out		The TEST pin is reserved for bus analysis tools and is not connected on normal memory modules (SO-DIMMs).
$\overline{\text{EVENT}}$	Wire OR Out	Active Low	The EVENT pin is reserved for use to flag critical module temperature. A resistor may be connected from EVENT bus line to VDDSPD on the system planar to act as a pullup.
$\overline{\text{RESET}}$	In	Active Low	This signal resets the DDR3 SDRAM

2.3 Pin Assignment

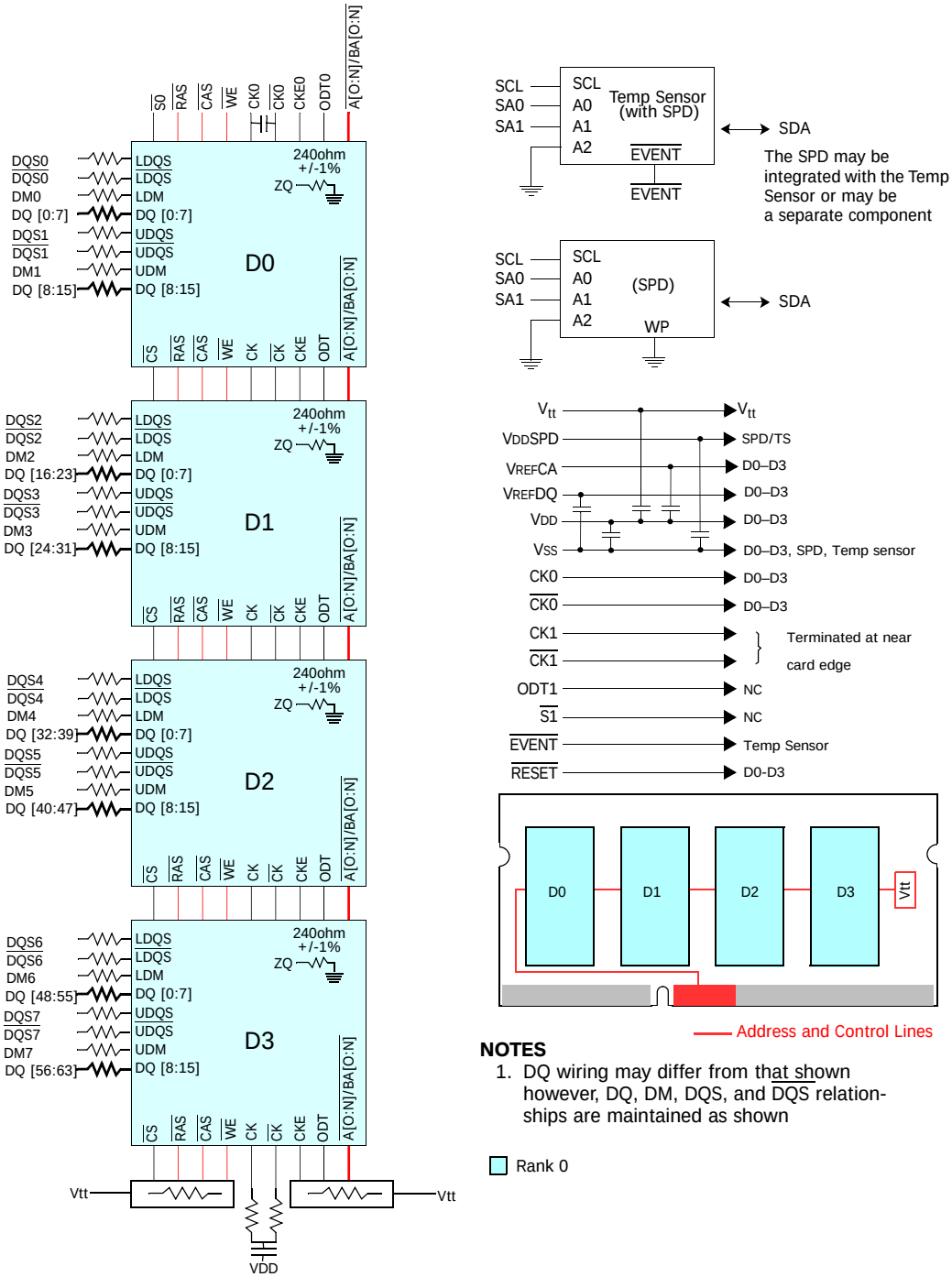
Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Sid	Pin #	Back Side
1	$V_{REF}DQ$	2	V_{SS}	53	DQ19	54	V_{SS}	105	V_{DD}	106	V_{DD}	157	DQ42	158	DQ46
3	V_{SS}	4	DQ4	55	V_{SS}	56	DQ28	107	A10/AP	108	BA1	159	DQ43	160	DQ47
5	DQ0	6	DQ5	57	DQ24	58	DQ29	109	BA0	110	$\overline{RAS}$	161	V_{SS}	162	V_{SS}
7	DQ1	8	V_{SS}	59	DQ25	60	V_{SS}	111	V_{DD}	112	V_{DD}	163	DQ48	164	DQ52
9	V_{SS}	10	$\overline{DQS0}$	61	V_{SS}	62	$\overline{DQS3}$	113	$\overline{WE}$	114	$\overline{S0}$	165	DQ49	166	DQ53
11	DM0	12	DQS0	63	DM3	64	DQS3	115	$\overline{CAS}$	116	ODT0	167	V_{SS}	168	V_{SS}
13	V_{SS}	14	V_{SS}	65	V_{SS}	66	V_{SS}	117	V_{DD}	118	V_{DD}	169	$\overline{DQS6}$	170	DM6
15	DQ2	16	DQ6	67	DQ26	68	DQ30	119	A13[2]	120	ODT1	171	DQS6	172	V_{SS}
17	DQ3	18	DQ7	69	DQ27	70	DQ31	121	$\overline{S1}$	122	NC	173	V_{SS}	174	DQ54
19	V_{SS}	20	V_{SS}	71	V_{SS}	72	V_{SS}	123	V_{DD}	124	V_{DD}	175	DQ50	176	DQ55
21	DQ8	22	DQ12	73	CKE0	74	CKE1	125	TEST	126	$V_{REF}CA$	177	DQ51	178	V_{SS}
23	DQ9	24	DQ13	75	V_{DD}	76	V_{DD}	127	V_{SS}	128	V_{SS}	179	V_{SS}	180	DQ60
25	V_{SS}	26	V_{SS}	77	NC	78	A15[2]	129	DQ32	130	DQ36	181	DQ56	182	DQ61
27	$\overline{DQS1}$	28	DM1	79	BA2	80	A14[2]	131	DQ33	132	DQ37	183	DQ57	184	V_{SS}
29	DQS1	30	$\overline{RESET}$	81	V_{DD}	82	V_{DD}	133	V_{SS}	134	V_{SS}	185	V_{SS}	186	$\overline{DQS7}$
31	V_{SS}	32	V_{SS}	83	A12/$\overline{BC}$	84	A11	135	$\overline{DQS4}$	136	DM4	187	DM7	188	DQS7
33	DQ10	34	DQ14	85	A9	86	A7	137	DQS4	138	V_{SS}	189	V_{SS}	190	V_{SS}
35	DQ11	36	DQ15	87	V_{DD}	88	V_{DD}	139	V_{SS}	140	DQ38	191	DQ58	192	DQ62
37	V_{SS}	38	V_{SS}	89	A8	90	A6	141	DQ34	142	DQ39	193	DQ59	194	DQ63
39	DQ16	40	DQ20	91	A5	92	A4	143	DQ35	144	V_{SS}	195	V_{SS}	196	V_{SS}
41	DQ17	42	DQ21	93	V_{DD}	94	V_{DD}	145	V_{SS}	146	DQ44	197	SA0	198	$\overline{EVENT}$
43	V_{SS}	44	V_{SS}	95	A3	96	A2	147	DQ40	148	DQ45	199	VDD_{SPD}	200	SDA
45	$\overline{DQS2}$	46	DM2	97	A1	98	A0	149	DQ41	150	V_{SS}	201	SA1	202	SCL
47	DQS2	48	V_{SS}	99	V_{DD}	100	V_{DD}	151	V_{SS}	152	$\overline{DQS5}$	203	V_{TT}	204	V_{TT}
49	V_{SS}	50	DQ22	101	CK0	102	CK1	153	DM5	154	DQS5				
51	DQ18	52	DQ23	103	$\overline{CK0}$	104	$\overline{CK1}$	155	V_{SS}	156	V_{SS}				

NC = No Connect; RFU = Reserved Future Use

1. TEST(pin 125) is reserved for bus analysis probes and is NC on normal memory modules.
2. This address might be connected to NC balls of the DRAMs (depending on density); either way they will be connected to the termination resistor.

3. Functional Block Diagram

3.1 512MB, 64Mx64 Module(1Rank of x16)

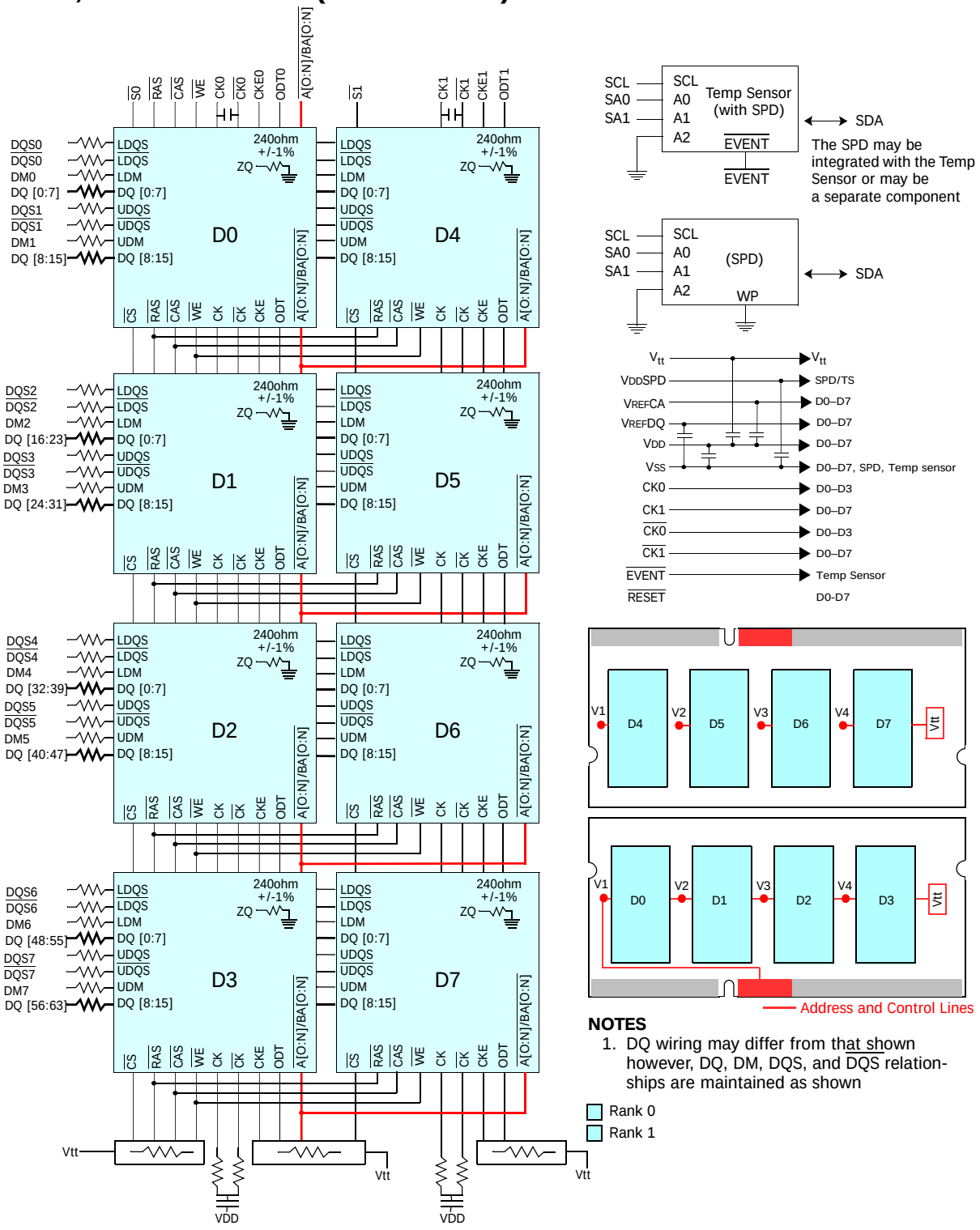


NOTES

1. DQ wiring may differ from that shown however, DQ, DM, DQS, and DQS relationships are maintained as shown

Rank 0

3.2 1GB, 128Mx64 Module(2Rank of x16)

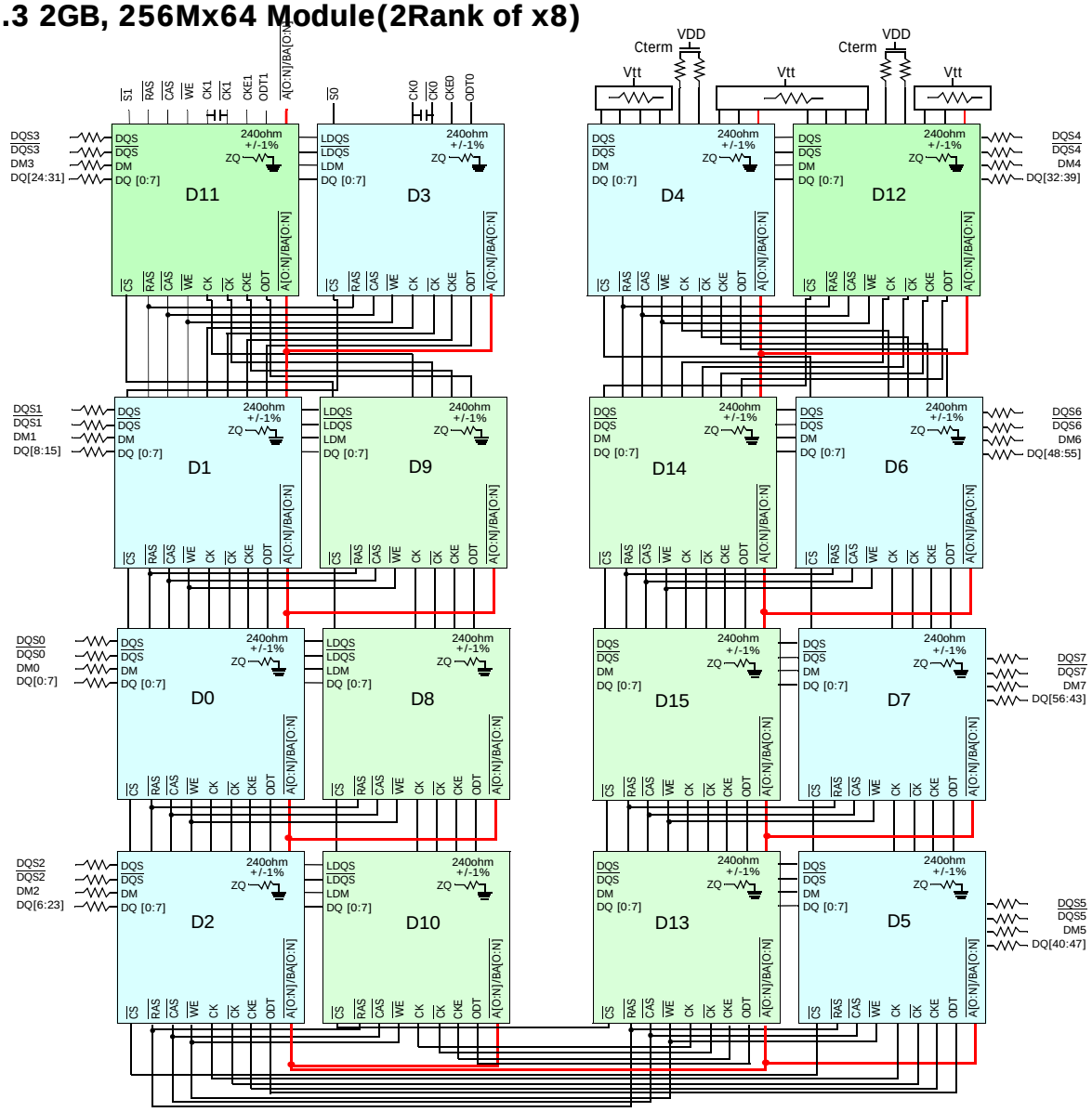


NOTES

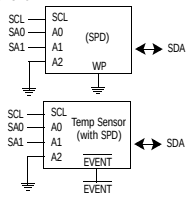
1. DQ wiring may differ from that shown however, DQ, DM, DQS, and DQS relationships are maintained as shown

Rank 0
Rank 1

3.3 2GB, 256Mx64 Module(2Rank of x8)



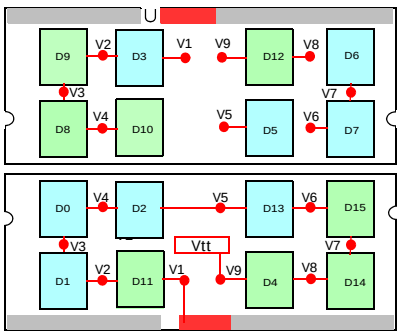
The SPD may be integrated with the Temp Sensor or may be a separate component

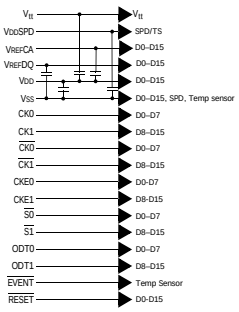


NOTES

1. DQ wiring may differ from that shown however, DQ, DM, DQS, and DQS relationships are maintained as shown

Rank 0
Rank 1





4. ABSOLUTE MAXIMUM RATINGS

4.1 Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	Notes
VDD	Voltage on VDD pin relative to Vss	- 0.4 V ~ 1.975 V	V	1,3
VDDQ	Voltage on VDDQ pin relative to Vss	- 0.4 V ~ 1.975 V	V	1,3
VIN, VOUT	Voltage on any pin relative to Vss	- 0.4 V ~ 1.975 V	V	1
TSTG	Storage Temperature	-55 to +100 ℃	℃	1, 2

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VDD and VDDQ must be within 300mV of each other at all times;and VREF must be not greater than 0.6XVDDQ,When VDD and VDDQ are less than 500mV; VREF may be equal to or less than 300mV.

4.2 DRAM Component Operating Temperature Range

Symbol	Parameter	Rating	Units	Notes
TOPER	Normal Temperature Range	0 to 85	℃	,2
	Extended Temperature Range	85 to 95	℃	1,3

1. Operating Temperature TOPER is the case surface temperature on the center / top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 - 85oC under all operating conditions
3. Some applications require operation of the DRAM in the Extended Temperature Range between 85°... and 95°... case temperature.
   Full specifications are guaranteed in this range, but the following additional conditions apply:
   a) Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 µs. (This double refresh requirement may not apply for some devices.) It is also possible to specify a component with 1X refresh (tREFI to 7.8µs) in the Extended Temperature Range. Please refer to supplier data sheet and/ or the DIMM SPD for option avail ability.
   b) If Self-Refresh operation is required in the Extended Temperature Range, than it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0band MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 = 0b).

5. AC & DC Operating Conditions

5.1 Recommended DC Operating Conditions

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.425	1.500	1.575	V	1,2
VDDQ	Supply Voltage for Output	1.425	1.500	1.575	V	1,2

1. Under all conditions, VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC paramaters are measured with VDD abd VDDQ tied together.

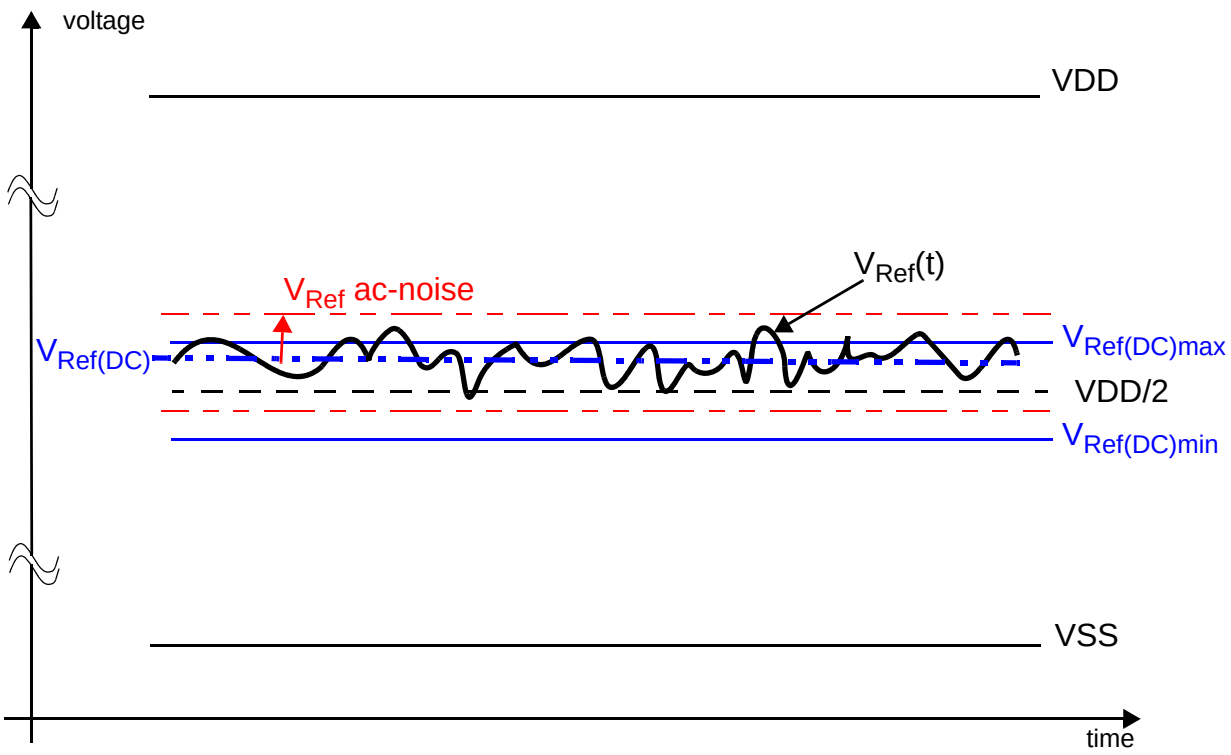
5.2 DC & AC Logic Input Levels

5.2.1 DC & AC Logic Input Levels for Single-Ended Signals

Symbol	Parameter	DDR3-800, DDR3-1066, DDR3-1333		Unit	Notes
		Min	Max		
VIH(DC)	DC input logic high	Vref + 0.100	-	V	1, 2
VIL(DC)	DC input logic low		Vref - 0.100	V	1, 2
VIH(AC)	AC input logic high	Vref + 0.175	-	V	1, 2
VIL(AC)	AC input logic low		Vref - 0.175	V	1, 2
VRefDQ(DC)	Reference Voltage for DQ, DM inputs	0.49 * VDD	0.51 * VDD	V	3, 4
VRefCA(DC)	Reference Voltage for ADD, CMD inputs	0.49 * VDD	0.51 * VDD	V	3, 4
VTT	Termination voltage for DQ, DQS outputs	VDDQ/2 - TBD	VDDQ/2 + TBD	V	

1. For DQ and DM, Vref = VrefDQ. For input ony pins except RESET#, Vref = VrefCA.
2. The “t.b.d.” entries might change based on overshoot and undershoot specification.
3. The ac peak noise on VRef may not allow VRef to deviate from VRef(DC) by more than +/-1% VDD (for reference: approx. +/- 15 mV).
   For reference: approx. VDD/2 +/- 15 mV.

The dc-tolerance limits and ac-noise limits for the reference voltages VRefCA and VRefDQ are illustrated in figure 6.2.1. It shows a valid reference voltage VRef(t) as a function of time. (VRef stands for VRefCA and VRefDQ like-wise).VRef(DC) is the linear average of VRef(t) over a very long period of time (e.g. 1 sec). This average has to meet the min/max requirements in Table 1. Furthermore VRef(t) may temporarily deviate from VRef(DC) by no more than +/- 1% VDD.



< Figure 6.2.1 : Illustration of Vref(DC) tolerance and Vref AC-noise limits >

The voltage levels for setup and hold time measurements VIH(AC), VIH(DC), VIL(AC) and VIL(DC) are dependent on VRef. "VRef " shall be understood as VRef(DC), as defined in Figure 6.2.1
This clarifies, that dc-variations of VRef affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for VRef(DC) deviations from the optimum position within the data-eye of the input signals.
This also clarifies that the DRAM setup/hold specification and derating values need to include time and voltage associated with VRef ac-noise. Timing and voltage effects due to ac-noise on VRef up to the specified limit (+/-1% of VDD) are included in DRAM timings and their associated deratings.

5.2.2 DC & AC Logic Input Levels for Differential Signals

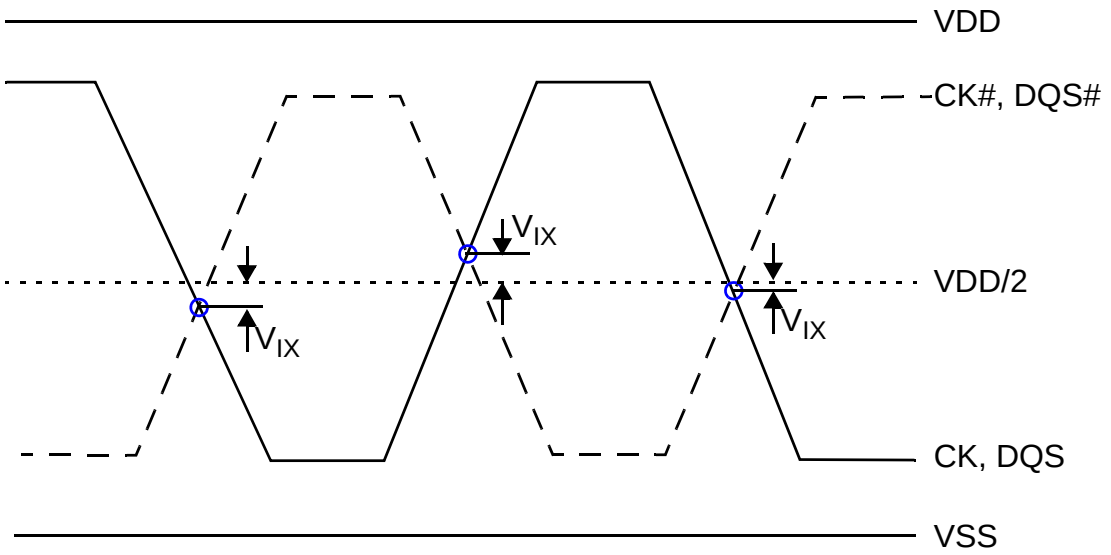
Symbol	Parameter	DDR3-800, DDR3-1066, DDR3-1333, DDR3-1600		Unit	Notes
		Min	Max		
VIHdiff	Differential input logic high	+ 0.200	-	V	1
VILdiff	Differential input logic low		- 0.200	V	1

Note1:

Refer to “Overshoot and Undershoot Specification section 6.5 on 26 page

5.2.3 Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signals (CK, CK# and DQS, DQS#) must meet the requirements in Table 6.2.3 The differential input cross point voltage VIX is measured from the actual cross point of true and complement signal to the midlevel between of VDD and VSS.



< Figure 5.2.3 Vix Definition >

Symbol	Parameter	DDR3-800, DDR3-1066, DDR3-1333, DDR3-1600		Unit	Notes
		Min	Max		
V_{IX}	Differential Input Cross Point Voltage relative to VDD/2	- 150	+ 150	mV	

< Table 5.2.3 : Cross point voltage for differential input signals (CK, DQS) >

5.3 Slew Rate Definitions

5.3.1 For Single Ended Input Signals

- Input Slew Rate for Input Setup Time (tIS) and Data Setup Time (tDS)

Setup (tIS and tDS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VRef and the first crossing of VIH(AC)min. Setup (tIS and tDS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VRef and the first crossing of VIL(AC)max.

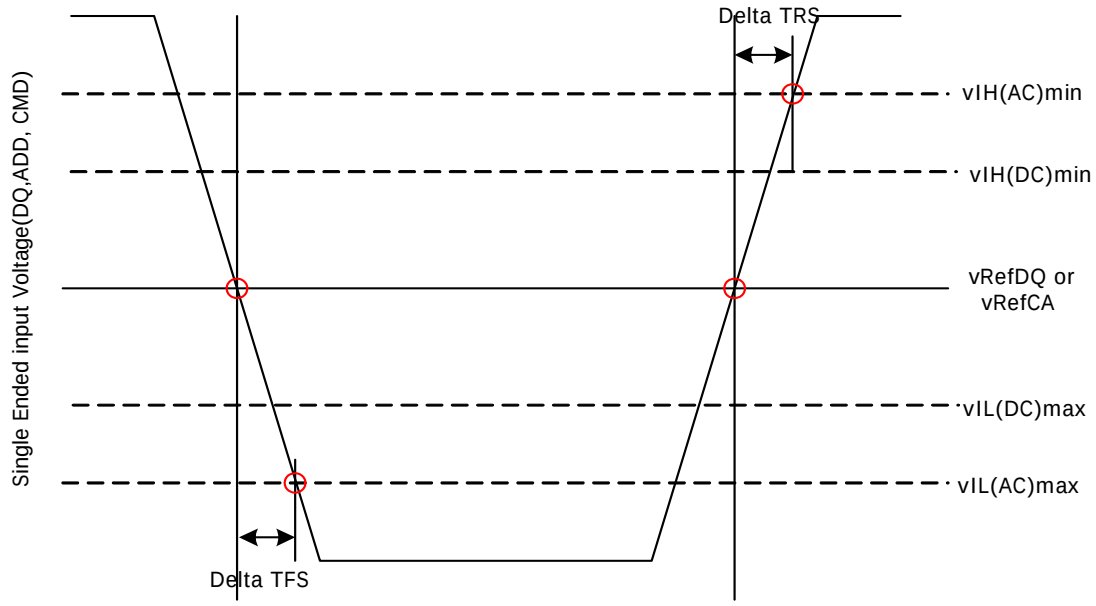
- Input Slew Rate for Input Hold Time (tIH) and Data Hold Time (tDH)

Hold nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(DC)max and the first crossing of VRef. Hold (tIH and tDH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(DC)min and the first crossing of VRef.

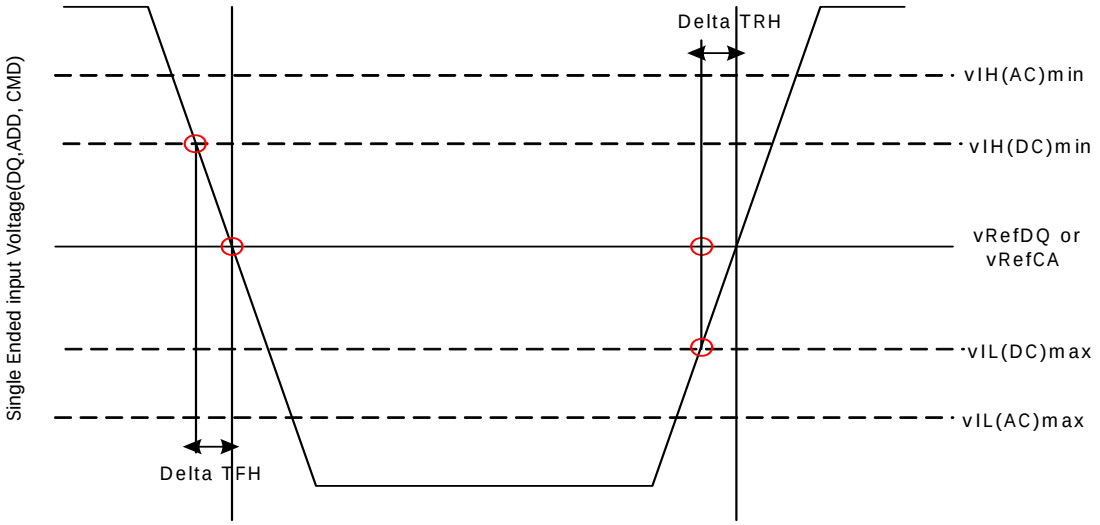
Description	Measured		Defined by	Applicable for
	Min	Max		
Input slew rate for rising edge	Vref	VIH(AC)min	$\frac{\text{VIH(AC)min-Vref}}{\overline{\text{Delta TRS}}}$	Setup (tIS, tDS)
Input slew rate for falling edge	Vref	VIL(AC)max	$\frac{\text{Vref-VIL(AC)max}}{\overline{\text{Delta TFS}}}$	
Input slew rate for rising edge	VIL(DC)max	Vref	$\frac{\text{Vref-VIL(DC)max}}{\overline{\text{Delta TFH}}}$	Hold (tIH, tDH)
Input slew rate for falling edge	VIH(DC)min	Vref	$\frac{\text{VIH(DC)min-Vref}}{\overline{\text{Delta TRH}}}$	

< Table 5.3.1 : Single-Ended Input Slew Rate Definition >

Part A: Set up



Part B: Hold



< Figure 5.3.1 : Input Nominal Slew Rate Definition for Single-Ended Signals >

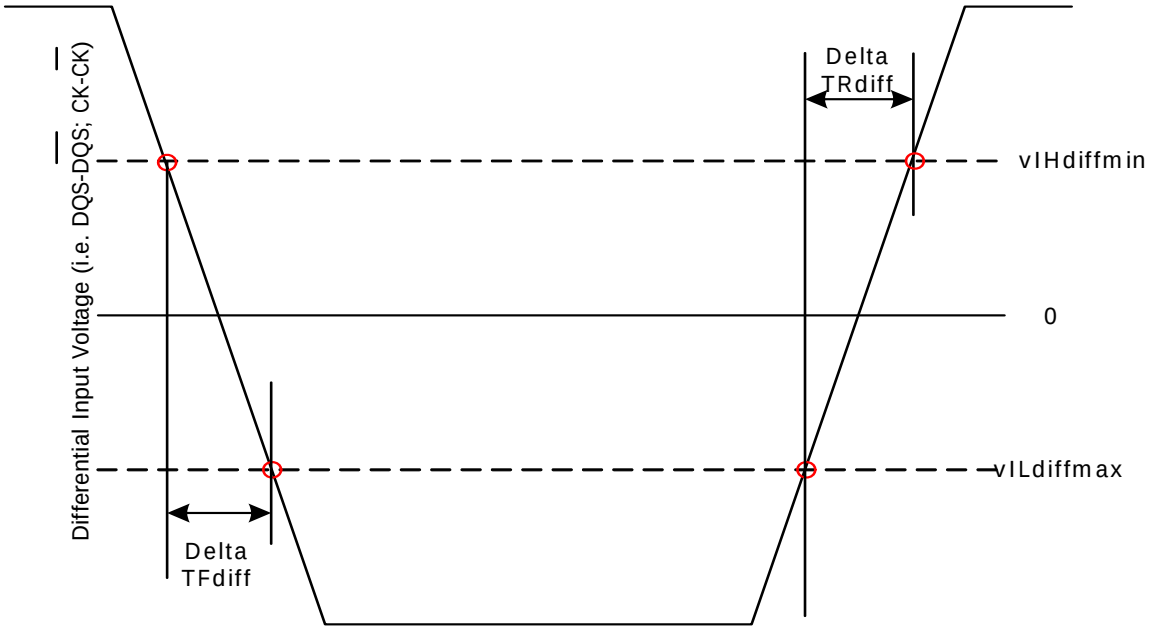
5.3.2 Differential Input Signals

Input slew rate for differential signals (CK, CK# and DQS, DQS#) are defined and measured as shown in below Table and Figure .

Description	Measured		Defined by
	Min	Max	
Differential input slew rate for rising edge (CK-CK and DQS-DQS)	VILdiffmax	VIHdiffmin	VIHdiffmin-VILdiffmax / $\overline{\text{DeltaTRdiff}}$
Differential input slew rate for falling edge (CK-CK and DQS-DQS)	VIHdiffmin	VILdiffmax	VIHdiffmin-VILdiffmax / $\overline{\text{DeltaTFdiff}}$

Note:

The differential signal (i.e. CK-CK and DQS-DQS) must be linear between these thresholds.



< Figure 5.3.2 : Differential Input Slew Rate Definition for DQS,DQS# and CK,CK# >

5.4 DC & AC Output Buffer Levels

5.4.1 Single Ended DC & AC Output Levels

Below table shows the output levels used for measurements of single ended signals.

Symbol	Parameter	DDR3-800, 1066, 1333	Unit	Notes
VOH(DC)	DC output high measurement level (for IV curve linearity)	0.8 x VDDQ	V	
VOM(DC)	DC output mid measurement level (for IV curve linearity)	0.5 x VDDQ	V	
VOL(DC)	DC output low measurement level (for IV curve linearity)	0.2 x VDDQ	V	
VOH(AC)	AC output high measurement level (for output SR)	VTT + 0.1 x VDDQ	V	1
VOL(AC)	AC output low measurement level (for output SR)	VTT - 0.1 x VDDQ	V	1

1. The swing of ± 0.1 x VDDQ is based on approximately 50% of the static single ended output high or low swing with a driver impedance of 40Ω and an effective test load of 25Ω to VTT = VDDQ / 2.

5.4.2 Differential DC & AC Output Levels

Below table shows the output levels used for measurements of differential signals.

Symbol	Parameter	DDR3-800, 1066, 1333	Unit	Notes
VOHdiff (AC)	AC differential output high measurement level (for output SR)	+ 0.2 x VDDQ	V	1
VOLdiff (AC)	AC differential output low measurement level (for outtput SR)	- 0.2 x VDDQ	V	1

1. The swing of °æ 0.2 x VDDQ is based on approximately 50% of the static differential output high or low swingwith a driver impedance of 40ßŸ and an effective test load of 25ßŸ to VTT = VDDQ/2 at each of the differential output

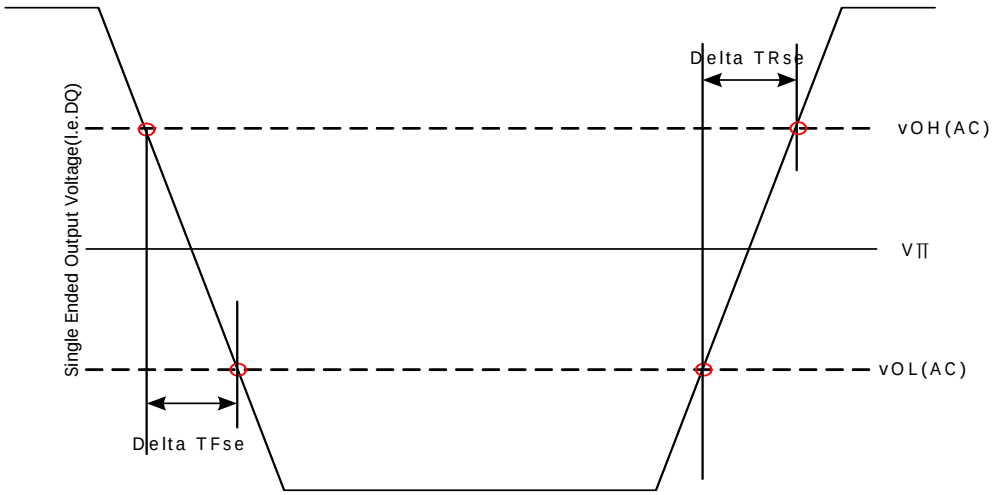
5.4.3 Single Ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOL(AC) and VOH(AC) for single ended signals as shown in below Table and Figure 6.4.3.

Description	Measured		Defined by
	From	To	
Single ended output slew rate for rising edge	VOL(AC)	VOH(AC)	$\frac{VOH(AC)-VOL(AC)}{DeltaTRse}$
Single ended output slew rate for falling edge	VOH(AC)	VOL(AC)	$\frac{VOH(AC)-VOL(AC)}{DeltaTFse}$

Note:

Output slew rate is verified by design and characterisation, and may not be subject to production test.



< Figure 5.4.3 : Single Ended Output Slew Rate Definition >

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		Units
		Min	Max	Min	Max	Min	Max	
Single-ended Output Slew Rate	SRQse	2.5	5	2.5	5	2.5	5	V/ns

***** Description :**
SR : Slew Rate
Q: Query Output (like in DQ, which stands for Data-in, Query-Output)
For Ron = RZQ/7 setting

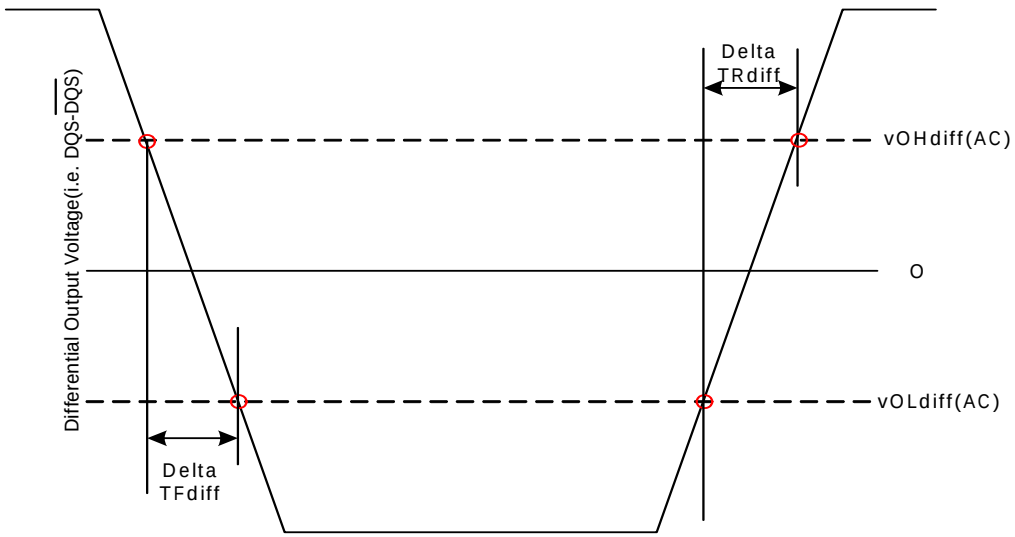
< Table 5.4.3 : Output Slew Rate (single-ended) >

5.4.4 Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOLdiff(AC) and VOHdiff(AC) for differential signals as shown in below Table and Figure 5.4.4

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	VOLdiff(AC)	VOHdiff(AC)	VOHdiff(AC)-VOLdiff(AC) / DeltaTRdiff
Differential output slew rate for falling edge	VOHdiff(AC)	VOLdiff(AC)	VOHdiff(AC)-VOLdiff(AC) / DeltaTFdiff

Note: Output slew rate is verified by design and characterization, and may not be subject to production test..



< Figure 5.4.4 : Differential Output Slew Rate Definition >

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		Units
		Min	Max	Min	Max	Min	Max	
Differential Output Slew Rate	SRQdiff	5	10	5	10	5	10	V/ns

*****Description :**
SR : Slew Rate
Q : Query Output (like in DQ, which stands for Data-in, Query-Output)
diff : Differential Signals
For Ron = RZQ/7 setting

< Table 5.4.4 : Differential Output Slew Rate >

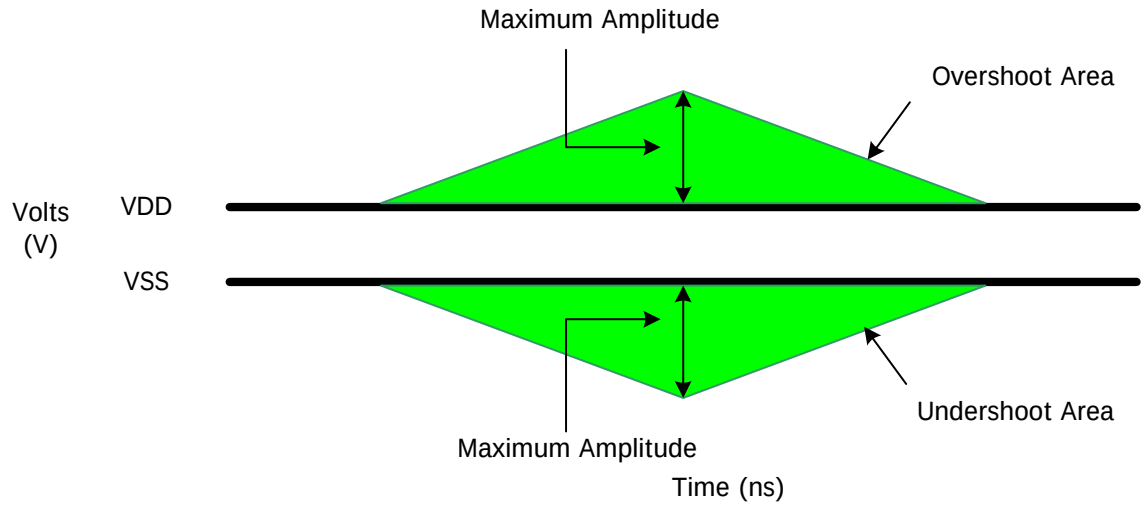
5.5 Overshoot and Undershoot Specifications

5.5.1 Address and Control Overshoot and Undershoot Specifications

Description	Specification		
	DDR3-800	DDR3-1066	DDR3-1333
Maximum peak amplitude allowed for overshoot area (see Figure)	0.4V	0.4V	0.4V
Maximum peak amplitude allowed for undershoot area (see Figure)	0.4V	0.4V	0.4V
Maximum overshoot area above VDD (See Figure)	0.67 V-ns	0.5 V-ns	0.4 V-ns
Maximum undershoot area below VSS (See Figure)	0.67 V-ns	0.5 V-ns	0.4 V-ns

< Table 5.5.1 : AC Overshoot/Undershoot Specification for Address and Control Pins >

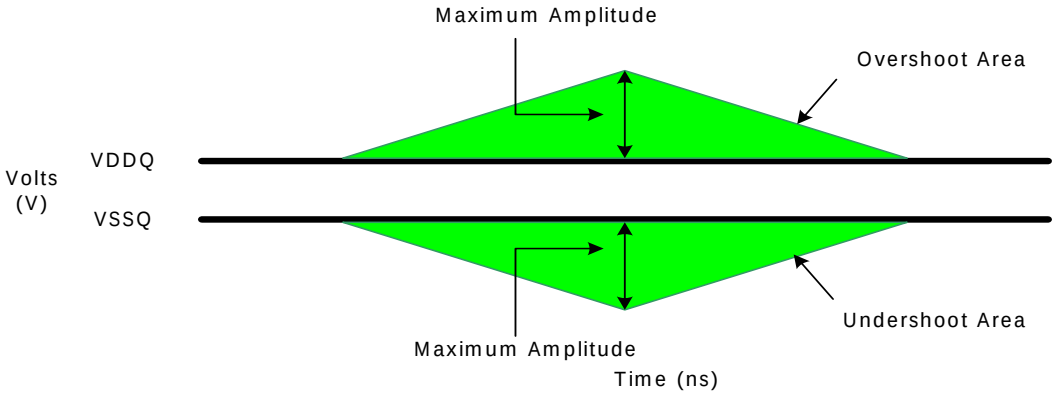
< Figure 5.5.1 : Address and Control Overshoot and Undershoot Definition >



5.5.2 Clock,Data,Strobe and Mask Overshoot and Undershoot Specifications

Description	Specification		
	DDR3-800	DDR3-1066	DDR3-1333
Maximum peak amplitude allowed for overshoot area (see Figure)	0.4V	0.4V	0.4V
Maximum peak amplitude allowed for undershoot area (see Figure)	0.4V	0.4V	0.4V
Maximum overshoot area above VDDQ (See Figure)	0.25 V-ns	0.19 V-ns	0.15 V-ns
Maximum undershoot area below VSSQ (See Figure)	0.25 V-ns	0.19 V-ns	0.15 V-ns

< Table 5.5.2 : AC Overshoot/Undershoot Specification for Clock, Data, Strobe and Mask >



Clock, Data Strobe and Mask Overshoot and Undershoot Definition

< Figure 5.5.2 : Clock, Data, Strobe and Mask Overshoot and Undershoot Definition >

5.6 Pin Capacitance

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		Units	Notes
		Min	Max	Min	Max	Min	Max		
Input/output capacitance (DQ, DM, DQS, DQS#, TDQS, TDQS#)	C_{IO}	TBD	TBD	TBD	TBD	TBD	TBD	pF	1,2,3
Input capacitance, CK and CK#	C_{CK}	TBD	TBD	TBD	TBD	TBD	TBD	pF	2,3,5
Input capacitance delta CK and CK#	C_{DCK}	TBD	TBD	TBD	TBD	TBD	TBD	pF	2,3,4
Input capacitance (All other input-only pins)	C_{I}	TBD	TBD	TBD	TBD	TBD	TBD	pF	2,3,6
Input capacitance delta, DQS and DQS#	C_{DDQS}	TBD	TBD	TBD	TBD	TBD	TBD	pF	2,3,12
Input capacitance delta (All CTRL input-only pins)	C_{DI_CTRL}	TBD	TBD	TBD	TBD	TBD	TBD	pF	2,3,7,8
Input capacitance delta (All ADD/CMD input-only pins)	$C_{DI\_ADD\_CMD}$	TBD	TBD	TBD	TBD	TBD	TBD	pF	2,3,9,10
Input/output capacitance delta (DQ, DM, DQS, DQS#)	C_{DIO}	TBD	TBD	TBD	TBD	TBD	TBD	pF	2,3,11

Notes:

1. TDQS/TDQS# are not necessarily input function but since TDQS is sharing DM pin and the parasitic characterization of TDQS/TDQS# should be close as much as possible, Cio&Cdio requirement is applied (recommend deleting note or changing to “Although the DM, TDQS and TDQS# pins have different functions, the loading matches DQ and DQS.”)
2. This parameter is not subject to production test. It is verified by design and characterization. Input capacitance is measured according to JEP147(“PROCEDURE FOR MEASURING INPUT CAPACITANCE USING A VECTOR NETWORK ANALYZER(VNA)”) with VDD, VDDQ, VSS,VSSQ applied and all other pins floating (except the pin under test, CKE, RESET# and ODT as necessary). VDD=VDDQ=1.5V, VBIAS=VDD/2 and on-die termination off.
3. This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here
4. Absolute value of C_{CK}-C_{CK}#.
5. The minimum C_{CK} will be equal to the minimum C_{I}.
6. Input only pins include: ODT, CS, CKE, A0-A15, BA0-BA2, RAS#, CAS#, WE#.
7. CTRL pins defined as ODT, CS and CKE.
8. $C_{DI\_CTRL}=C_{I}(CNTL) - 0.5 * C_{I}(CLK) + C_{I}(CLK\#))$
9. ADD pins defined as A0-A15, BA0-BA2 and CMD pins are defined as RAS#, CAS# and WE#.
10. $C_{DI\_ADD\_CMD}=C_{I}(ADD\_CMD) - 0.5*(C_{I}(CLK)+C_{I}(CLK\#))$
11. $C_{DIO}=C_{IO}(DQ) - 0.5*(C_{IO}(DQS)+C_{IO}(DQS\#))$
12. Absolute value of $C_{IO}(DQS) - C_{IO}(DQS\#)$

5.7 IDD Specifications(T_{CASE} : 0 to 95°C)

512MB, 64M x 64 SO-DIMM : HMT164S6AFP6C

Symbol	DDR3 800	DDR3 1066	DDR3 1333	Unit	note
IDD0	360	420	480	mA	
IDD1	480	540	620	mA	
IDD2P(F)	100	120	140	mA	
IDD2P(S)	40	40	40	mA	
IDD2Q	180	240	280	mA	
IDD2N	200	240	300	mA	
IDD3P	140	180	200	mA	
IDD3N	220	280	340	mA	
IDD4W	700	880	1060	mA	
IDD4R	700	860	1020	mA	
IDD5B	740	780	840	mA	
IDD6(D)	40	40	40	mA	1
IDD6(S)	24	24	24	mA	1
IDD7	1300	1420	1720	mA	

1GB, 128M x 64 SO-DIMM : HMT112S6AFP6C

Symbol	DDR3 800	DDR3 1066	DDR3 1333	Unit	note
IDD0	560	660	780	mA	
IDD1	680	780	960	mA	
IDD2P(F)	200	240	280	mA	
IDD2P(S)	80	80	80	mA	
IDD2Q	360	480	560	mA	
IDD2N	400	480	600	mA	
IDD3P	280	360	400	mA	
IDD3N	440	560	680	mA	
IDD4W	900	1120	1360	mA	
IDD4R	900	1100	1320	mA	
IDD5B	940	1020	1140	mA	
IDD6(D)	80	80	80	mA	1
IDD6(S)	48	48	48	mA	1
IDD7	1500	1660	2020	mA	

2GB, 256M x 64 SO-DIMM : HMT125S6AFP8C

Symbol	DDR3 800	DDR3 1066	DDR3 1333	Unit	note
IDD0	1040	1240	1440	mA	
IDD1	1160	1360	1560	mA	
IDD2P(F)	400	480	560	mA	
IDD2P(S)	160	160	160	mA	
IDD2Q	720	960	1120	mA	
IDD2N	800	960	1200	mA	
IDD3P	560	720	800	mA	
IDD3N	880	1120	1360	mA	
IDD4W	1520	1920	2160	mA	
IDD4R	1440	1800	2280	mA	
IDD5B	1880	2040	2320	mA	
IDD6(D)	160	160	160	mA	1
IDD6(S)	96	96	96	mA	1
IDD7	2200	2480	3040	mA	

5.7 IDD Measurement Conditions

Within the tables provided further down, an overview about the IDD measurement conditions is provided as follows:

Table 1 — Overview of Tables providing IDD Measurement Conditions and DRAM Behavior

Table number	Measurement Conditions
Table 5 on page 33	IDD0 and IDD1
Table 6 on page 36	IDD2N, IDD2Q, IDD2P(0), IDD2P(1)
Table 7 on page 38	IDD3N and IDD3P
Table 8 on page 39	IDD4R, IDD4W, IDD7
Table 9 on page 42	IDD7 for different Speed Grades and different tRRD, tFAW conditions
Table 10 on page 43	IDD5B
Table 11 on page 44	IDD6, IDD6ET

Within the tables about IDD measurement conditions, the following definitions are used:

- LOW is defined as VIN <= VILAC(max.); HIGH is defined as VIN >= VIHAC(min.).

- STABLE is defined as inputs are stable at a HIGH or LOW level.

- FLOATING is defined as inputs are VREF = VDDQ / 2.

- SWITCHING is defined as described in the following 2 tables.

Table 2 — Definition of SWITCHING for Address and Command Input Signals

SWITCHING for **Address (row, column) and Command Signals ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)** is defined as:	
Address (row, column):	If not otherwise mentioned the inputs are stable at HIGH or LOW during 4 clocks and change then to the opposite value (e.g. Ax Ax Ax Ax $\overline{Ax}$ $\overline{Ax}$ $\overline{Ax}$ $\overline{Ax}$ Ax Ax Ax Ax ..... please see each IDDx definition for details
Bank address:	If not otherwise mentioned the bank addresses should be switched like the row/column addresses - please see each IDDx definition for details
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$):	Define D = {$\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ } := {HIGH, LOW, LOW, LOW} Define $\overline{D}$ = {$\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ } := {HIGH, HIGH,HIGH,HIGH} Define Command Background Pattern = D D $\overline{D}$ $\overline{D}$ D D $\overline{D}$ $\overline{D}$ D D $\overline{D}$ $\overline{D}$ ... If other commands are necessary (e.g. ACT for IDD0 or Read for IDD4R), the Background Pattern Command is substituted by the respective $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ levels of the necessary command. See each IDDx definition for details and figures 1,2,3 as examples.

Table 3 — Definition of SWITCHING for Data (DQ)

SWITCHING for **Data (DQ)** is defined as	
Data (DQ)	Data DQ is changing between HIGH and LOW every other data transfer (once per clock) for DQ signals, which means that data DQ is stable during one clock; see each IDDx definition for exceptions from this rule and for further details. See figures 1,2,3 as examples.
Data Masking (DM)	NO Switching; DM must be driven LOW all the time

Timing parameters are listed in the following table:

Table 4 — For IDD testing the following parameters are utilized.

Parameter Bin		**DDR3-800**		**DDR3-1066**			**DDR3-1333**			**Unit**
		5-5-5	6-6-6	6-6-6	7-7-7	8-8-8	7-7-7	8-8-8	9-9-9	
t_{CKmin}(IDD)		2.5		1.875			1.5			ns
CL(IDD)		5	6	6	7	8	7	8	9	clk
t_{RCDmin}(IDD)		12.5	15	11.25	13.13	15	10.5	12	13.5	ns
t_{RCmin}(IDD)		50	52.5	48.75	50.63	52.50	46.5	48	49.5	ns
t_{RASmin}(IDD)		37.5	37.5	37.5	37.5	37.5	36	36	36	ns
t_{RPmin}(IDD)		12.5	15	11.25	13.13	15	10.5	12	13.5	ns
t_{FAW}(IDD)	x4/x8	40	40	37.5	37.5	37.5	30	30	30	ns
	x16	50	50	50	50	50	45	45	45	ns
t_{RRD}(IDD)	x4/x8	10	10	7.5	7.5	7.5	6.0	6.0	6.0	ns
	x16	10	10	10	10	10	7.5	7.5	7.5	ns
t_{RFC}(IDD) - 512Mb		90	90	90	90	90	90	90	90	ns
t_{RFC}(IDD) - 1 Gb		110	110	110	110	110	110	110	110	ns
t_{RFC}(IDD) - 2 Gb		160	160	160	160	160	160	160	160	ns
t_{RFC}(IDD) - 4 Gb		tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	ns

The following conditions apply:

- IDD specifications are tested after the device is properly initialized.

- Input slew rate is specified by AC Parametric test conditions.

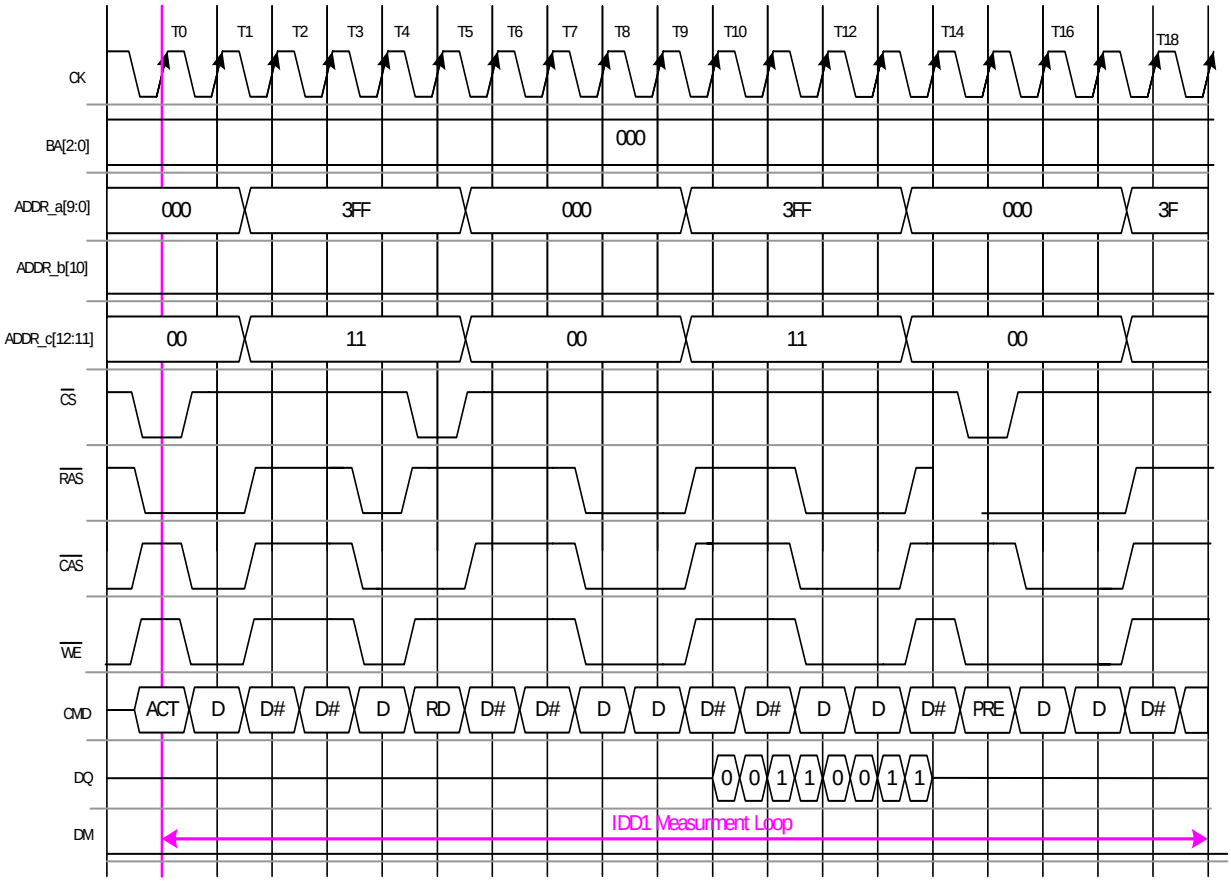
- IDD parameters are specified with ODT and output buffer disabled (MR1 Bit A12).

Table 5 — IDD Measurement Conditions for IDD0 and IDD1

Current	I_{DD0}	I_{DD1}
Name	**Operating Current 0** **-> One Bank Activate** **-> Precharge**	**Operating Current 1** **-> One Bank Activate** **-> Read** **-> Precharge**
Measurement Condition		
Timing Diagram Example		Figure 1
CKE	HIGH	HIGH
External Clock	on	on
t_{CK}	t_{CKmin}(IDD)	t_{CKmin}(IDD)
t_{RC}	t_{RCmin}(IDD)	t_{RCmin}(IDD)
t_{RAS}	t_{RASmin}(IDD)	t_{RASmin}(IDD)
t_{RCD}	n.a.	t_{RCDmin}(IDD)
t_{RRD}	n.a.	n.a.
CL	n.a.	CL(IDD)
AL	n.a.	0
$\overline{CS}$	HIGH between. Activate and Precharge Commands	HIGH between Activate, Read and Precharge
Command Inputs ($\overline{CS}$,$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	SWITCHING as described in Table 2 only exceptions are Activate and Precharge commands; example of IDD0 pattern: **A0**D$\overline{D}$D$\overline{D}$D$\overline{D}$D$\overline{D}$D$\overline{D}$ **P0** (DDR3-800: t_{RAS} = 37.5ns between (A)ctivate and (P)recharge to bank 0; Definition of D and $\overline{D}$: see Table 2	SWITCHING as described in Table 2; only exceptions are Activate, Read and Precharge commands; example of IDD1 pattern: **A0**D$\overline{D}$D$\overline{D}$**R0**D$\overline{D}$D$\overline{D}$D$\overline{D}$D$\overline{D}$ **P0** (DDR3-800 -555: t_{RCD} = 12.5ns between (A)ctivate and (R)ead to bank **0**; Definition of D and $\overline{D}$: see Table 2)

Table 5 — IDD Measurement Conditions for IDD0 and IDD1

Current	I_{DD0}	I_{DD1}
Name	**Operating Current 0** **-> One Bank Activate** **-> Precharge**	**Operating Current 1** **-> One Bank Activate** **-> Read** **-> Precharge**
Row, Column Afddresses	Row addresses SWITCHING as described in Table 2; Address Input A10 must be LOW all the time!	Row addresses SWITCHING as described in Table 2; Address Input A10 must be LOW all the time!
Bank Addresses	bank address is fixed (bank 0)	bank address is fixed (bank 0)
Data I/O	SWITCHING as described in Table 3	Read Data: output data switches every clock, which means that Read data is stable during one clock cycle. To achieve Iout = 0mA, the output buffer should be switched off by MR1 Bit A12 set to “1”. When there is no read data burst from DRAM, the DQ I/O should be FLOATING.
Output Buffer DQ,DQS / MR1 bit A12	off / 1	off / 1
ODT / MR1 bits [A6, A2]	disabled / [0,0]	disabled / [0,0]
Burst length	n.a.	8 fixed / MR0 Bits [A1, A0] = {0,0}
Active banks	one ACT-PRE loop	one ACT-RD-PRE loop
Idle banks	all other	all other
Precharge Power Down Mode / Mode Register Bit 12	n.a.	n.a.



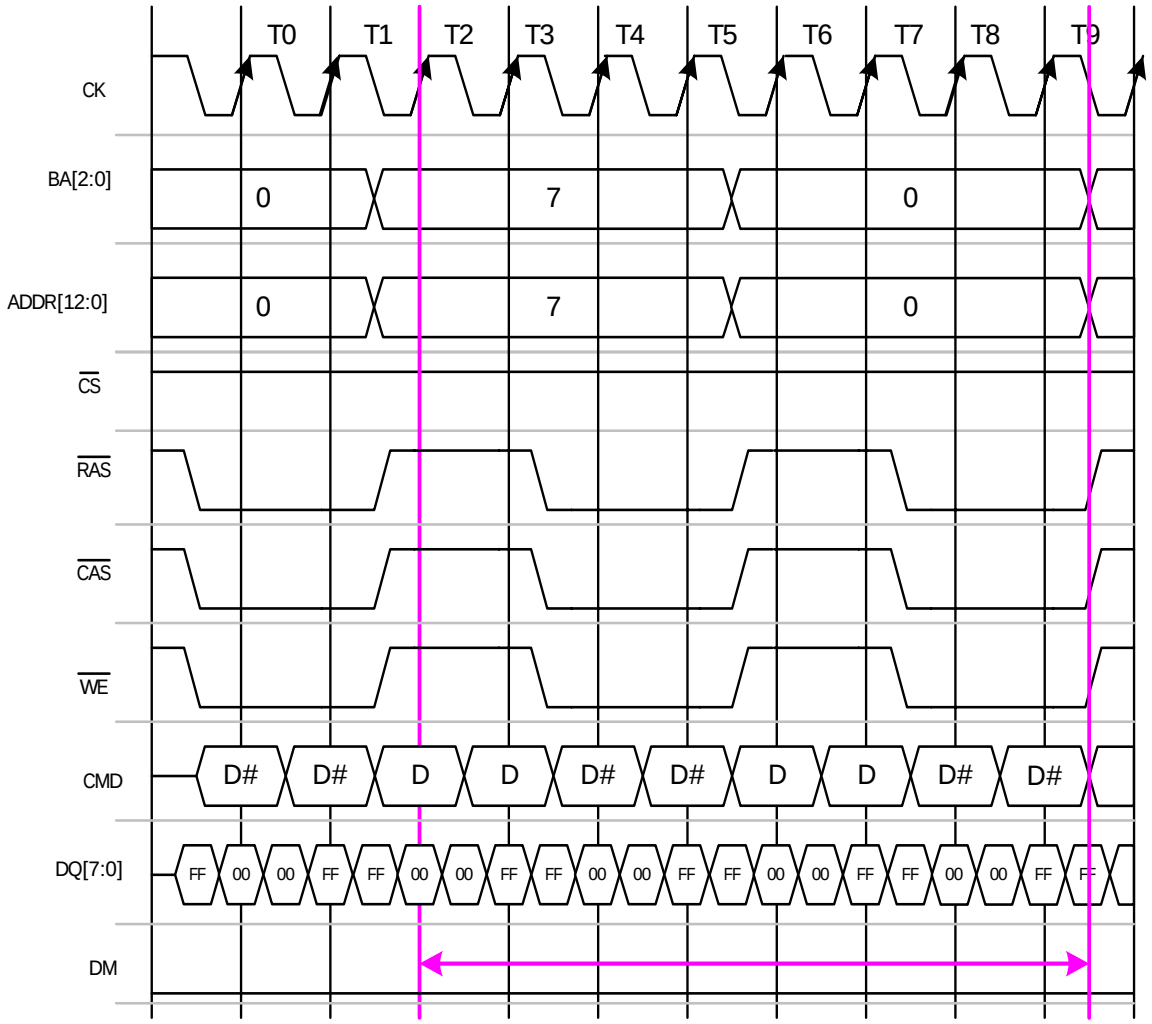
< Figure 1. IDD1 Example > (DDR3-800-555, 512Mb x8): Data DQ is shown but the output buffer should be switched off (per MR1 Bit A12 ="1") to achieve Iout = 0mA. Address inputs are split into 3 parts.

Table 6 — IDD Measurement Conditions for IDD2N, IDD2P(1), IDD2P(0) and IDD2Q

Current	I_{DD2N}	$I_{DD2P}(1)$ [a]	$I_{DD2P}(0)$	I_{DD2Q}
Name	**Precharge Standby Current**	**Precharge Power Down Current Fast Exit - MRS A12 Bit = 1**	**Precharge Power Down Current Slow Exit - MRS A12 Bit = 0**	**Precharge Quiet Standby Current**
Measurement Condition				
Timing Diagram Example	Figure 2			
CKE	HIGH	LOW	LOW	HIGH
External Clock	on	on	on	on
t_{CK}	t_{CKmin}(IDD)	t_{CKmin}(IDD)	t_{CKmin}(IDD)	t_{CKmin}(IDD)
t_{RC}	n.a.	n.a.	n.a.	n.a.
t_{RAS}	n.a.	n.a.	n.a.	n.a.
t_{RCD}	n.a.	n.a.	n.a.	n.a.
t_{RRD}	n.a.	n.a.	n.a.	n.a.
CL	n.a.	n.a.	n.a.	n.a.
AL	n.a.	n.a.	n.a.	n.a.
$\overline{CS}$	HIGH	STABLE	STABLE	HIGH
Bank Address, Row Addr. and Command Inputs	SWITCHING as described in Table 2	STABLE	STABLE	STABLE
Data inputs	SWITCHING	FLOATING	FLOATING	FLOATING
Output Buffer DQ,DQS / MR1 bit A12	off / 1	off / 1	off / 1	off / 1
ODT / MR1 bits [A6, A2]	disabled / [0,0]	disabled / [0,0]	disabled / [0,0]	disabled / [0,0]
Burst length	n.a.	n.a.	n.a.	n.a.
Active banks	none	none	none	none
Idle banks	all	all	all	all
Precharge Power Down Mode / Mode Register Bit [a]	n.a.	Fast Exit / 1 (any valid command after tXP[b])	Slow Exit / 0 Slow exit (RD and ODT commands must satisfy tXPDLL-AL)	n.a.

a. In DDR3, the MRS Bit 12 defines DLL on/off behaviour ONLY for precharge power down. There are 2 different Precharge Power Down states possible: one with DLL on (fast exit, bit 12 = 1) and one with DLL off (slow exit, bit 12 = 0).

b. Because it is an exit after precharge power down, the valid commands are: Activate, Refresh, Mode-Register Set, Enter - Self Refresh



<Figure 2. IDD2N / IDD3N Example > (DDR3-800-555, 512Mb x8)

Table 7 — IDD Measurement Conditions for IDD3N and IDD3P(fast exit)

Current	I_{DD3N}	I_{DD3P}
Name	**Active Standby Current**	**Active Power-Down Current[a] Always Fast Exit**
Measurement Condition		
Timing Diagram Example	Figure 2	
CKE	HIGH	LOW
External Clock	on	on
t_{CK}	t_{CKmin}(IDD)	t_{CKmin}(IDD)
t_{RC}	n.a.	n.a.
t_{RAS}	n.a.	n.a.
t_{RCD}	n.a.	n.a.
t_{RRD}	n.a.	n.a.
CL	n.a.	n.a.
AL	n.a.	n.a.
$\overline{CS}$	HIGH	STABLE
Addr. and cmd Inputs	SWITCHING as described in Table 2	STABLE
Data inputs	SWITCHING as described in Table 3	FLOATING
Output Buffer DQ,DQS / MR1 bit A12	off / 1	off / 1
ODT / MR1 bits [A6, A2]	disabled / [0,0]	disabled / [0,0]
Burst length	n.a.	n.a.
Active banks	all	all
Idle banks	none	none
Precharge Power Down Mode / Mode Register Bit [a]	n.a.	n.a. (Active Power Down Mode is always “Fast Exit” with DLL on

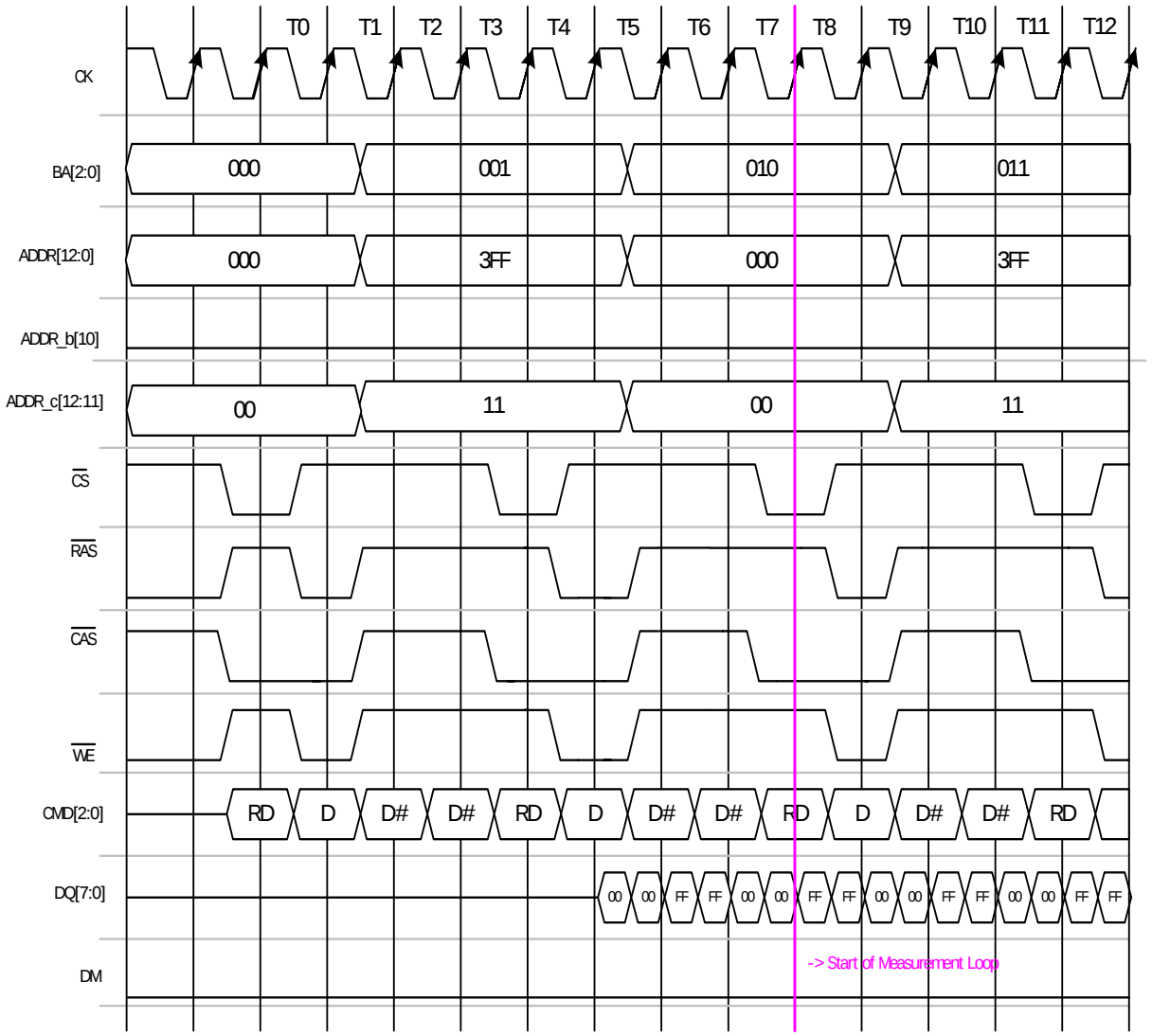
a. DDR3 will offer only ONE active power down mode with DLL on (-> fast exit). MRS bit 12 will not be used for active power down. Instead bit 12 will be used to switch between two different precharge power down modes.

Table 8 — IDD Measurement Conditions for IDD4R, IDD4W and IDD7

Current	I_{DD4R}	I_{DD4W}	I_{DD7}
Name	**Operating Current Burst Read**	**Operating Current Burst Write**	**All Bank Interleave Read Current**
Measurement Condition			
Timing Diagram Example	Figure 3		
CKE	HIGH	HIGH	HIGH
External Clock	on	on	on
t_{CK}	t_{CKmin}(IDD)	t_{CKmin}(IDD)	t_{CKmin}(IDD)
t_{RC}	n.a.	n.a.	t_{RCmin}(IDD)
t_{RAS}	n.a.	n.a.	t_{RASmin}(IDD)
t_{RCD}	n.a.	n.a.	t_{RCDmin}(IDD)
t_{RRD}	n.a.	n.a.	t_{RRDmin}(IDD)
CL	CL(IDD)	CL(IDD)	CL(IDD)
AL	0	0	t_{RCDmin} - 1 t_{CK}
$\overline{CS}$	HIGH btw. valid cmds	HIGH btw. valid cmds	HIGH btw. valid cmds
Command Inputs ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	SWITCHING as described in Table 2; exceptions are Read commands => IDD4R Pattern: **R0**DDD**R1**DDD**R2**DDD**R3** .DDD **R4** ..... Rx = Read from bank x; Definition of D and $\overline{D}$: see Table 2	SWITCHING as described in Table 2 ; exceptions are Write commands => IDD4W Pattern: **W0**DDD**W1**DDD**W2**DDD**W3** DDD **W4** ... Wx = Write to bank x; Definition of D and $\overline{D}$: see Table 2	For patterns see Table 9

Table 8 — IDD Measurement Conditions for IDD4R, IDD4W and IDD7

Current	I_{DD4R}	I_{DD4W}	I_{DD7}
Name	**Operating Current Burst Read**	**Operating Current Burst Write**	**All Bank Interleave Read Current**
Row, Colum Addresses	column addresses SWITCHING as described in Table 2 ; Address Input A10 must be LOW all the time!	column addresses SWITCHING as described in Table 2 ; Address Input A10 must be LOW all the time!	STABLE during DESELECTs
Bank Addresses	bank address cycling (0 -> 1 -> 2 -> 3 ...)	bank address cycling (0 -> 1 -> 2 -> 3 ...)	bank address cycling (0 -> 1 -> 2 -> 3 ...), see pattern in Table 9
DQ I/O	Seamless Read Data Burst (BL8): output data switches every clock, which means that Read data is stable during one clock cycle. To achieve Iout = 0mA the output buffer should be switched off by MR1 Bit A12 set to “1”.	Seamless Write Data Burst (BL8): input data switches every clock, which means that Write data is stable during one clock cycle. DM is low all the time.	Read Data (BL8): output data switches every clock, which means that Read data is stable during one clock cycle. To achieve Iout = 0mA the output buffer should be switched off by MR1 Bit A12 set to “1”.
Output Buffer DQ,DQS / MR1 bit A12	off / 1	off / 1	off / 1
ODT / MR1 bits [A6, A2]	disabled / [0,0]	disabled / [0,0]	disabled / [0,0]
Burst length	8 fixed / MR0 Bits [A1, A0] = {0,0}	8 fixed / MR0 Bits [A1, A0] = {0,0}	8 fixed / MR0 Bits [A1, A0] = {0,0}
Active banks	all	all	all, rotational
Idle banks	none	none	none
Precharge Power Down Mode / Mode Register Bit	n.a.	n.a.	n.a.



< Figure 3. IDD4R Example > (DDR3-800-555, 512Mb x8): data DQ is shown but the output buffer should be switched off (per MR1 Bit A12="1") to achieve Iout = 0mA. Address inputs are split into 3 parts.

Table 9 — IDD7 Pattern for different Speed Grades and different tRRD, tFAW conditions

Speed	Bin	Org.	tFAW	tFAW	tRRD	tRRD	IDD7 Pattern[a]
Mb/s			[ns]	[CLK]	[ns]	[CLK]	(Note this entire sequence is repeated.)
800	all	x4/x8	40	16	10	4	A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D A4 RA4 D D A5 RA5 D D A6 RA6 D D A7 RA7 D D
	all	x16	50	20	10	4	A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D D A4 RA4 D D A5 RA5 D D A6 RA6 D D A7 RA7 D D D D D D
1066	all	x4/x8	37.5	20	7.5	4	A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D D A4 RA4 D D A5 RA5 D D A6 RA6 D D A7 RA7 D D D D D D
	all	x16	50	27	10	6	A0 RA0 D D D D A1 RA1 D D D D A2 RA2 D D D D A3 RA3 D D D D D D D A4 RA4 D D D D A5 RA5 D D D D A6 RA6 D D D D A7 RA7 D D D D D D D
1333	all	x4/x8	30	20	6	4	A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D D A4 RA4 D D A5 RA5 D D A6 RA6 D D A7 RA7 D D D D D D
	all	x16	45	30	7.5	5	A0 RA0 D D D A1 RA1 D D D A2 RA2 D D D A3 RA3 D D D D D D D D D D A4 RA4 D D D A5 RA5 D D D A6 RA6 D D D A7 RA7 D D D D D D D D D D D D
1600	all	x4/x8	30	24	6	5	A0 RA0 D D D A1 RA1 D D D A2 RA2 D D D A3 RA3 D D D D D D A4 RA4 D D D A5 RA5 D D D A6 RA6 D D D A7 RA7 D D D D D D D
	all	x16	40	32	7.5	6	A0 RA0 D D D D A1 RA1 D D D D A2 RA2 D D D D A3 RA3 D D D D D D D D D D D D A4 RA4 D D D D A5 RA5 D D D D A6 RA6 D D D D A7 RA7 D D D D D D D D D D D

a. A0 = Activation of Bank 0; RA0 = Read with Auto-Precharge of Bank 0; D = Deselect

Table 10 — IDD Measurement Conditions for IDD5B

Current	I_{DD5B}
Name	**Burst Refresh Current**
Measurement Condition	
CKE	HIGH
External Clock	on
t_{CK}	t_{CKmin}(IDD)
t_{RC}	n.a.
t_{RAS}	n.a.
t_{RCD}	n.a.
t_{RRD}	n.a.
t_{RFC}	t_{RFCmin}(IDD)
CL	n.a.
AL	n.a.
$\overline{CS}$	HIGH btw. valid cmds
Addr. and cmd Inputs	SWITCHING
Data inputs	SWITCHING
Output Buffer DQ,DQS / MR1 bit A12	off / 1
ODT / MR1 bits [A6, A2]	disabled / [0,0]
Burst length	n.a.
Active banks	Refresh command every tRFC=tRFCmin
Idle banks	none
Precharge Power Down Mode / Mode Register Bit	n.a.

Table 11 — IDD Measurement Conditions for IDD6 and IDD6ET

Current	I_{DD6}	I_{DD6ET}
Name	**Self-Refresh Current Normal Temperature Range** T_{CASE} = 0 .. 85 °C	**Self-Refresh Current Extended Temperature Range** [a] T_{CASE} = 0 .. 95 °C
Measurement Condition		
Temperature	T_{CASE} = 85 °C	T_{CASE} = 95 °C
Auto Self Refresh (ASR) / MR2 Bit A6	Disabled / "0"	Disabled / "0"
Self Refresh Temperature Range (SRT) / MR2 Bit A7	Normal / "0"	Extended / "1"
CKE	LOW	LOW
External Clock	OFF; CK and $\overline{CK}$ at LOW	OFF; CK and $\overline{CK}$ at LOW
t_{CK}	n.a.	n.a.
t_{RC}	n.a.	n.a.
t_{RAS}	n.a.	n.a.
t_{RCD}	n.a.	n.a.
t_{RRD}	n.a.	n.a.
CL	n.a.	n.a.
AL	n.a.	n.a.
$\overline{CS}$	FLOATING	FLOATING
Command Inputs ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	FLOATING	FLOATING
Row, Colum Addresses	FLOATING	FLOATING
Bank Addresses	FLOATING	FLOATING
Data I/O	FLOATING	FLOATING
Output Buffer DQ,DQS / MR1 bit A12	off / 1	off / 1
ODT / MR1 bits [A6, A2]	disabled / [0,0]	disabled / [0,0]
Burst length	n.a.	n.a.
Active banks	all during self-refresh actions	all during self-refresh actions
Idle banks	all btw. Self-Refresh actions	all btw. Self-Refresh actions
Precharge Power Down Mode / MR0 bit A12	n.a.	n.a.

a. Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if DDR3 SDRAM devices support the following options or requirements referred to in this material.

6. Electrical Characteristics and AC Timing

6.1 Refresh Parameters by Device Density

Parameter	Symbol		512Mb	1Gb	2Gb	4Gb	8Gb	Units
REF command to ACT or REF command time	tRFC		90	110	160	300	350	ns
Average periodic refresh interval	tREFI	0 ×C < T_{CASE} < 85 ×C	7.8	7.8	7.8	7.8	7.8	ms
		85 ×C < T_{CASE} < 95 ×C	3.9	3.9	3.9	3.9	3.9	ms

6.2 DDR3 SDRAM Standard Speed Bins include tCK, tRCD, tRP, tRAS and tRC for each corresponding bin

DDR3 800 Speed Bin			DDR3-800D		DDR3-800E		Unit	Notes
CL - nRCD - nRP			5-5-5		6-6-6			
Parameter		Symbol	min	max	min	max		
Internal read command to first data		t_{AA}	12.5	20	15	20	ns	
ACT to internal read or write delay time		t_{RCD}	12.5	—	15	—	ns	
PRE command period		t_{RP}	12.5	—	15	—	ns	
ACT to ACT or REF command period		t_{RC}	50	—	52.5	—	ns	
ACT to PRE command period		t_{RAS}	37.5	9 * tREFI	37.5	9 * tREFI	ns	
CL = 5	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	Reserved		ns	1)2)3)4)
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	2.5	3.3	ns	1)2)3)
Supported CL Settings			5, 6		6		n_{CK}	
Supported CWL Settings			5		5		n_{CK}	

DDR3 1066 Speed Bin			DDR3-1066E		DDR3-1066F		DDR3-1066G		Unit	Note
CL - nRCD - nRP			6-6-6		7-7-7		8-8-8			
Parameter		Symbol	min	max	min	max	min	max		
Internal read command to first data		t_{AA}	11.25	20	13.125	20	15	20	ns	
ACT to internal read or write delay time		t_{RCD}	11.25	—	13.125	—	15	—	ns	
PRE command period		t_{RP}	11.25	—	13.125	—	15	—	ns	
ACT to ACT or REF command period		t_{RC}	48.75	—	50.625	—	52.5	—	ns	
ACT to PRE command period		t_{RAS}	37.5	9 * tREFI	37.5	9 * tREFI	37.5	9 * tREFI	ns	
CL = 5	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	Reserved		Reserved		ns	1)2)3)4)6)
	CWL = 6	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		ns	4)
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	2.5	3.3	2.5	3.3	ns	1)2)3)6)
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	Reserved		Reserved		ns	1)2)3)4)
CL = 7	CWL = 5	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		ns	4)
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	1.875	< 2.5	Reserved		ns	1)2)3)4)
CL = 8	CWL = 5	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		ns	4)
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	1.875	< 2.5	1.875	< 2.5	ns	1)2)3)
Supported CL Settings			5, 6, 7, 8		6, 7, 8		6, 8		n_{CK}	
Supported CWL Settings			5, 6		5, 6		5, 6		n_{CK}	

DDR3 1333 Speed Bin			DDR3-1333F (optional)		DDR3-1333G		DDR3-1333H		DDR3-1333J (optional)		Unit	Note
CL - nRCD - nRP			7-7-7		8-8-8		9-9-9		10-10-10			
Parameter		Symbol	min	max	min	max	min	max	min	max		
Internal read command to first		t_{AA}	10.5	20	12	20	13.5	20	15	20	ns	
ACT to internal read or write delay time		t_{RCD}	10.5	—	12	—	13.5	—	15	—	ns	
PRE command period		t_{RP}	10.5	—	12	—	13.5	—	15	—	ns	
ACT to ACT or REF command period		t_{RC}	46.5	—	48	—	49.5	—	51	—	ns	
ACT to PRE command period		t_{RAS}	36	9 * tREFI	36	9 * tREFI	36	9 * tREFI	36	9 * tREFI	ns	
CL = 5	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	2.5	3.3	Reserved		Reserved		ns	1,2,3,4,7
	CWL = 6, 7	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	2.5	3.3	2.5	3.3	2.5	3.3	ns	1,2,3,7
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	Reserved		Reserved		Reserved		ns	1,2,3,4,7
	CWL = 7	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
CL = 7	CWL = 5	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	1.875	< 2.5	Reserved		Reserved		ns	1,2,3,4,7
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	Reserved		Reserved		Reserved		ns	1,2,3,4
CL = 8	CWL = 5	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	1.875	< 2.5	1.875	< 2.5	1.875	< 2.5	ns	1,2,3,7
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	1.5	<1.875	Reserved		Reserved		ns	1,2,3,4
CL = 9	CWL = 5, 6	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	1.5	<1.875	1.5	<1.875	Reserved		ns	1,2,3,4
CL = 10	CWL = 5, 6	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	1.5	<1.875	1.5	<1.875	1.5	<1.875	ns	1,2,3
			(Optional)		(Optional)		(Optional)				ns	5
Supported CL Settings			5, 6, 7, 8, 9		5, 6, 7, 8, 9		6, 8, 9		6, 8, 10		n_{CK}	
Supported CWL Settings			5, 6, 7		5, 6, 7		5, 6, 7		5, 6, 7		n_{CK}	

Speed Bin Table Notes

Absolute Specification (T_{OPER}; V_{DDQ} = V_{DD} = 1.5V +/- 0.075 V);

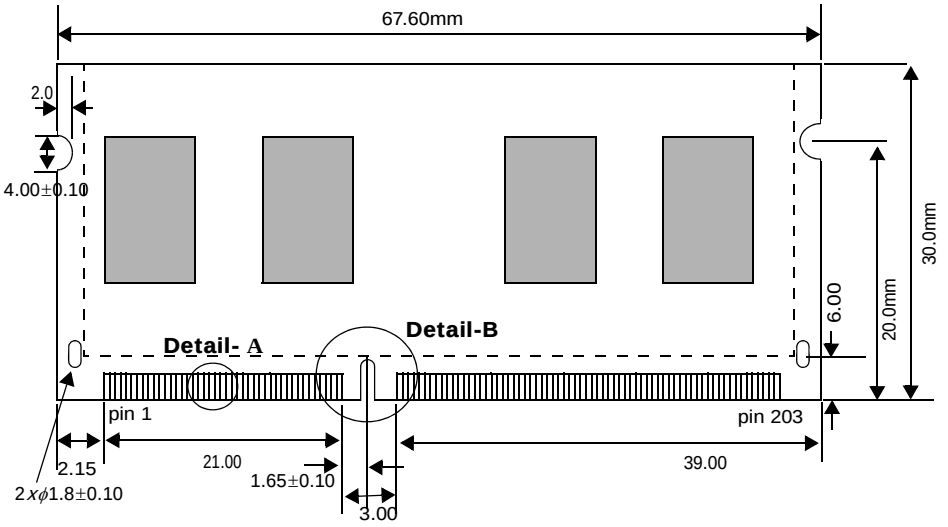
Notes:

1. The CL setting and CWL setting result in tCK(AVG).MIN and tCK(AVG).MAX requirements. When making a selection of tCK(AVG), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2. tCK(AVG).MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard tCK(AVG) value (2.5, 1.875, 1.5, or 1.25 ns) when calculating CL [nCK] = tAA [ns] / tCK(AVG) [ns], rounding up to the next 'Supported CL'.
3. tCK(AVG).MAX limits: Calculate tCK(AVG) = tAA.MAX / CLSELECTED and round the resulting tCK(AVG) down to the next valid speed bin (i.e. 3.3ns or 2.5ns or 1.875 ns or 1.25 ns). This result is tCK(AVG).MAX corresponding to CLSELECTED.
4. 'Reserved' settings are not allowed. User must program a different value.
5. 'Optional' settings allow certain devices in the industry to support this setting, however, it is not a mandatory feature. Refer to supplier's data sheet and SPD information if and how this setting is supported.
6. Any DDR3-1066 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
7. Any DDR3-1333 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.

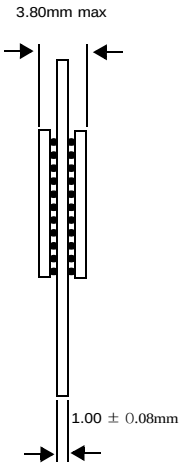
7. DIMM Outline Diagram

7.1 64Mx64 - HMT164S6AFP(R)6C

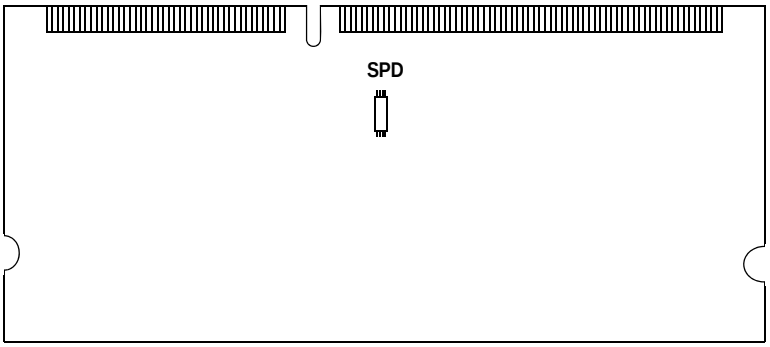
Front View



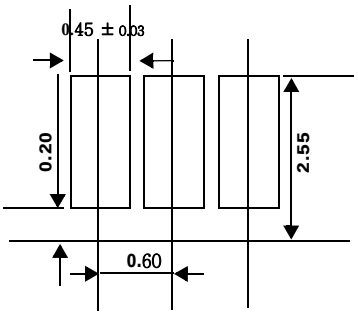
Side



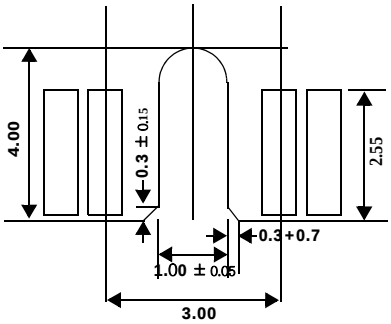
Rear View



Detail of Contacts A

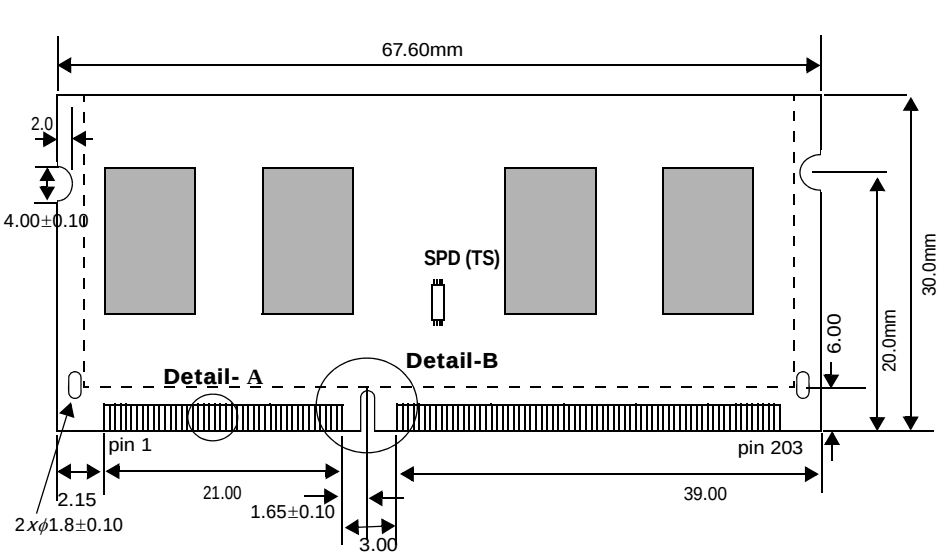


Detail of Contacts B



64Mx64 - HMT164S6AFP(R)6C (with temperature sensor)

Front View



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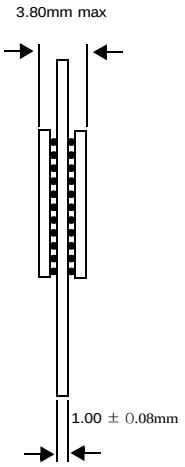
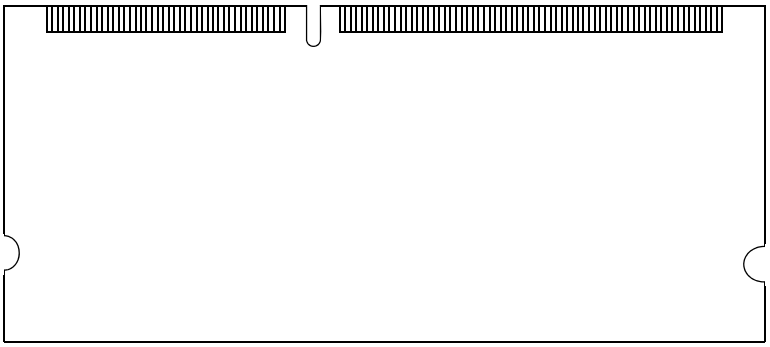
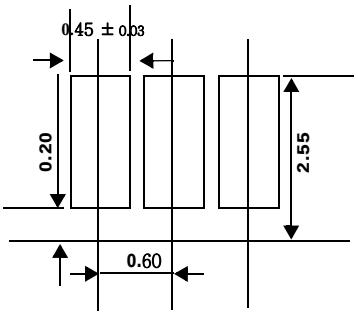


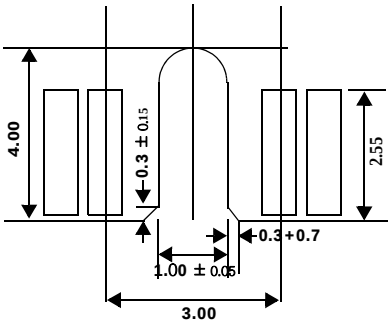
Rear View



Detail of Contacts A

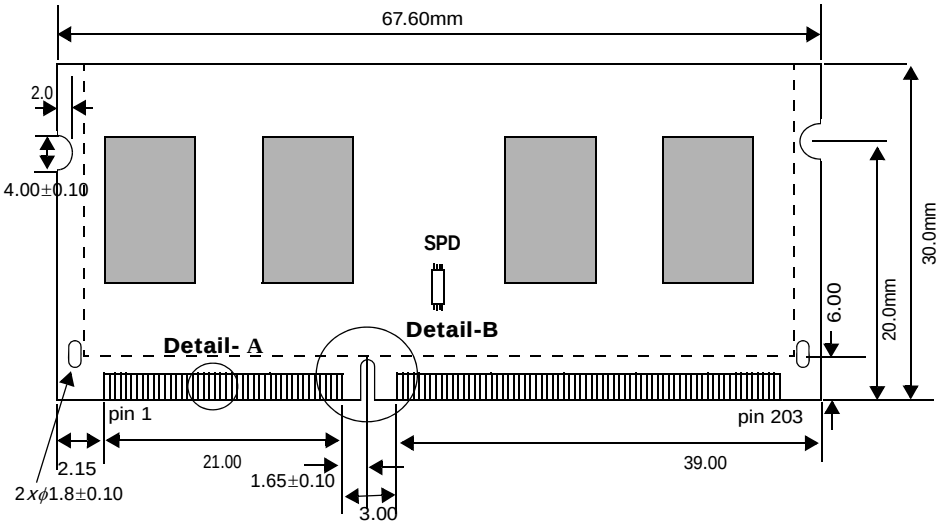


Detail of Contacts B

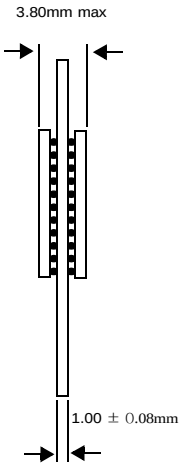


7.2 128Mx64 - HMT112S6AFP(R)6C

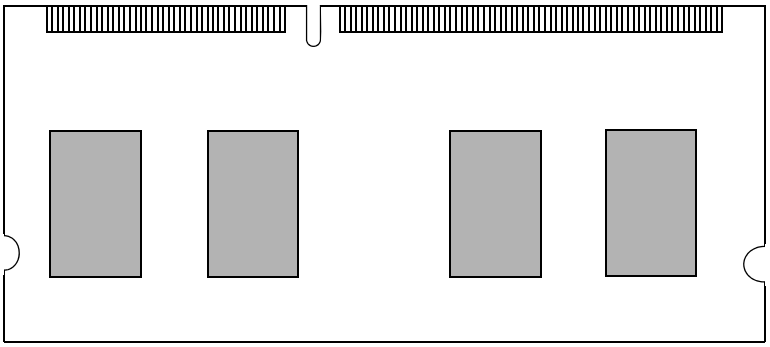
Front View



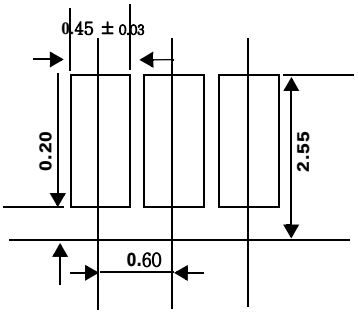
Side



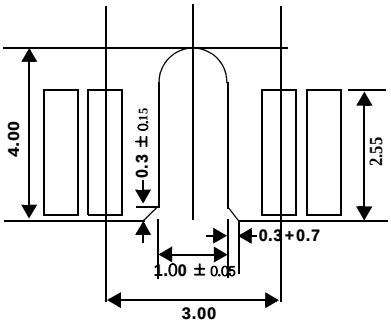
Rear View



Detail of Contacts A

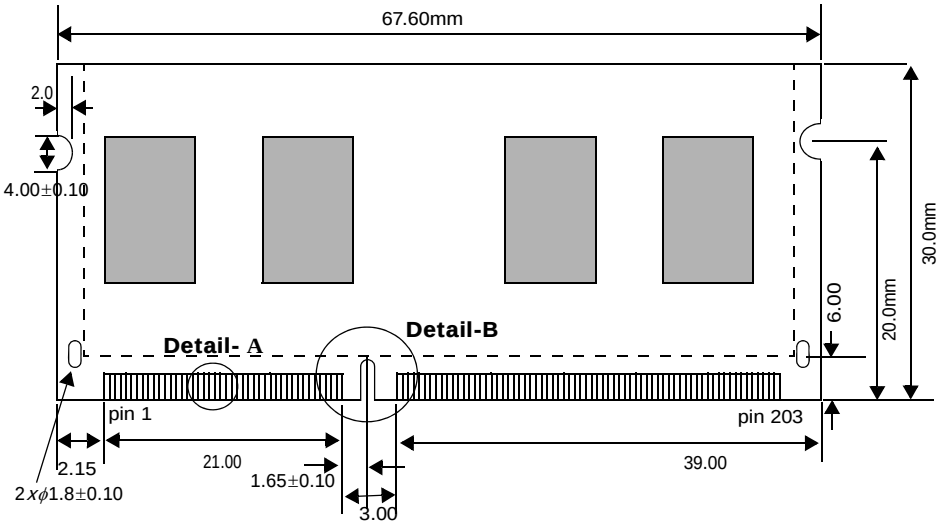


Detail of Contacts B

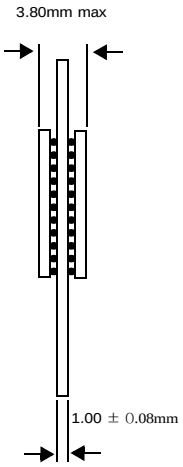


128Mx64 - HMT112S6AFP(R)6C (with temperature sensor)

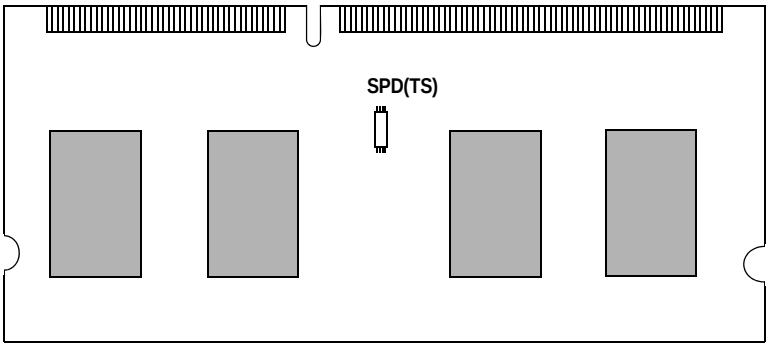
Front View



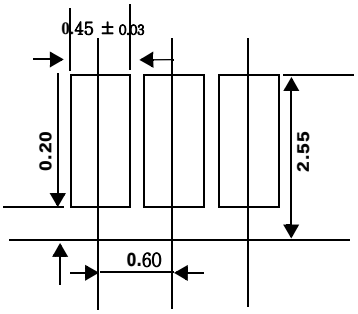
Side



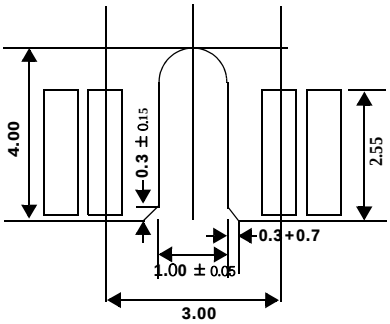
Rear View



Detail of Contacts A

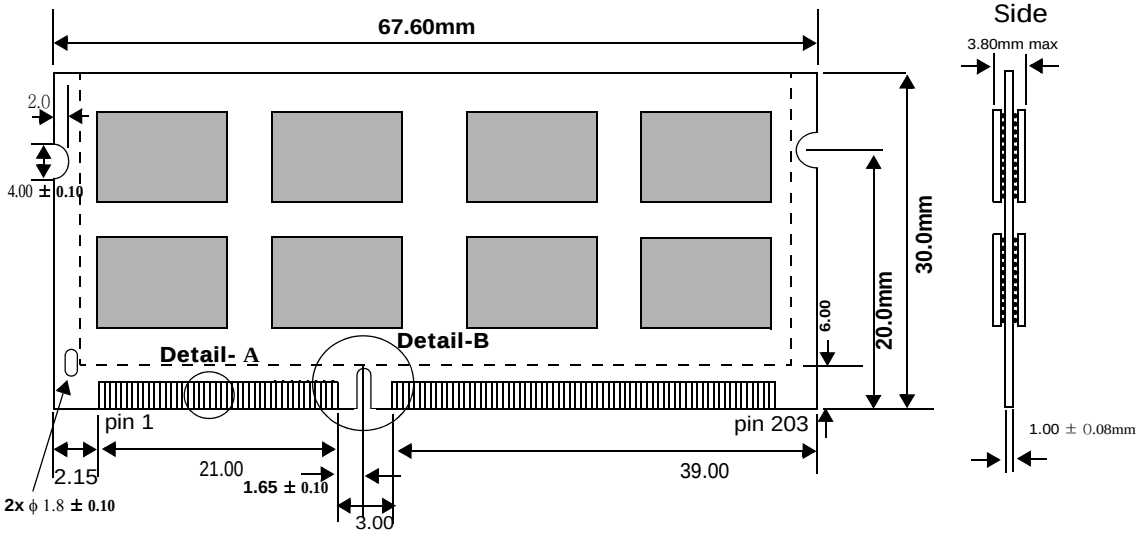


Detail of Contacts B

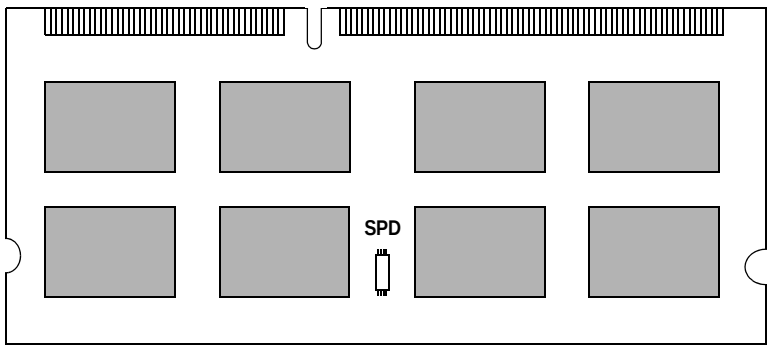


7.3 256Mx64 - HMT125S6AFP(R)8C

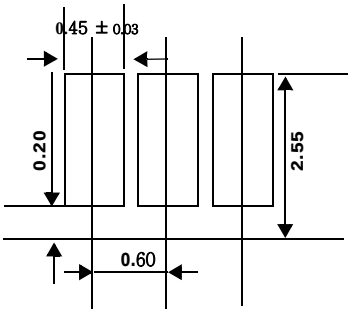
Front View



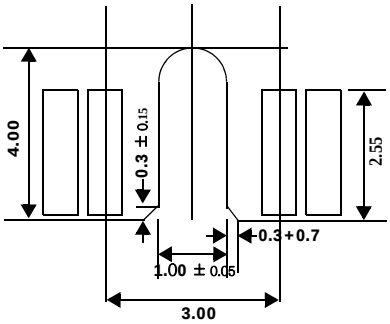
Rear View



Detail of Contacts A

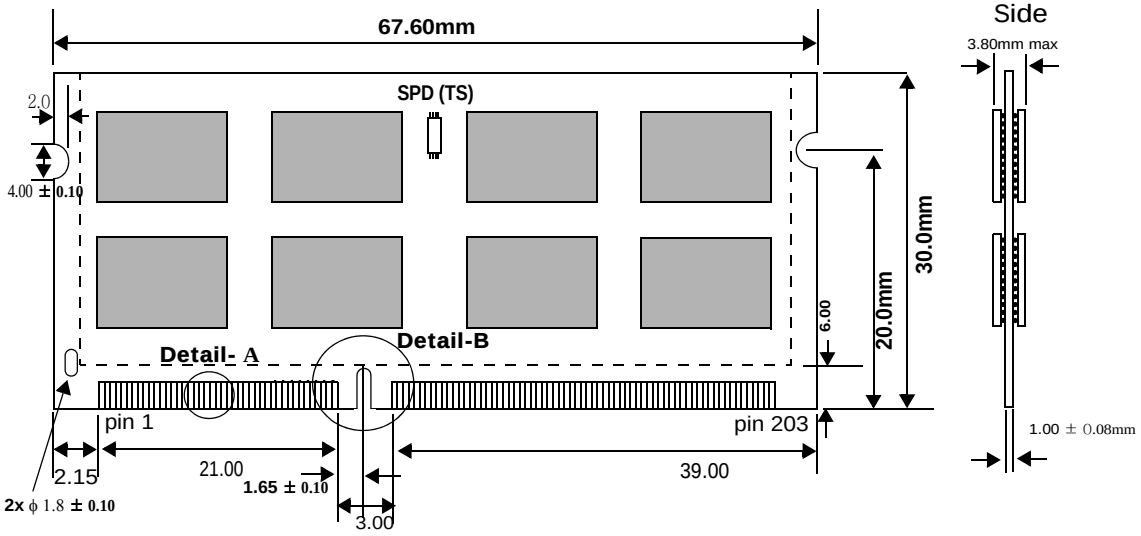


Detail of Contacts B

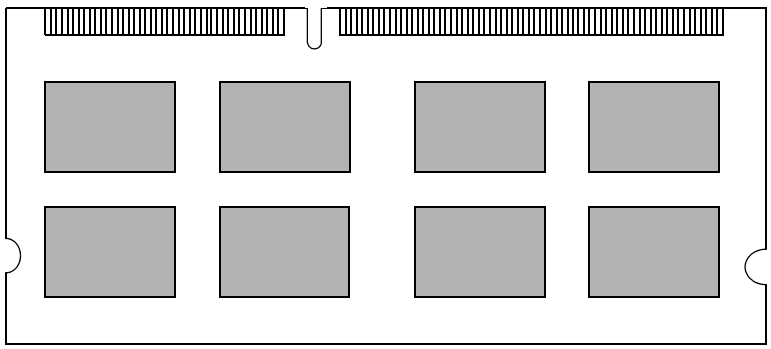


256Mx64 - HMT125S6AFP(R)8C (with temperature sensor)

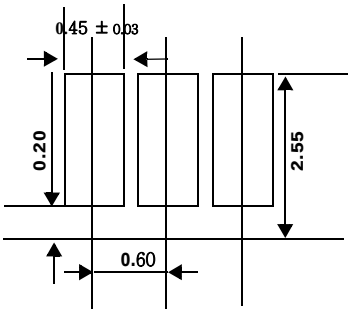
Front View



Rear View



Detail of Contacts A



Detail of Contacts B