240pin DDR2 SDRAM Unbuffered DIMMs based on 2Gb A version

This Hynix unbuffered Dual In-Line Memory Module (DIMM) series consists of 2Gb A version DDR2 SDRAMs in Fine Ball Grid Array (FBGA) packages on a 240pin glass-epoxy substrate. This Hynix 2Gb version A based DDR2 Unbuffered DIMM series provide a high performance 8 byte interface in 133.35mm width form factor of industry standard. It is suitable for easy interchange and addition.

FEATURES

- JEDEC standard Double Data Rate2 Synchronous DRAMs (DDR2 SDRAMs) with 1.8V +/- 0.1V Power Supply
- All inputs and outputs are compatible with SSTL_1.8 interface
- 8 Bank architecture
- Posted CAS
- Programmable CAS Latency 3,4,5, 6
- OCD (Off-Chip Driver Impedance Adjustment)
- ODT (On-Die Termination)
- Fully differential clock operations (CK & $\overline{CK}$)
- Programmable Burst Length 4 / 8 with both sequential and interleave mode
- Auto refresh and self refresh supported
- 8192 refresh cycles / 64ms
- Serial presence detect with EEPROM
- DDR2 SDRAM Package:
  60ball FBGA(256Mx8)
- 133.35 x 30.00 mm form factor
- RoHS compliant

ORDERING INFORMATION

Part Name	Density	Org.	# of DRAMs	# of ranks	Materials	ECC
HMP351U6AFR8C - Y5/S5/S6	4GB	512Mx64	16	2	Halogen-free	None
HMP351U7AFR8C - Y5/S5/S6	4GB	512Mx72	18	2	Halogen-free	ECC

SPEED GRADE & KEY PARAMETERS

	Y5 (DDR2-667)	S6 (DDR2-800)	S5 (DDR2-800)	Unit
Speed @CL3	400	400	400	Mbps
Speed @CL4	533	533	533	Mbps
Speed @CL5	667	800	800	Mbps
Speed @CL6	-	800	800	Mbps
CL-tRCD-tRP	5-5-5	6-6-6	5-5-5	tCK

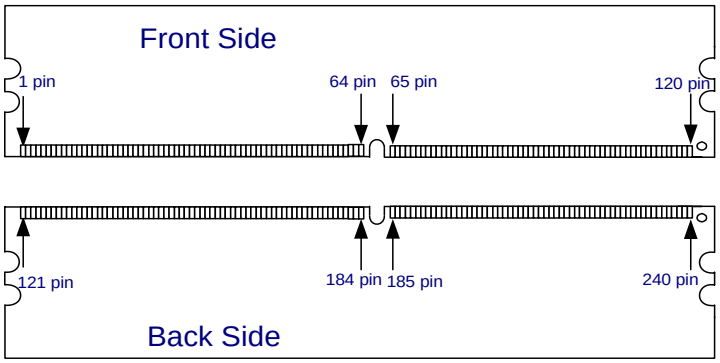
ADDRESS TABLE

Density	Organization	Ranks	SDRAMs	# of DRAMs	# of row/bank/column Address	Refresh Method
4GB	512M x 64	2	256Mb x 8	16	14(A0~A13)/3(BA0~BA2)/10(A0~A9)	8K / 64ms
4GB	512M x 72	2	256Mb x 8	18	14(A0~A13)/3(BA0~BA2)/10(A0~A9)	8K / 64ms

Input/Output Functional Description

Symbol	Type	Polarity	Pin Description
CK[2:0], $\overline{CK}$[2:0]	SSTL	Differential Crossing	CK and /CK are differential clock inputs. All the DDR2 SDRAM addr/cntl inputs are sampled on the crossing of positive edge of CK and negative edge of /CK. Output(read) data is reference to the crossing of CK and /CK (Both directions of crossing)
CKE[1:0]	SSTL	Active High	Activates the DDR2 SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode or the Self Refresh mode.
$\overline{S}$[1:0]	SSTL	Active Low	Enables the associated DDR2 SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. Rank 0 is selected by $\overline{S}$0; Rank 1 is selected by $\overline{S}$1
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	SSTL	Active Low	/RAS,/CAS and /WE(ALONG WITH S) define the command being entered.
ODT[1:0]	SSTL	Active High	Asserts on-die termination for DQ, DM, DQS and $\overline{DQS}$ signals if enabled via the DDR2 SDRAM mode register.
Vref	Supply		Reference voltage for SSTL18 inputs
V_{DDQ}	Supply		Power supplies for the DDR2 SDRAM output buffers to provide improved noise immunity. For all current DDR2 unbuffered DIMM designs, V_{DDQ} shares the same power plane as V_{DD} pins.
BA[2:0]	SSTL	-	Selects which DDR2 SDRAM internal bank of four or eight is activated.
A[9:0], A10/AP, A[13:11]	SSTL	-	During a Bank Activate command cycle, Address input defines the row address(RA0~RA15) During a Read or Write command cycle, Address input defines the column address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{CK}$. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high., autoprecharge is selected and BA0-BAn defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle., AP is used in conjunction with BA0-BAn to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0-BAn inputs. If AP is low, then BA0-BAn are used to define which bank to precharge.
DQ[63:0], CB[7:0]	SSTL	-	Data and Check Bit Input/Output pins.
DM[8:0]	SSTL	Active High	DM is an input mask signal for write data. Input data is masked when DM is sampled High coincident with that input data during a write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading.
V_{DD},V_{SS}	Supply		Power and ground for the DDR2 SDRAM input buffers, and core logic. V_{DD} and V_{DDQ} pins are tied to V_{DD}/V_{DDQ} planes on these modules.
DQS[8:0], $\overline{DQS}$[8:0]	SSTL	Differential crossing	Data strobe for input and output data. For Rawcards using x16 organized DRAMs, DQ0~7 connect to the LDQS pin of the DRAMs and DQ8~15 connect to the UDQS pin of the DRAM
SA[2:0]		-	These signals are tied at the system planar to either V_{SS} or V_{DD} to configure the serial SPD EEPROM.
SDA		-	This is a bidirectional pin used to transfer data into or out of the SPD EEPROM. A resister must be connected to V_{DD} to act as a pull up.
SCL		-	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from SCL to V_{DD} to act as a pull up on the system board.
VDDSPD	Supply		Power supply for SPD EEPROM. This supply is separate from the VDD/VDDQ power plane. EEPROM supply is operable from 1.7V to 3.6V.

PIN CONFIGURATION



PIN ASSIGNMENT

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VREF	41	VSS	81	DQ33	121	VSS	161	NC(CB4)*	201	VSS
2	VSS	42	NC(CB0)*	82	VSS	122	DQ4	162	NC(CB5)*	202	DM4
3	DQ0	43	NC(CB1)*	83	$\overline{DQS4}$	123	DQ5	163	VSS	203	NC
4	DQ1	44	VSS	84	DQS4	124	VSS	164	NC(DM8)*	204	VSS
5	VSS	45	NC($\overline{DQS8}$)*	85	VSS	125	DM0	165	NC	205	DQ38
6	$\overline{DQS0}$	46	NC(DQS8)*	86	DQ34	126	NC	166	VSS	206	DQ39
7	DQS0	47	VSS	87	DQ35	127	VSS	167	NC(CB6)*	207	VSS
8	VSS	48	NC(CB2)*	88	VSS	128	DQ6	168	NC(CB7)*	208	DQ44
9	DQ2	49	NC(CB3)*	89	DQ40	129	DQ7	169	VSS	209	DQ45
10	DQ3	50	VSS	90	DQ41	130	VSS	170	VDDQ	210	VSS
11	VSS	51	VDDQ	91	VSS	131	DQ12	171	CKE1	211	DM5
12	DQ8	52	CKE0	92	$\overline{DQS5}$	132	DQ13	172	VDD	212	NC
13	DQ9	53	VDD	93	DQS5	133	VSS	173	A15	213	VSS
14	VSS	54	BA2	94	VSS	134	DM1	174	A14	214	DQ46
15	$\overline{DQS1}$	55	NC	95	DQ42	135	NC	175	VDDQ	215	DQ47
16	DQS1	56	VDDQ	96	DQ43	136	VSS	176	A12	216	VSS
17	VSS	57	A11	97	VSS	137	CK1	177	A9	217	DQ52
18	NC	58	A7	98	DQ48	138	$\overline{CK1}$	178	VDD	218	DQ53
19	NC	59	VDD	99	DQ49	139	VSS	179	A8	219	VSS
20	VSS	60	A5	100	VSS	140	DQ14	180	A6	220	CK2
21	DQ10	61	A4	101	SA2	141	DQ15	181	VDDQ	221	$\overline{CK2}$
22	DQ11	62	VDDQ	102	NC,TEST[1]	142	VSS	182	A3	222	VSS

* The pin names in parenthesizes are applied to DIMM with ECC only.

PIN ASSIGNMENT(Continued)

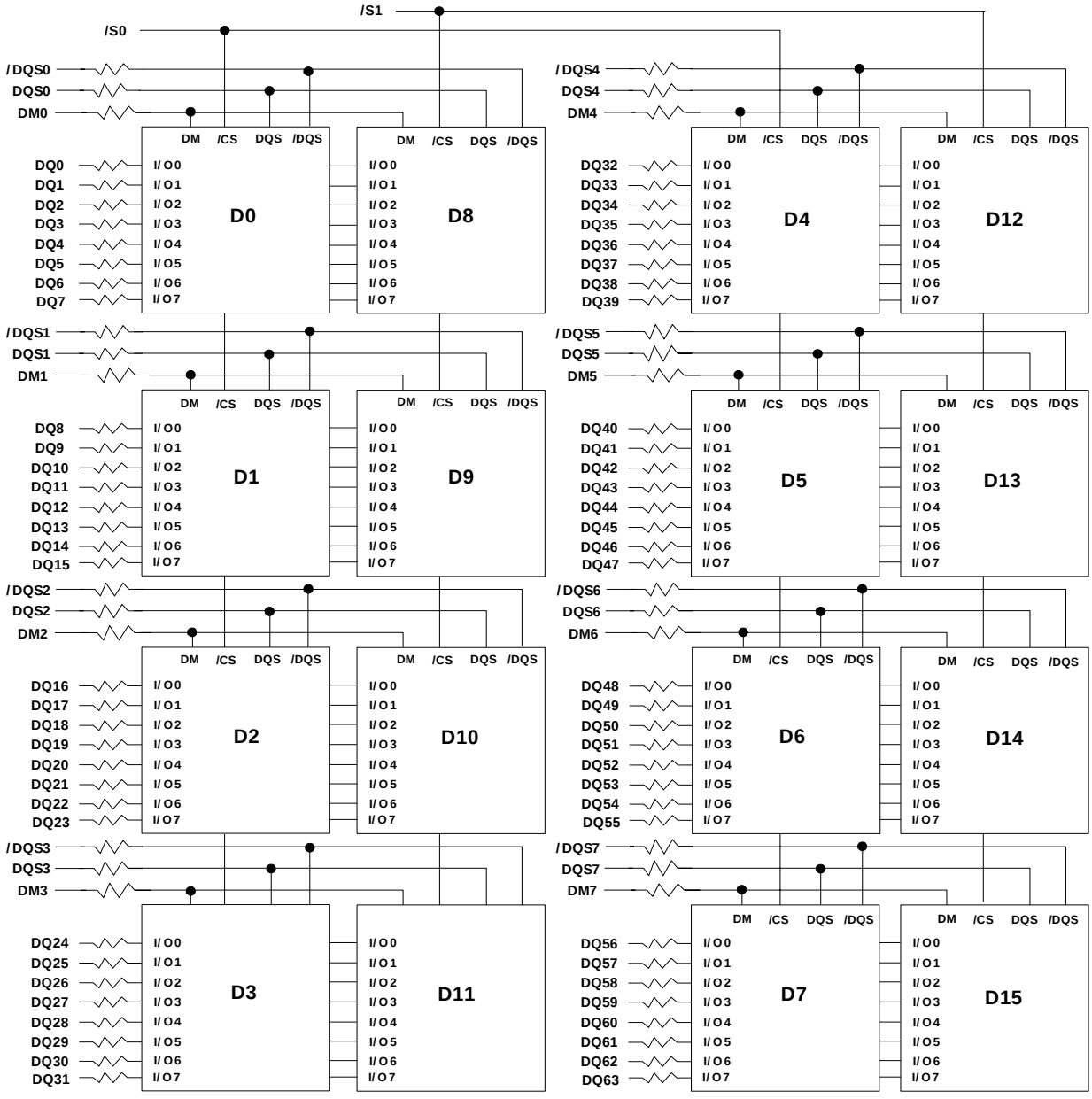
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
23	VSS	63	A2	103	VSS	143	DQ20	183	A1	223	DM6
24	DQ16	64	VDD	104	$\overline{DQS}$6	144	DQ21	184	VDD	224	NC
25	DQ17	65	VSS	105	DQS6	145	VSS	185	CK0	225	VSS
26	VSS	66	VSS	106	VSS	146	DM2	186	$\overline{CK}$0	226	DQ54
27	$\overline{DQS}$2	67	VDD	107	DQ50	147	NC	187	VDD	227	DQ55
28	DQS2	68	NC	108	DQ51	148	VSS	188	A0	228	VSS
29	VSS	69	VDD	109	VSS	149	DQ22	189	VDD	229	DQ60
30	DQ18	70	A10/AP	110	DQ56	150	DQ23	190	BA1	230	DQ61
31	DQ19	71	BA0	111	DQ57	151	VSS	191	VDDQ	231	VSS
32	VSS	72	VDDQ	112	VSS	152	DQ28	192	$\overline{RAS}$	232	DM7
33	DQ24	73	$\overline{WE}$	113	$\overline{DQS}$7	153	DQ29	193	$\overline{S}$0	233	NC
34	DQ25	74	$\overline{CAS}$	114	DQS7	154	VSS	194	VDDQ	234	VSS
35	VSS	75	VDDQ	115	VSS	155	DM3	195	ODT0	235	DQ62
36	$\overline{DQS}$3	76	$\overline{S}$1	116	DQ58	156	NC	196	A13	236	DQ63
37	DQS3	77	ODT1	117	DQ59	157	VSS	197	VDD	237	VSS
38	VSS	78	VDDQ	118	VSS	158	DQ30	198	VSS	238	VDDSPD
39	DQ26	79	VSS	119	SDA	159	DQ31	199	DQ36	239	SA0
40	DQ27	80	DQ32	120	SCL	160	VSS	200	DQ37	240	SA1

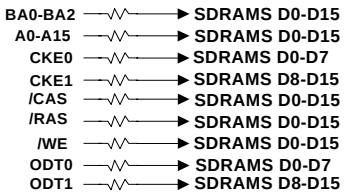
*NC=No connect

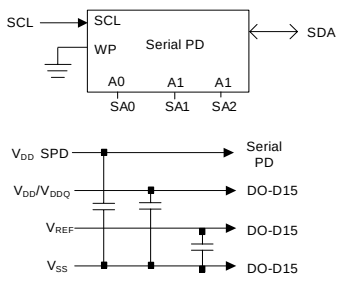
Notes:

1. The TEST pin is reserved for bus analysis tools and is not connected on standard memory module products (DIMMs).
2. NC Pins should not be connected to anything, including bussing within the NC group.

FUNCTIONAL BLOCK DIAGRAM
4GB(512Mbx64) - HMP351U6AFR8C





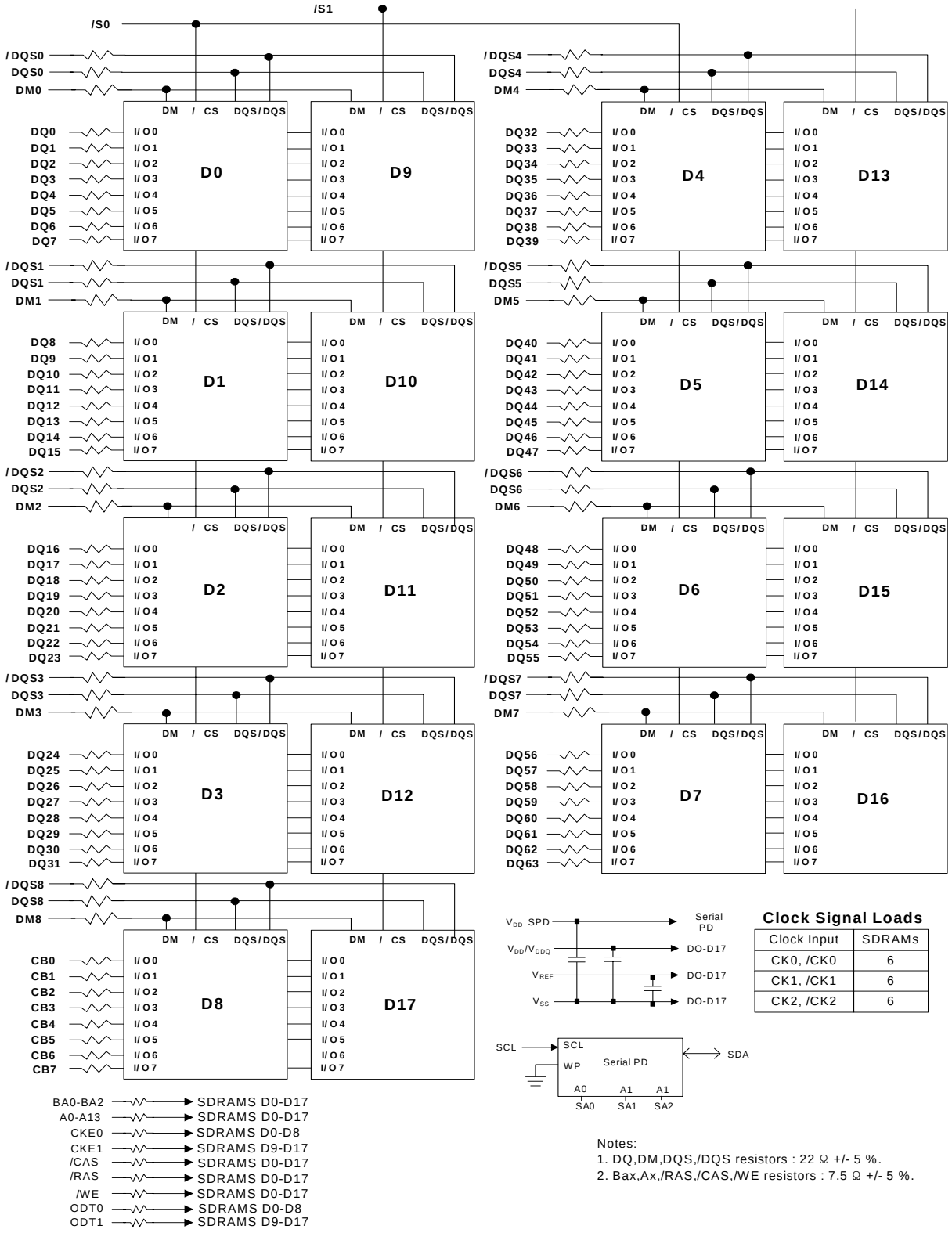


Clock Signal Loads

Clock Input	SDRAMs
CK0, /CK0	4
CK1, /CK1	6
CK2, /CK2	6

Notes:
1. DQ,DM,DQS,/DQS resistors : 22 Ω +/- 5 %.
2. Bax,Ax,/RAS,/CAS,/WE resistors : 7.5 Ω +/- 5 %.

FUNCTIONAL BLOCK DIAGRAM
4GB(512Mbx72) - HMP351U7AFR8C



Clock Signal Loads

Clock Input	SDRAMs
CK0, /CK0	6
CK1, /CK1	6
CK2, /CK2	6

Notes:
1. DQ,DM,DQS,/DQS resistors : 22 Ω +/- 5 %.
2. Bax,Ax,/RAS,/CAS,/WE resistors : 7.5 Ω +/- 5 %.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit	Note
Voltage on V_{DD} pin relative to Vss	V_{DD}	- 1.0 ~ 2.3	V	1
Voltage on V_{DDQ} pin relative to Vss	V_{DDQ}	- 0.5 ~ 2.3	V	1
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	- 0.5 ~ 2.3	V	1

Operation Conditions and Environmental Parameters

Parameter	Symbol	Rating	Units	Notes
DIMM Operating temperature(ambient)	T_{OPR}	0 ~ +55	^{o}C	
Storage Temperature	T_{STG}	-50 ~ +100	^{o}C	1
Storage Humidity(without condensation)	H_{STG}	5 to 95	%	1
DIMM Barometric Pressure(operating & storage)	P^{BAR}	105 to 69	K Pascal	2
DRAM Component Case Temperature Range	T_{CASE}	0 ~+95	^{o}C	3

Notes:

1. Stress greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating con ditions for extended periods may affect reliability.
2. Up to 9850 ft.
3. If the DRAM case temperature is Above 85^{o}C, the Auto-Refresh command interval has to be reduced to tREFI=3.9us. For Measurement conditions of T_{CASE}, please refer to the JEDEC document JESD51-2.

DC OPERATING CONDITIONS (SSTL_1.8)

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.7	1.8	1.9	V	1
VDDL	Supply Voltage for DLL	1.7	1.8	1.9	V	1,2
VDDQ	Supply Voltage for Output	1.7	1.8	1.9	V	1,2
VREF	Input Reference Voltage	0.49*VDDQ	0.50*VDDQ	0.51*VDDQ	mV	3,4
VTT	Termination Voltage	VREF-0.04	VREF	VREF+0.04	V	5
VDDSPD	EEPROM Supply Voltage	1.7	-	3.6	V	

Notes:

1. Min. Type. and Max. values increase by 100mV for C3(DDR2-533 3-3-3) speed option.
2. VDDQ tracks with VDD,VDDL tracks with VDD. AC parameters are measured with VDD,VDDQ and VDD.
3. The value of VREF may be selected by the user to provide optimum noise margin in the system. Typically the value of VREF is expected to be about 0.5 x VDDQ of the transmitting device and VREF is expected to track variations in VDDQ.
4. Peak to peak ac noise on VREF may not exceed +/-2% VREF (dc).
5. VTT of transmitting device must track VREF of receiving device.

INPUT DC LOGIC LEVEL

Parameter	Symbol	Min	Max	Unit	Note
dc Input logic HIGH	V_{IH}(DC)	V_{REF} + 0.125	V_{DDQ} + 0.3	V	
dc Input logic LOW	V_{IL}(DC)	-0.30	V_{REF} - 0.125	V	

INPUT AC LOGIC LEVEL

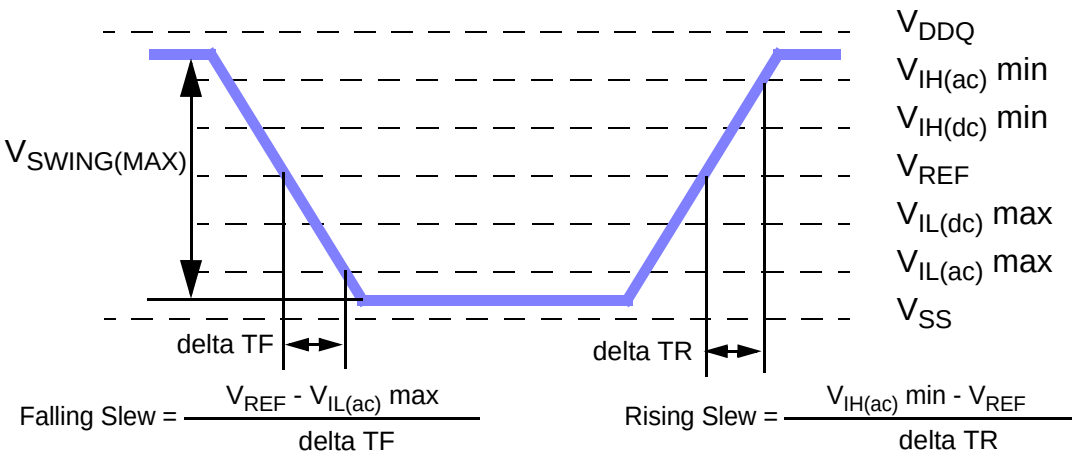
Parameter	Symbol	DDR2 667, 800		Unit	Note
		Min	Max		
AC Input logic High	V_{IH}(AC)	V_{REF} + 0.200	-	V	
AC Input logic Low	V_{IL}(AC)	-	V_{REF} - 0.200	V	

AC INPUT TEST CONDITIONS

Symbol	Condition	Value	Units	Notes
V_{REF}	Input reference voltage	0.5 * V_{DDQ}	V	1
$V_{SWING(MAX)}$	Input signal maximum peak to peak swing	1.0	V	1
SLEW	Input signal minimum slew rate	1.0	V/ns	2, 3

Notes:

1. Input waveform timing is referenced to the input signal crossing through the V_{REF} level applied to the device under test.
2. The input signal minimum slew rate is to be maintained over the range from V_{REF} to $V_{IH(ac)}$ min for rising edges and the range from V_{REF} to $V_{IL(ac)}$ max for falling edges as shown in the below figure.
3. AC timings are referenced with input waveforms switching from VIL(ac) to VIH(ac) on the positive transitions and VIH(ac) to VIL(ac) on the negative transitions.

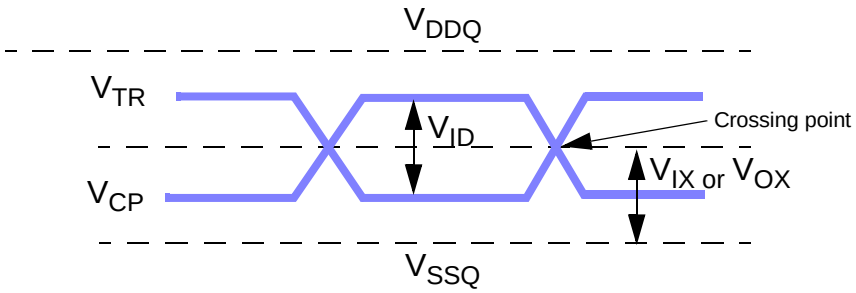


< Figure: AC Input Test Signal Waveform >

Differential Input AC logic Level

Symbol	Parameter	Min.	Max.	Units	Note
V_{ID} (ac)	ac differential input voltage	0.5	V_{DDQ} + 0.6	V	1
V_{IX} (ac)	ac differential cross point voltage	0.5 * V_{DDQ} - 0.175	0.5 * V_{DDQ} + 0.175	V	2

1. V_{IN}(DC) specifies the allowable DC execution of each input of differential pair such as CK, $\overline{CK}$, DQS, $\overline{DQS}$, LDQS, $\overline{LDQS}$, UDQS and $\overline{UDQS}$.
2. V_{ID}(DC) specifies the input differential voltage |V_{TR} -V_{CP} | required for switching, where V_{TR} is the true input (such as CK, DQS, LDQS or UDQS) level and V_{CP} is the complementary input (such as $\overline{CK}$, $\overline{DQS}$, $\overline{LDQS}$ or $\overline{UDQS}$) level. The minimum value is equal to V_{IH}(DC) - V_{IL}(DC).



< Differential signal levels >

Notes:

1. V_{ID}(AC) specifies the input differential voltage |V_{TR} -V_{CP} | required for switching, where V_{TR} is the true input signal (such as CK, DQS, LDQS or UDQS) and V_{CP} is the complementary input signal (such as $\overline{CK}$, $\overline{DQS}$, $\overline{LDQS}$ or $\overline{UDQS}$). The minimum value is equal to V_{IH}(AC) - V_{IL}(AC).
2. The typical value of V_{IX}(AC) is expected to be about 0.5 * V_{DDQ} of the transmitting device and V_{IX}(AC) is expected to track variations in V_{DDQ}. V_{IX}(AC) indicates the voltage at which differential input signals must cross.

DIFFERENTIAL AC OUTPUT PARAMETERS

Symbol	Parameter	Min.	Max.	Units	Note
V_{OX} (ac)	ac differential cross point voltage	0.5 * V_{DDQ} - 0.125	0.5 * V_{DDQ} + 0.125	V	1

Note:

1. The typical value of V_{OX}(AC) is expected to be about 0.5 * V_{DDQ} of the transmitting device and V_{OX}(AC) is expected to track variations in V_{DDQ}. V_{OX}(AC) indicates the voltage at which differential output signals must cross.

OUTPUT BUFFER LEVELS

OUTPUT AC TEST CONDITIONS

Symbol	Parameter	SSTL_18	Units	Notes
V_{OTR}	Output Timing Measurement Reference Level	0.5 * V_{DDQ}	V	1

Note:

1. The VDDQ of the device under test is referenced.

OUTPUT DC CURRENT DRIVE

Symbol	Parameter	SSTl_18	Units	Notes
$I_{OH(dc)}$	Output Minimum Source DC Current	- 13.4	mA	1, 3, 4
$I_{OL(dc)}$	Output Minimum Sink DC Current	13.4	mA	2, 3, 4

Notes:

1.V_{DDQ} = 1.7 V; V_{OUT} = 1420 mV. (V_{OUT} - V_{DDQ})/I_{OH} must be less than 21 ohm for values of V_{OUT} between V_{DDQ} and V_{DDQ} - 280 mV.

2. V_{DDQ} = 1.7 V; V_{OUT} = 280 mV. V_{OUT}/I_{OL} must be less than 21 ohm for values of V_{OUT} between 0 V and 280 mV.

3. The dc value of V_{REF} applied to the receiving device is set to V_{TT}

4. The values of I_{OH}(dc) and I_{OL}(dc) are based on the conditions given in Notes 1 and 2. They are used to test device drive current capability to ensure V_{IH} min plus a noise margin and V_{IL} max minus a noise margin are delivered to an SSTL_18 receiver. The actual current values are derived by shifting the desired driver operating point along a 21 ohm load line to define a convenient driver current for measurement.

PIN Capacitance (VDD=1.8V,VDDQ=1.8V, TA=25°C)

4GB: HMP351U6AFR8C

Pin	Symbol	Min	Max	Unit
CK, $\overline{CK}$	CCK	TBD	TBD	pF
CKE, ODT, $\overline{CS}$	CI1	TBD	TBD	pF
Address, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	CI2	TBD	TBD	pF
DQ, DM, DQS, $\overline{DQS}$	CIO	TBD	TBD	pF

4GB: HMP351U7AFR8C

Pin	Symbol	Min	Max	Unit
CK, $\overline{CK}$	CCK	TBD	TBD	pF
CKE, ODT, $\overline{CS}$	CI1	TBD	TBD	pF
Address, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	CI2	TBD	TBD	pF
DQ, DM, DQS, $\overline{DQS}$	CIO	TBD	TBD	pF

Notes:
1. Pins not under test are tied to GND.
2. These value are guaranteed by design and tested on a sample basis only.

4GB, 512M x 64 U - DIMM: HMP351U6AFR8C

Symbol	Y5 (DDR2 667@CL 5)	S6 (DDR2 800@CL 6)	Unit	Note
IDD0	1120	1200	mA	
IDD1	1200	1280	mA	
IDD2P	192	192	mA	
IDD2Q	720	800	mA	
IDD2N	800	880	mA	
IDD3P(F)	560	560	mA	
IDD3P(S)	288	288	mA	
IDD3N	1120	1280	mA	
IDD4R	2000	2360	mA	
IDD4W	1880	2200	mA	
IDD5B	2160	2280	mA	
IDD6	240	240	mA	1
IDD7	2640	2880	mA	

4GB, 512M x 72 ECC U-DIMM: HMP351U7AFR8C

Symbol	Y5 (DDR2 667@CL 5)	S6 (DDR2 800@CL 6)	Unit	Note
IDD0	1260	1350	mA	
IDD1	1350	1440	mA	
IDD2P	216	216	mA	
IDD2Q	810	900	mA	
IDD2N	900	990	mA	
IDD3P(F)	630	630	mA	
IDD3P(S)	324	324	mA	
IDD3N	1260	1440	mA	
IDD4R	2250	2655	mA	
IDD4W	2115	2475	mA	
IDD5B	2430	2565	mA	
IDD6	270	270	mA	1
IDD7	2970	3240	mA	

Note: 1. IDD6 current values are guaranteed up to Tcase of 85°C max.

IDD MEASUREMENT CONDITIONS

Symbol	Conditions		Units
IDD0	**Operating one bank active-precharge current**; ^{t}CK = ^{t}CK(IDD), ^{t}RC = ^{t}RC(IDD), ^{t}RAS = ^{t}RAS-min(IDD);CKE is HIGH, $\overline{CS}$ is HIGH between valid commands;Address bus inputs are SWITCHING;Data bus inputs are SWITCHING		mA
IDD1	**Operating one bank active-read-precharge current**; IOUT = 0mA;BL = 4, CL = CL(IDD), AL = 0; ^{t}CK = ^{t}CK(IDD), ^{t}RC = ^{t}RC (IDD), ^{t}RAS = ^{t}RASmin(IDD), ^{t}RCD = ^{t}RCD(IDD); CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W		mA
IDD2P	**Precharge power-down current**; All banks idle; ^{t}CK = ^{t}CK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		mA
IDD2Q	**Precharge quiet standby current**;All banks idle; ^{t}CK = ^{t}CK(IDD);CKE is HIGH, $\overline{CS}$ is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		mA
IDD2N	**Precharge standby current**; All banks idle; ^{t}CK = ^{t}CK(IDD); CKE is HIGH, $\overline{CS}$ is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA
IDD3P	**Active power-down current**; All banks open; ^{t}CK = ^{t}CK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Fast PDN Exit MRS(12) = 0	mA
		Slow PDN Exit MRS(12) = 1	mA
IDD3N	**Active standby current**; All banks open; ^{t}CK = ^{t}CK(IDD), ^{t}RAS = ^{t}RASmax(IDD), ^{t}RP =^{t}RP(IDD); CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA
IDD4W	**Operating burst write current**; All banks open, Continuous burst writes; BL = 4, CL = CL(IDD), AL = 0; ^{t}CK = ^{t}CK(IDD), ^{t}RAS = ^{t}RASmax(IDD), ^{t}RP = ^{t}RP(IDD); CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA
IDD4R	**Operating burst read current**; All banks open, Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; ^{t}CK = ^{t}CK(IDD), ^{t}RAS = ^{t}RASmax(IDD), ^{t}RP = ^{t}RP(IDD); CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W		mA
IDD5B	**Burst refresh current**; ^{t}CK = ^{t}CK(IDD); Refresh command at every ^{t}RFC(IDD) interval; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA
IDD6	**Self refresh current**; CK and $\overline{CK}$ at 0V; CKE ≤ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING. IDD6 current values are guaranteed up to Tcase of 85℃ max.	Normal	mA
		Low Power	
IDD7	**Operating bank interleave read current**; All bank interleaving reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = ^{t}RCD(IDD)-1*^{t}CK(IDD); ^{t}CK = ^{t}CK(IDD), ^{t}RC = ^{t}RC(IDD), ^{t}RRD = ^{t}RRD(IDD), ^{t}RCD = 1*^{t}CK(IDD); CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R; - Refer to the following page for detailed timing conditions		mA

Notes:

1. IDD specifications are tested after the device is properly initialized
2. Input slew rate is specified by AC Parametric Test Condition
3. IDD parameters are specified with ODT disabled.
4. Data bus consists of DQ, DM, DQS, $\overline{DQS}$, RDQS, $\overline{RDQS}$, LDQS, $\overline{LDQS}$, UDQS, and $\overline{UDQS}$. IDD values must be met with all combinations of EMRS bits 10 and 11.
5. Definitions for IDD
   LOW is defined as Vin ≤ VILAC (max)
   HIGH is defined as Vin ≥ VIHAC (min)
   STABLE is defined as inputs stable at a HIGH or LOW level
   FLOATING is defined as inputs at VREF = VDDQ/2
   SWITCHING is defined as:
   inputs changing between HIGH and LOW every other clock cycle (once per two clocks) for address and control signals, and inputs changing between HIGH and LOW every other data transfer (once per clock) for DQ signals not including masks or strobes.

Electrical Characteristics & AC Timings

Speed Bins and CL,tRCD,tRP,tRC and tRAS for Corresponding Bin

Speed	DDR2-800(S5)	DDR2-667(Y5)	Unit
Bin(CL-tRCD-tRP)	5-5-5	5-5-5	
Parameter	min	min	
CAS Latency	5	5	ns
tRCD	12.5	15	ns
tRP	12.5	15	ns
tRC	57.5	60	ns
tRAS	45	45	ns

AC Timing Parameters by Speed Grade

Parameter	Symbol	DDR2-667		DDR2-800		Unit	Note
		min	max	min	max		
DQ output access time from CK/$\overline{CK}$	tAC	-450	+450	-400	+400	ps	
DQS output access time from CK/$\overline{CK}$	tDQSCK	-400	+400	-350	+350	ps	
CK high-level width	tCH	0.45	0.55	0.45	0.55	tCK	
CK low-level width	tCL	0.45	0.55	0.45	0.55	tCK	
CK half period	tHP	min(tCL, tCH)	-	min(tCL, tCH)	-	ps	
Clock cycle time, CL=x	tCK	3000	8000	2500		ps	
DQ and DM input setup time (differential strobe)	tDS	100	-	50	-	ps	1
DQ and DM input hold time (differential strobe)	tDH	175	-	125	-	ps	1
Control & Address input pulse width for each input	tIPW	0.6	-	0.6	-	tCK	
DQ and DM input pulse width for each input	tDIPW	0.35	-	0.35	-	tCK	
Data-out high-impedance time from CK/$\overline{CK}$	tHZ	-	tAC max	-	tAC max	ps	
DQS low-impedance time from CK/$\overline{CK}$	tLZ(DQS)	tAC min	tAC max	tAC min	tAC max	ps	
DQ low-impedance time from CK/$\overline{CK}$	tLZ(DQ)	2*tAC min	tAC max	2*tAC min	tAC max	ps	
DQS-DQ skew for DQS and associated DQ signals	tDQSQ	-	240	-	200	ps	
DQ hold skew factor	tQHS	-	340	-	300	ps	
DQ/DQS output hold time from DQS	tQH	tHP - tQHS	-	tHP - tQHS	-	ps	
First DQS latching transition to associated clock edge	tDQSS	- 0.25	+ 0.25	- 0.25	+ 0.25	tCK	
DQS input high pulse width	tDQSH	0.35	-	0.35	-	tCK	
DQS input low pulse width	tDQSL	0.35	-	0.35	-	tCK	
DQS falling edge to CK setup time	tDSS	0.2	-	0.2	-	tCK	
DQS falling edge hold time from CK	tDSH	0.2	-	0.2	-	tCK	
Mode register set command cycle time	tMRD	2	-	2	-	tCK	
Write preamble	tWPRE	0.35	-	0.35	-	tCK	
Write postamble	tWPST	0.4	0.6	0.4	0.6	tCK	
Address and control input setup time	tIS	200	-	175	-	ps	
Address and control input hold time	tIH	275	-	250	-	ps	
Read preamble	tRPRE	0.9	1.1	0.9	1.1	tCK	
Read postamble	tRPST	0.4	0.6	0.4	0.6	tCK	
Auto-Refresh to Active/Auto-Refresh command period	tRFC	127.5	-	127.5	-	ns	
Active to active command period for 1KB page size products	tRRD	7.5	-	7.5	-	ns	
Active to active command period for 2KB page size products	tRRD	10	-	10	-	ns	
Four Active Window for 1KB page size products	tFAW	37.5	-	35	-	ns	
Four Active Window for 2KB page size products	tFAW	50	-	45	-	ns	

- continued -

Parameter	Symbol	DDR2-667		DDR2-800		Unit	Note
		min	max	min	max		
$\overline{CAS}$ to $\overline{CAS}$ command delay	tCCD	2		2		tCK	
Write recovery time	tWR	15	-	15	-	ns	
Auto precharge write recovery + precharge time	tDAL	WR+tRP	-	WR+tRP	-	tCK	
Internal write to read command delay	tWTR	7.5	-	7.5	-	ns	
Internal read to precharge command delay	tRTP	7.5		7.5		ns	
Exit self refresh to a non-read command	tXSNR	tRFC + 10		tRFC + 10		ns	
Exit self refresh to a read command	tXSRD	200	-	200	-	tCK	
Exit precharge power down to any non-read command	tXP	2	-	2	-	tCK	
Exit active power down to read command	tXARD	2		2		tCK	
Exit active power down to read command (Slow exit, Lower power)	tXARDS	7 - AL		8 - AL		tCK	
CKE minimum pulse width (high and low pulse width)	tCKE	3		3		tCK	
ODT turn-on delay	tAOND	2	2	2	2	tCK	
ODT turn-on	tAON	tAC(min)	tAC(max) +0.7	tAC(min)	tAC(max) +0.7	ns	
ODT turn-on(Power-Down mode)	tAONPD	tAC(min)+2	2tCK+ tAC(max)+1	tAC(min) +2	2tCK+ tAC(max)+1	ns	
ODT turn-off delay	tAOFD	2.5	2.5	2.5	2.5	tCK	
ODT turn-off	tAOF	tAC(min)	tAC(max)+ 0.6	tAC(min)	tAC(max) +0.6	ns	
ODT turn-off (Power-Down mode)	tAOFPD	tAC(min) +2	2.5tCK+ tAC(max)+1	tAC(min) +2	2.5tCK+ tAC(max)+1	ns	
ODT to power down entry latency	tANPD	3		3		tCK	
ODT power down exit latency	tAXPD	8		8		tCK	
OCD drive mode output delay	tOIT	0	12	0	12	ns	
Minimum time clocks remains ON after CKE asynchronously drops LOW	tDelay	tIS+tCK+tIH		tIS+tCK +tIH		ns	
Average periodic Refresh Interval	tREFI	-	7.8	-	7.8	us	2
	tREFI	-	3.9	-	3.9	us	3

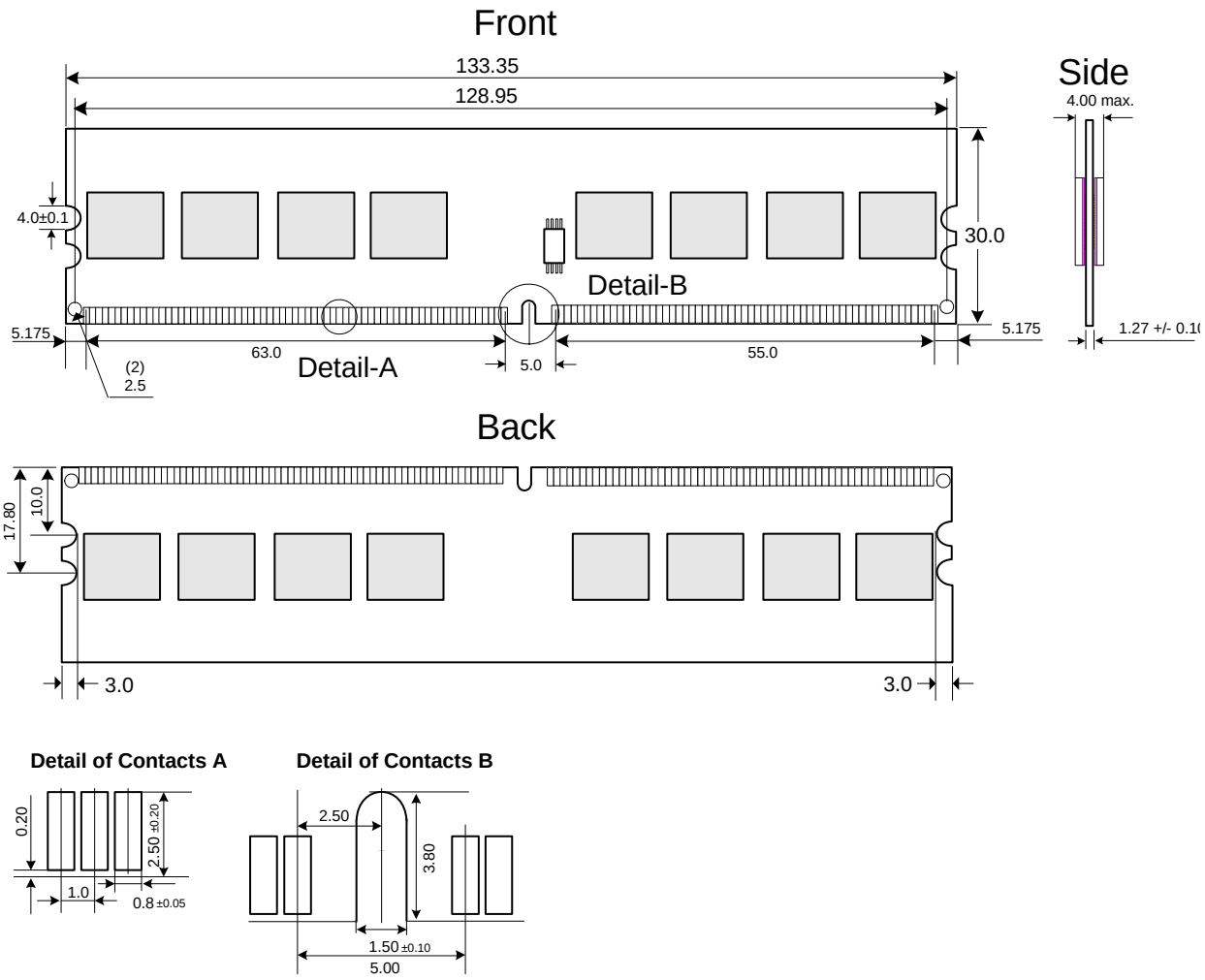
Notes:

1. For details and notes, please refer to the relevant HYNIX component datasheet (HY5PS1G[8,16]31CFP).

2. 0°C ≤ TCASE ≤ 85°C

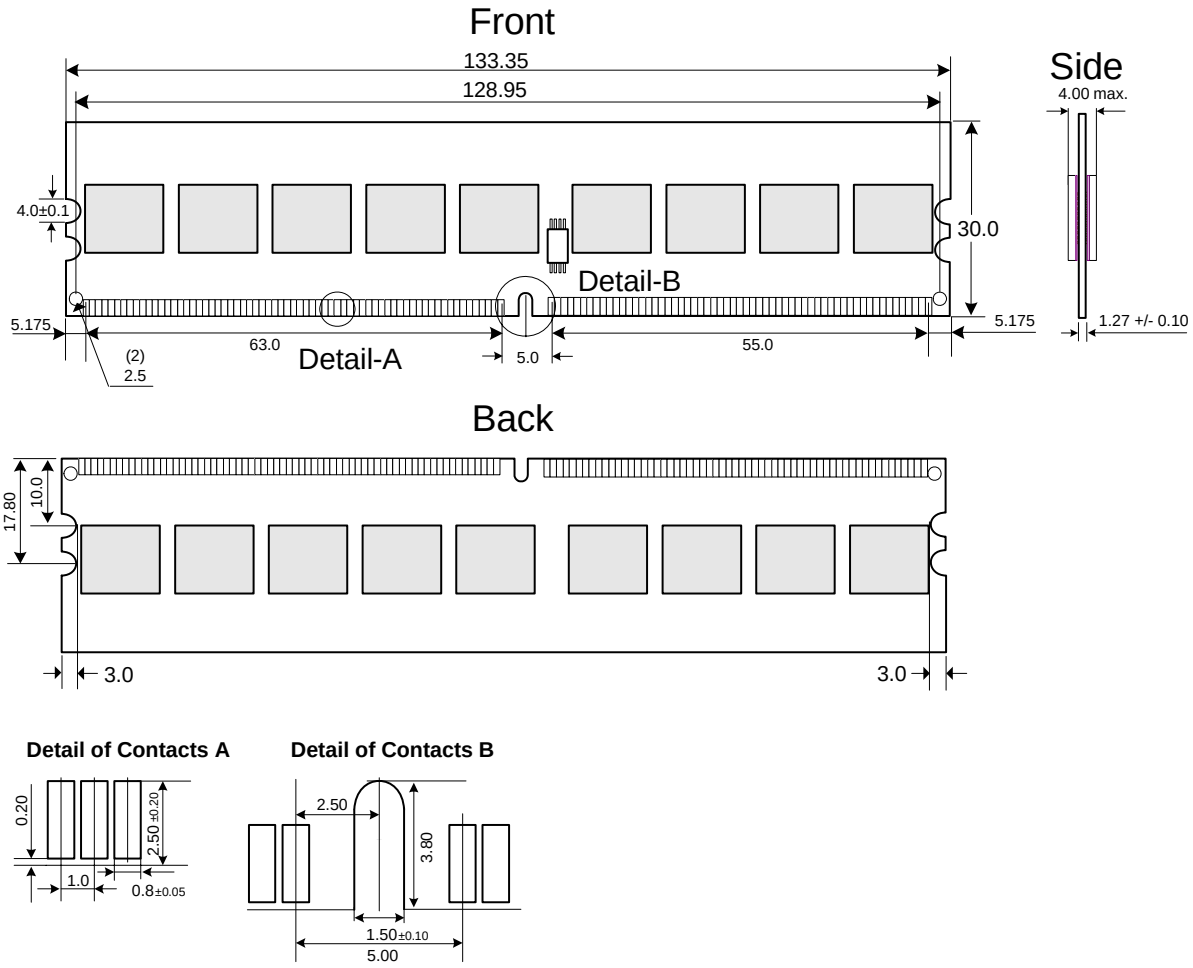
3. 85°C < TCASE ≤ 95°C

PACKAGE OUTLINE
512Mx 64 - HMP351U6AFR8C



Note : All dimensions are in millimeters unless otherwise stated.

PACKAGE OUTLINE
512Mx 72 - HMP351U7AFR8C



Note : All dimensions are in millimeters unless otherwise stated.

REVISION HISTORY

Revision	History	Date
0.1	Initial data sheet released	Mar. 2009