

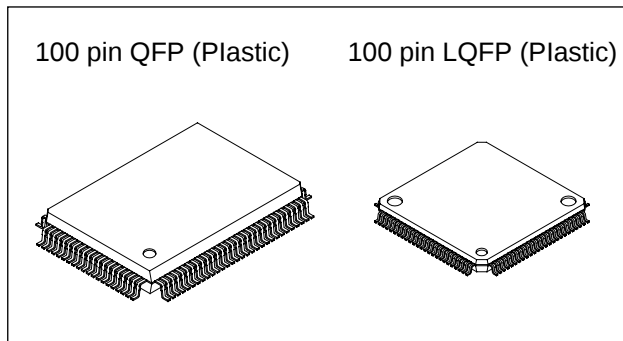
CMOS 8-bit Single Chip Microcomputer

Description

The CXP877P48A is a CMOS 8-bit microcomputer which consists of A/D converter, serial interface, timer/counter, time base timer, vector interruption, high precision timing pattern generation circuit, PWM generator, PWM for tuner, VISS/VASS circuit, 32kHz timer/event counter, remote control receiving circuit, VCR vertical sync separation circuit and the measuring circuit which measure signals of capstan FG and drum FG/PG and other servo systems, as well as basic configurations like 8-bit CPU, PROM, RAM and I/O port. They are integrated into a single chip.

Also CXP877P48A provides sleep/stop function which enables to lower power consumption and ultra low speed instruction mode in 32kHz operation.

This IC is the PROM-incorporated version of the CXP87748A with built-in mask ROM. This provides the additional feature of being able to write directly into the program. Thus, it is most suitable for evaluation use during system development and for small-quantity production.



Structure

Silicon gate CMOS IC

Features

- A wide instruction set (213 instructions) which cover various types of data
 - 16-bit arithmetic instruction/multiplication and division instructions/boolean bit operation instruction
- Minimum instruction cycle
 - During operation 333ns/12MHz (Supply voltage 3.0 to 5.5V)
 - During operation 250ns/16MHz (Supply voltage 4.5 to 5.5V)
 - During operation 122μs/32kHz
- Incorporated PROM capacity 48Kbytes
- Incorporated RAM capacity 1344bytes
- Peripheral functions
 - A/D converter 8-bit, 12-channel, successive approximation system (Conversion time 20.0μs/16MHz)
 - Serial interface Incorporated 8-bit and 8-stage FIFO (1 to 8 bytes auto transfer), 1-channel
8-bit serial I/O, 1-channel
 - Timer 8-bit timer, 8-bit timer/counter, 19-bit time base timer
32kHz timer/counter
 - High precision timing pattern generator PPG 19 pins 32-stage programmable
RTG 5-pins 2-channel
 - PWM/DA gate output 12-bit, 2-channel (Repetitive frequency 62kHz/16MHz)
 - Servo input control Capstan FG, Drum FG/PG, CTL input
 - VSYNC separator
 - FRC capture unit
 - PWM output Incorporated 26-bit and 8-stage FIFO
14-bit, 1-channel
 - VISS/VASS circuit Pulse duty auto detection circuit
 - Remote control receiving circuit 8-bit pulse measuring counter, 6-stage FIFO
- Interruption 21 factors, 15 vectors, multi-interruption possible
- Standby mode SLEEP/STOP
- Package 100-pin plastic QFP/LQFP

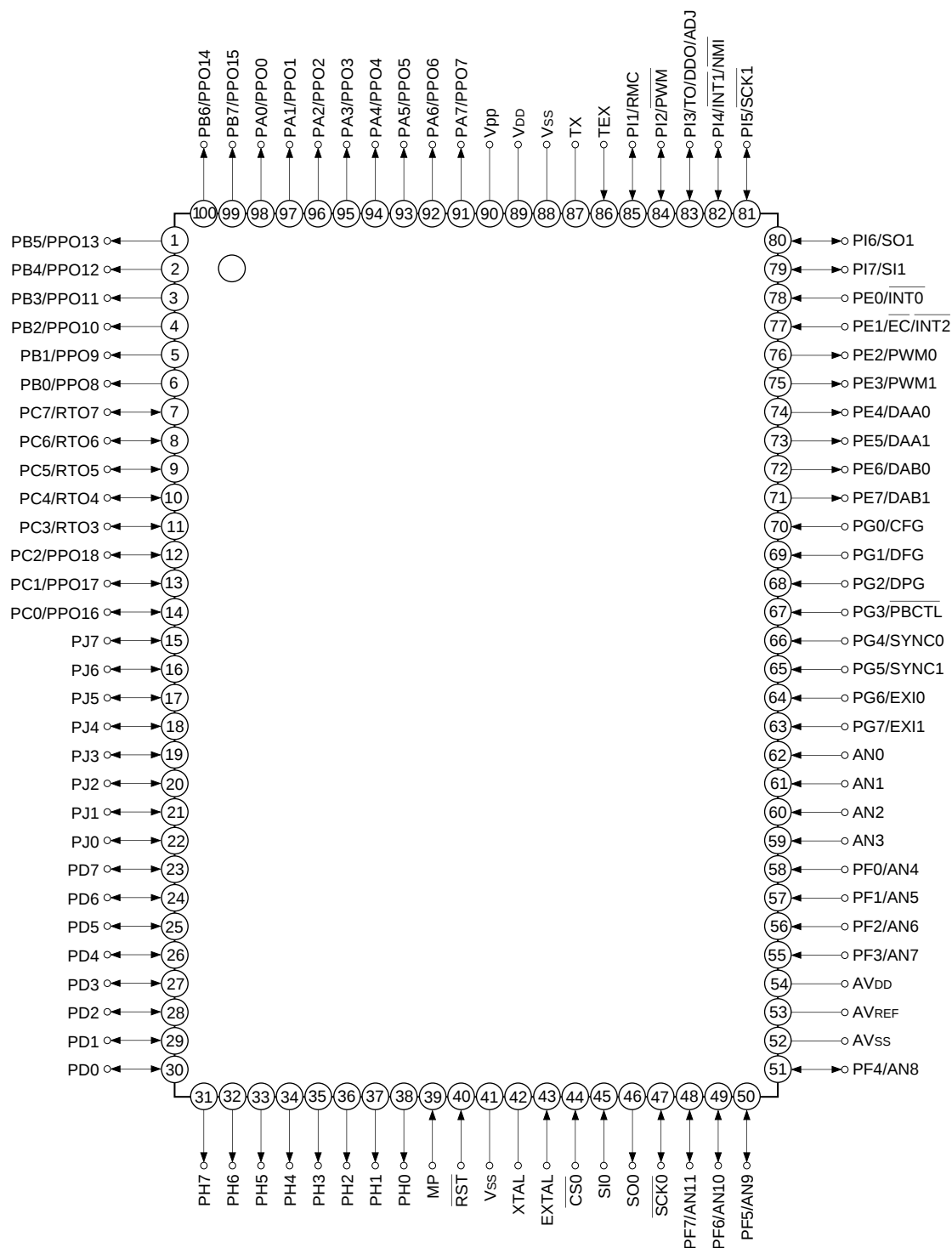
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The diagram illustrates the internal architecture of the SPC700 CPU core and its peripheral components. The core is divided into several functional blocks:

- CPU Core:** The central component, labeled "SPC700 CPU CORE", which is connected to the "CLOCK GENERATOR/SYSTEM CONTROL" and "RAM 1344 BYTES".
- Memory:** Includes "RAM 1344 BYTES" and "PROM 48K BYTES".
- Timers and Counters:** Includes a "PRESCALER/TIME BASE TIMER", a "32kHz TIMER/COUNTER", and an "8 BIT TIMER/COUNTER 0".
- Serial Interface:** Includes a "SERIAL INTERFACE UNIT (CH0)" and a "SERIAL INTERFACE UNIT (CH1)".
- Input/Output:** Includes an "A/D CONVERTER", a "V SYNC SEPARATOR", and a "CAPSTAN/DRUM CTL".
- Control and Timing:** Includes a "SERVO INPUT CONTROL", a "REMOCON INPUT", and a "VSS/VASS" block.
- Generators:** Includes a "14 BIT PWM GENERATOR", a "12 BIT PWM GENERATOR CH0", and a "12 BIT PWM GENERATOR CH1".
- Real Time Pulse Generator:** Includes a "REAL TIME PULSE GENERATOR" with channels "CH0" and "CH1".
- Programmable Pattern Generator:** Includes a "PROGRAMMABLE PATTERN GENERATOR" with "RAM" and "FIFO" blocks.
- Interrupt Controller:** Includes an "INTERRUPT CONTROLLER" with "NMI" and "PE0/INT0" inputs.
- Ports:** Includes "PORT A" through "PORT J", each with a specific data width (e.g., PORT A: 8 bits, PORT B: 8 bits, PORT C: 8 bits, PORT D: 8 bits, PORT E: 2 bits, PORT F: 6 bits, PORT G: 4 bits, PORT H: 4 bits, PORT I: 8 bits, PORT J: 8 bits).
- External Connections:** Includes "Vpp", "Vss", "Vbd", "MP", "RST", "XTAL", "TX", and "TEX" pins.

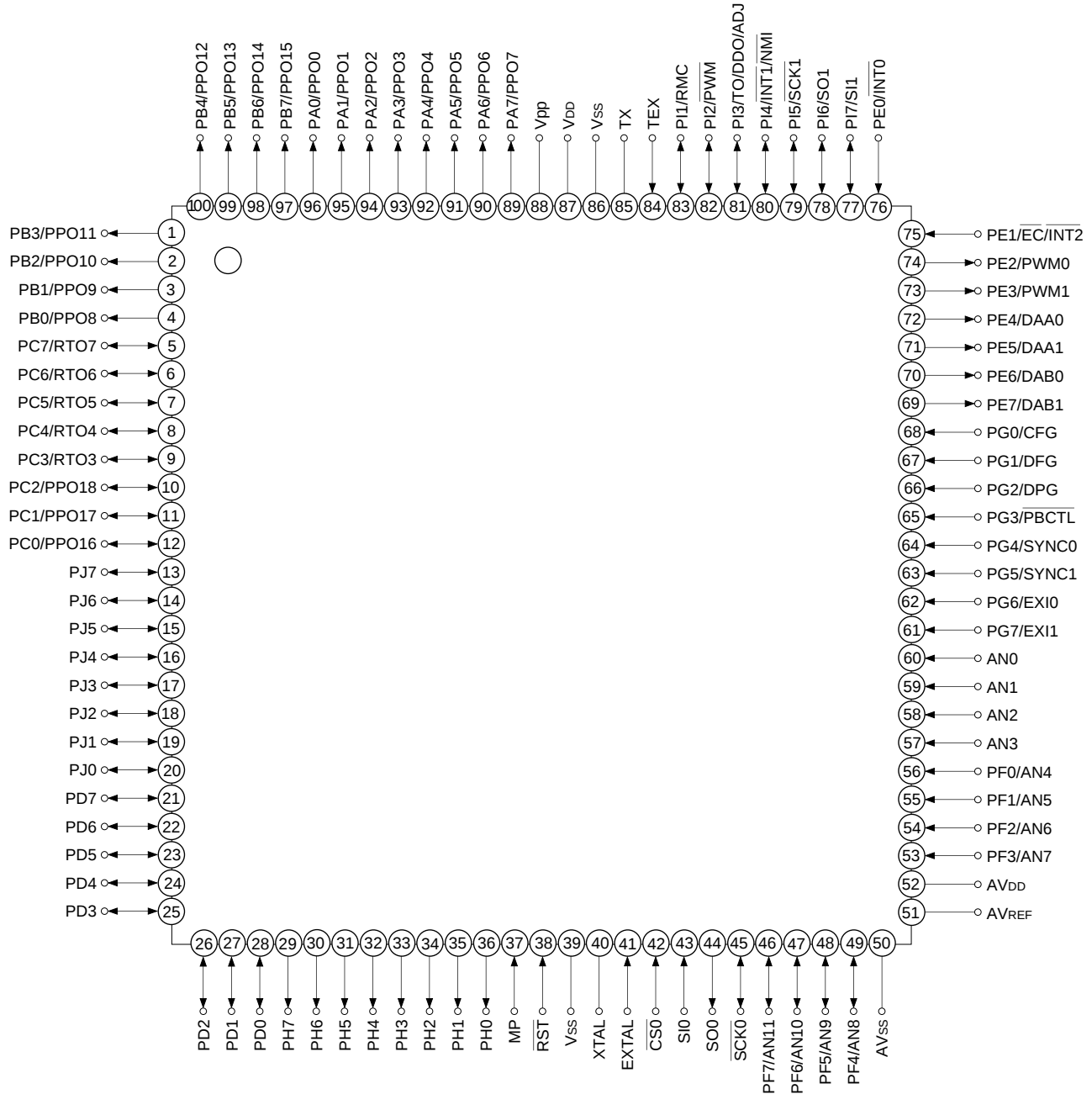
The diagram shows the interconnections between these components, including data buses, control lines, and timing signals. The SPC700 CPU core is the central processing unit, and the various peripheral blocks provide the necessary functions for system operation.

Pin Configuration 1 (Top View) 100 pin QFP package



- Note)**
1. Vpp (Pin 90) is always connected to VDD.
 2. Vss (Pins 41 and 88) are both connected to GND.

Pin Configuration 2 (Top View) 100 pin LQFP package



- Note)**
1. Vpp (Pin 88) is always connected to VDD.
 2. Vss (Pins 39 and 86) are both connected to GND.

Pin Description

Symbol	I/O	Description	
PA0/PPO0 to PA7/PPO7	Output/ Real time Output	(Port A) 8-bit output port. Data is gated with PPO contents by OR-gate and they are output. (8 pins)	Programmable pattern generator (PPG) output. Functions as high precision real time pulse output port. (19 pins)
PB0/PPO8 to PB7/PPO15	Output/ Real time Output	(Port B) 8-bit output port. Data is gated with PPO contents by OR-gate and they are output. (8 pins)	
PC0/PPO16 to PC2/PPO18	I/O/ Real time Output	(Port C) 8-bit I/O port, enables to specify I/O by bit unit. Data is gated with PPO or RTO contents by OR-gate and they are output. (8 pins)	
PC3/RTO3 to PC7/RTO7	I/O/ Real time Output		Real time pulse generator (RTG) output. Functions as high precision real time pulse output port. (5 pins)
PD0 to PD7	I/O	(Port D) 8-bit I/O port. Enable to specify I/O by 4-bit unit. Enables to drive 12mA sink current. (8 pins)	
PE0/ $\overline{\text{INT0}}$	Input/input	(Port E) 8-bit port. Lower 2 bits are input pins and upper 6 bits are output pins. (8 pins)	Input pin to request external interruption. Active when falling edge.
PE1/ $\overline{\text{EC}}/\overline{\text{INT2}}$	Input/input/input		External event input pin for timer/counter. Input pin to request external interruption. Active when falling edge.
PE2/PWM0	Output/output		PWM output pins. (2 pins)
PE3/PWM1	Output/output		
PE4/DAA0	Output/output		DA gate pulse output pins. (4 pins)
PE5/DAA1	Output/output		
PE6/DAB0	Output/output		
PE7/DAB1	Output/output		
AN0 to AN3	Input	Analog input pins to A/D converter. (12 pins)	
PF0/AN4 to PF3/AN7	Input/input	(Port F) Lower 4 bits are input port and upper 4 bits are output port. Lower 4 bits also serve as standby release input pin. (8 pins)	
PF4/AN8 to PF7/AN11	Output/input		
$\overline{\text{SCK0}}$	I/O	Serial clock (CH0) I/O pin.	
SO0	Output	Serial data (CH0) output pin.	
SI0	Input	Serial data (CH0) input pin.	
$\overline{\text{CS0}}$	Input	Serial chip select (CH0) input pin.	

Symbol	I/O	Description	
PG0/CFG	Input/input	(Port G) 8-bit input port. (8 pins)	Capstan FG input pin.
PG1/DFG	Input/input		Drum FG input pin.
PG2/DPG	Input/input		Drum PG input pin.
PG3/PBCTL	Input/input		Playback CTL pulse input pin.
PG4/SYNC0	Input/input		Composite sync signal input pin.
PG5/SYNC1	Input/input		
PG6/EXI0	Input/input		External input pin to FRC capture unit.
PG7/EXI1	Input/input		
PH0 to PH7	Output	(Port H) 8-bit output port ; Medium withstand voltage (12V) and high current (12mA), N-ch open drain output. (8 pins)	
PI1/RMC	I/O/input	(Port I) 7-bit I/O port. I/O port can be specified by bit unit. (7 pins)	Remote control receiving circuit input pin.
PI2/PWM	I/O/output		14-bit PWM output pin.
PI3/TO/ DDO/ADJ	I/O/output/ output/output		Timer/counter, CTL duty detection, 32kHz oscillation adjustment output pin.
PI4/INT1/ NMI	I/O/input/input		Input pin to request external interruption and non maskable interruption. Active when falling edge.
PI5/SCK1	I/O/I/O		Serial clock (CH1) I/O pin.
PI6/SO1	I/O/output		Serial data (CH1) output pin.
PI7/SI1	I/O/input		Serial data (CH1) input pin.
PJ0 to PJ7	I/O	(Port J) 8-bit I/O port. Function as standby release input can be specified by bit unit. I/O can be specified by bit unit.	
EXTAL	Input	Connecting pin of crystal oscillator for system clock. When supplying the external clock, input the external clock to EXTAL pin and input opposite phase clock to XTAL pin.	
XTAL	Output		
TEX	Input	Connecting pin of crystal oscillator for 32kHz timer clock. When used as event counter, input to TEX pin and leave TX pin open. (Feedback resistor is not removed.)	
TX	Output		
RST	Input	System reset pin of active "L" level.	
MP	Input	Microprocessor mode input pin. Always connect to GND.	
AV _{DD}		Positive power supply pin of A/D converter.	
AV _{REF}	Input	Reference voltage input pin of A/D converter.	
AV _{SS}		GND pin of A/D converter.	
V _{DD}		Positive power supply pin.	
V _{pp}		Vcc supply for writing of built-in PROM. Under normal operating conditions, connect to V _{DD} .	
V _{SS}		GND pin. Connect both V _{SS} pins to GND.	

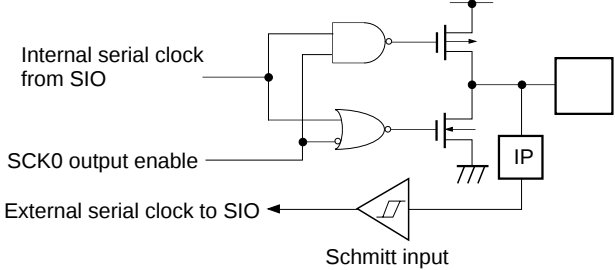
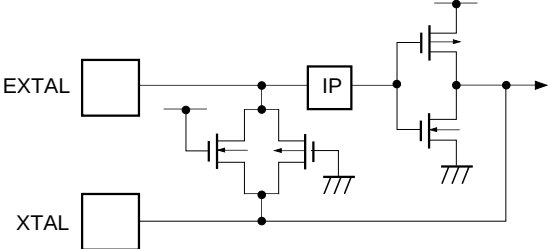
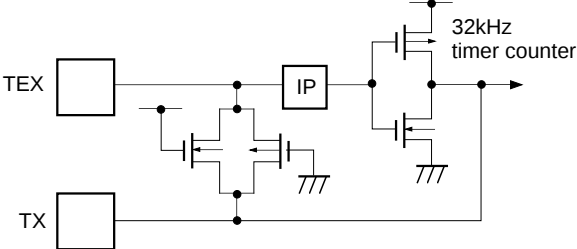
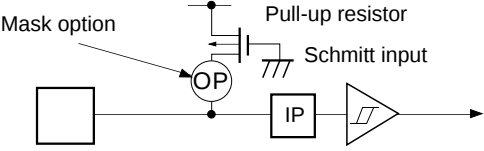
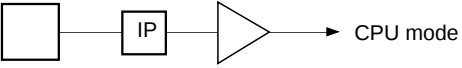
Input/Output Circuit Formats for Pins

Pin	Circuit format	When reset
Port A Port B PA0/PPO0 to PA7/PPO7 PB0/PPO8 to PB7/PPO15 16 pins	PPO data Port A or Port B Data bus RD Output becomes active from high impedance by data writing to port register.	Hi-Z
Port C PC0/PPO16 to PC2/PPO18 PC3/RTO3 to PC7/RTO7 8 pins	PPO, RTO data Port C data Port C direction Data bus RD (Port C) (Every bit) Input protection circuit IP	Hi-Z
Port D PD0 to PD7 8 pins	Port D data Port D direction Data bus RD (Port D) (Every 4 bits) (PD0 to 3) (PD4 to 7) High current 12mA IP	Hi-Z

Pin	Circuit format	When reset
PE0/ $\overline{\text{INT0}}$ PE1/ $\overline{\text{EC}}/\text{INT2}$ 2 pins	Port E Schmitt input IP RD (Port E) Data bus	Hi-Z
PE2/PWM0 PE3/PWM1 PE4/DAA0 PE5/DAA1 4 pins	Port E DA gate output or PWM output Hi-Z control Port E data Port/DA output select RD (Port E) Data bus	Hi-Z
PE6/DAB0 PE7/DAB1 2 pins	Port E DA gate output Hi-Z control Port E data Port/DA output select RD (Port E) Data bus	H level
AN0 to AN3 4 pins	Input multiplexer IP A/D converter	Hi-Z
PF0/AN4 to PF3/AN7 4 pins	Port F Input multiplexer IP A/D converter RD (Port F) Data bus	Hi-Z

Pin	Circuit format	When reset
PF4/AN8 to PF7/AN11 4 pins	Port F	Hi-Z
PG0/CFG PG1/DFG PG2/DPG PG3/PBCTL PG4/SYNC0 PG5/SYNC1 PG6/EXI0 PG7/EXI1 8 pins	Port G Note) For PG4 and PG5 input format, there are CMOS schmitt input and TTL schmitt input with product.	Hi-Z
PH0 to PH7 8 pins	Port H	Hi-Z
PI2/PWM PI3/TO/ DDO/ADJ 2 pins	Port I PI2: From 14-bit PWM PI3: From timer/counter, CTL duty detection circuit, 32kHz timer	Hi-Z

PIn	Circuit format	When reset
PI1/RMC PI4/INT1/NMI PI7/SI1 3 pins	Port I Port I data Port I direction Data bus RD (Port I) Schmitt input IP PI1: To remote control circuit PI4: To interruption circuit PI7: To serial CH1	Hi-Z
PI5/SCK1 PI6/SO1 2 pins	Port I function select From serial CH1 Port I data Port I direction Data bus RD (Port I) MPX Note) (PI5 is schmitt input PI6 is inverter input) To serial CH1 IP	Hi-Z
PJ0 to PJ7 8 pins	Port J data Port J direction Data bus RD (Port J) Edge detection Standby release IP	Hi-Z
CS0 SIO 2 pins	Schmitt input IP To SIO	Hi-Z
SO0 1 pin	SO0 from SIO SO0 output enable	Hi-Z

Pin	Circuit format	When reset
$\overline{\text{SCK0}}$ 1 pin	 Internal serial clock from SIO SCK0 output enable External serial clock to SIO Schmitt input IP	Hi-Z
EXTAL XTAL 2 pins	 - Shows the circuit composition during oscillation. - Feedback resistor is removed during stop.	Oscillation
TEX TX 2 pins	 - Shows the circuit composition during oscillation. - Feedback resistor is removed during 32kHz oscillation circuit stop by software. At this time TEX pin outputs "L" level and TX pin outputs "H" level.	Oscillation
$\overline{\text{RST}}$ 1 pin	 Mask option Pull-up resistor Schmitt input IP	L level
MP 1 pin	 CPU mode	Hi-Z

Absolute Maximum Ratings

(V_{SS} = 0V)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V _{DD}	−0.3 to +7.0	V	
	V _{pp}	−0.3 to +13	V	Incorporated PROM
	AV _{DD}	AV _{SS} to +7.0* ¹	V	
	AV _{SS}	−0.3 to +0.3	V	
Input voltage	V _{IN}	−0.3 to +7.0* ²	V	
Output voltage	V _{OUT}	−0.3 to +7.0* ²	V	
Medium withstand output voltage	V _{OUTP}	−0.3 to +15.0	V	PH pin
High level output current	I _{OH}	−5	mA	
High level total output current	ΣI _{OH}	−50	mA	Total of output pins
Low level output current	I _{OL}	15	mA	Other than high current output pins: per pin
	I _{OLC}	20	mA	High current port pin* ³ : per pin
Low level total output current	ΣI _{OL}	130	mA	Total of output pins
Operating temperature	T _{opr}	−10 to +75	°C	
Storage temperature	T _{stg}	−55 to +150	°C	
Allowable power dissipation	P _D	600	mW	QFP package type
		380		LQFP package type

*¹ AV_{DD} and V_{DD} should be set to a same voltage.

*² V_{IN} and V_{OUT} should not exceed V_{DD} + 0.3V.

*³ The high current operation transistors are the N-CH transistors of the PD and PH ports.

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should better take place under the recommended operating conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions

(V_{SS} = 0V)

Item	Symbol	Min.	Max.	Unit	Remarks	
Supply voltage	V _{DD}	4.5	5.5	V	fc = 16MHz	Guaranteed range during high speed mode (1/2 dividing clock) operation
		3.0	5.5	V	fc = 12MHz	
		2.7	5.5	V	Guaranteed range during low speed mode (1/16 dividing clock) operation	
		2.7	5.5	V	Guaranteed operation range by TEX clock	
		2.5	5.5	V	Guaranteed data hold operation range during STOP	
	V _{pp}	V _{pp} = V _{DD}		V	*9	
Analog power supply	AV _{DD}	3.0	5.5	V	*1	
High level input voltage	V _{IH}	0.7V _{DD}	V _{DD}	V	*2	
	V _{IHS}	0.8V _{DD}	V _{DD}	V	CMOS schmitt input*3	
	V _{IHTS}	2.2	V _{DD}	V	TTL schmitt input*4, *7	
	V _{IHEX}	V _{DD} − 0.4	V _{DD} + 0.3	V	EXTAL pin*5, *7	TEX pin*6, *7
		V _{DD} − 0.2	V _{DD} + 0.2	V	EXTAL pin*5, *8	TEX pin*6, *8
Low level input voltage	V _{IL}	0	0.3V _{DD}	V	*2, *7	
		0	0.2V _{DD}	V	*2, *8	
	V _{ILS}	0	0.2V _{DD}	V	CMOS schmitt input*3	
	V _{ILTS}	0	0.8	V	TTL schmitt input*4, *7	
	V _{ILEX}	−0.3	0.4	V	EXTAL pin*5, *7	TEX pin*6, *7
		−0.3	0.2	V	EXTAL pin*5, *8	TEX pin*6, *8
Operating temperature	Topr	−20	+75	°C		

*1 AV_{DD} and V_{DD} should be set to a same voltage.

*2 Normal input port (each pin of PC, PD, PE0 to PE1, PF0 to PF3, PG, PI and PJ), MP pin.

*3 Each pin of $\overline{\text{CS0}}$, SI0, $\overline{\text{SCK0}}$, $\overline{\text{RST}}$, PE0/ $\overline{\text{INT0}}$, PE1/ $\overline{\text{EC/INT2}}$, PG (For PG4 and PG5, when CMOS schmitt input is selected with mask option), PI1/RMC, PI4/ $\overline{\text{INT1/NMI}}$, PI5/ $\overline{\text{SCK1}}$ and PI7/SI1.

*4 Each pin of PG4 and PG5 (When TTL schmitt input is selected with mask option)

*5 It specifies only when the external clock is input.

*6 It specifies only when the event count clock is input.

*7 This case applies to the range of 4.5 to 5.5V supply voltage (V_{DD}).

*8 This case applies to the range of 3.0 to 3.6V supply voltage (V_{DD}).

*9 V_{pp} and V_{DD} should be set to a same voltage.

Electrical Characteristics

DC Characteristics ($V_{DD} = 4.5$ to $5.5V$)($T_a = -10$ to $+75^\circ C$, $V_{SS} = 0V$)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V _{OH}	PA to PD, PE2 to PE7, PF4 to PF7, PH (V _{OL} only)	V _{DD} = 4.5V, I _{OH} = −0.5mA	4.0			V
			V _{DD} = 4.5V, I _{OH} = −1.2mA	3.5			V
Low level output voltage	V _{OL}	PI1 to PI7 PJ, SO0, SCK0	V _{DD} = 4.5V, I _{OL} = 1.8mA			0.4	V
			V _{DD} = 4.5V, I _{OL} = 3.6mA			0.6	V
		PD, PH	V _{DD} = 4.5V, I _{OL} = 12.0mA			1.5	V
Input current	I _{IHE}	EXTAL	V _{DD} = 5.5V, V _{IH} = 5.5V	0.5		40	μA
	I _{ILE}		V _{DD} = 5.5V, V _{IL} = 0.4V	−0.5		−40	μA
	I _{IHT}	TEX	V _{DD} = 5.5V, V _{IH} = 5.5V	0.1		10	μA
	I _{ILT}		V _{DD} = 5.5V, V _{IL} = 0.4V	−0.1		−10	μA
	I _{ILR}	RST		−1.5		−400	μA
I/O leakage current	I _{IZ}	PA to PG, PI, PJ, MP AN0 to AN3, CS0, SI0, SO0 SCK0, RST	V _{DD} = 5.5V, V _I = 0, 5.5V			±10	μA
Open drain output leakage current (N-CH Tr OFF in state)	I _{LOH}	PH	V _{DD} = 5.5V V _{OH} = 12V			50	μA
Supply current*1	I _{DD1}	V _{DD}	16MHz crystal oscillation (C ₁ = C ₂ = 15pF)		24	45	mA
			V _{DD} = 5V ± 0.5V*2				
	I _{DDS1}		SLEEP mode		1.5	8	mA
			V _{DD} = 5V ± 0.5V				
	I _{DD2}		32kHz crystal oscillation (C ₁ = C ₂ = 47pF)		430	1000	μA
			V _{DD} = 3V ± 0.3V				
	I _{DDS2}		SLEEP mode		9	30	μA
			V _{DD} = 3V ± 0.3V				
I _{DDS3}	STOP mode (EXTAL and TEX pins oscillation stop)				30	μA	
	V _{DD} = 5V ± 0.5V						
Input capacity	C _{IN}	Other than V _{DD} , V _{SS} , AV _{DD} , and AV _{SS}	Clock 1MHz 0V other than the measured pins		10	20	pF

*1 When entire output pins are open.

*2 When setting upper 2 bits (CPU clock selection) of clock control register CLC (address: 00FEH) to "00" and operating in high speed mode (1/2 dividing clock).

DC Characteristics ($V_{DD} = 3.0$ to $3.6V$)($T_a = -10$ to $+75^\circ C$, $V_{SS} = 0V$)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA to PD, PE2 to PE7, PF4 to PF7, PH (V_{OL} only)	$V_{DD} = 3.0V$, $I_{OH} = -0.15mA$	2.7			V
		PI1 to PI7	$V_{DD} = 3.0V$, $I_{OH} = -0.5mA$	2.3			V
Low level output voltage	V_{OL}	PJ, SO0, SCK0	$V_{DD} = 3.0V$, $I_{OL} = 1.2mA$			0.3	V
			$V_{DD} = 3.0V$, $I_{OL} = 1.6mA$			0.5	V
		PD, PH	$V_{DD} = 3.0V$, $I_{OL} = 5mA$			1.0	V
Input current	I_{IHE}	EXTAL	$V_{DD} = 3.6V$, $V_{IH} = 3.6V$	0.3		20	μA
	I_{ILE}		$V_{DD} = 3.6V$, $V_{IL} = 0.3V$	-0.3		-20	μA
	I_{IHT}	TEX	$V_{DD} = 3.6V$, $V_{IH} = 3.6V$	0.1		10	μA
	I_{ILT}		$V_{DD} = 3.6V$, $V_{IL} = 0.3V$	-0.1		-10	μA
	I_{ILR}	RST		-0.9		-200	μA
I/O leakage current	I_{IZ}	PA to PG, PI, PJ, MP, AN0 to AN3, CS0, SI0, SO0, SCK0, RST	$V_{DD} = 3.6V$, $V_I = 0, 3.6V$			± 10	μA
Open drain output leakage current	I_{LOH}	PH	$V_{DD} = 3.6V$, $V_{OH} = 12V$			50	μA
Supply current*1	I_{DD1}	V_{DD}	12MHz crystal oscillation ($C_1 = C_2 = 15pF$)		12	25	mA
			$V_{DD} = 3.3V \pm 0.3V^{*2}$				
	I_{DDS1}		SLEEP mode		0.7	2.5	mA
			$V_{DD} = 3.3V \pm 0.3V$				
	I_{DDS3}		STOP mode (EXTAL and TEX pins oscillation stop)			30	μA
			$V_{DD} = 3.3V \pm 0.3V$				
Input capacity	C_{IN}	Other than V_{DD} , V_{SS} , AV_{DD} , and AV_{SS}	Clock 1MHz 0V other than the measured pins		10	20	pF

*1 When entire output pins are open.

*2 When setting upper 2 bits (CPU clock selection) of clock control register CLC (address: 00FEH) to "00" and operating in high speed mode (1/2 dividing clock).

AC Characteristics

(1) Clock timing

(Ta = -10 to +75°C, VDD = 3.0 to 5.5V, VSS = 0V)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
System clock frequency	fc	XTAL EXTAL	Fig. 1, Fig. 2 VDD = 4.5 to 5.5V	1	16	MHz
				1	12	
System clock input pulse width	tXL, tXH	XTAL EXTAL	Fig. 1, Fig. 2 (External clock drive) VDD = 4.5 to 5.5V	28		ns
				37.5		
System clock input rise and fall times	tCR, tCF	XTAL EXTAL	Fig. 1, Fig. 2 (External clock drive)		200	ns
Event count clock input pulse width	tEH, tEL	$\overline{EC}$	Fig. 3	tsys × 4*		ns
Event count clock input rise and fall times	tER, tEF	$\overline{EC}$	Fig. 3		20	ns
System clock frequency	fc	TEX TX	Fig. 2 VDD = 2.7 to 5.5V (32kHz clock applied condition)	32.768		kHz
Event count clock input pulse width	tTL, tTH	TEX	Fig. 3	10		μs
Event count clock input rise and fall times	tTR, tTF	TEX	Fig. 3		20	ms

* tsys indicates three values according to the contents of the clock control register (address; 00FEH) upper 2 bits (CPU clock selection).

tsys [ns] = 2000/fc (Upper 2-bit = "00"), 4000/fc (Upper 2-bit = "01"), 16000/fc (Upper 2-bit = "11")

Fig. 1. Clock timing

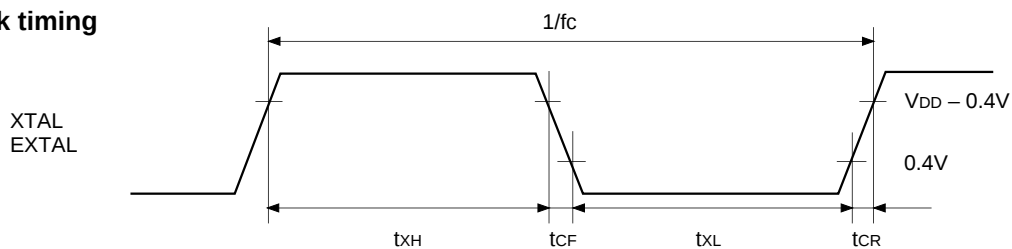


Fig. 2. Clock applied condition

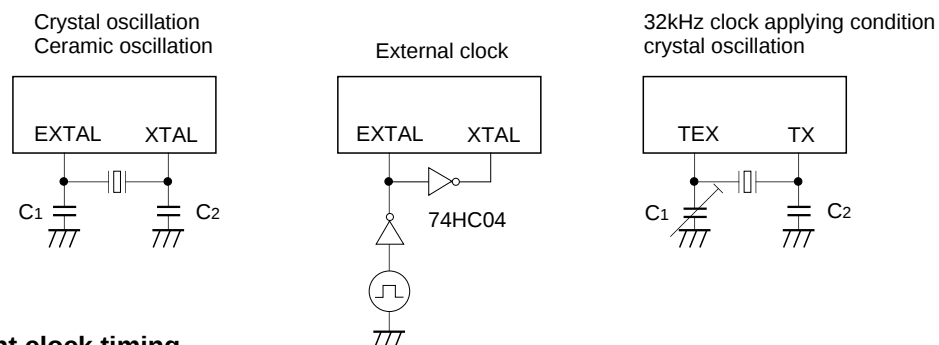
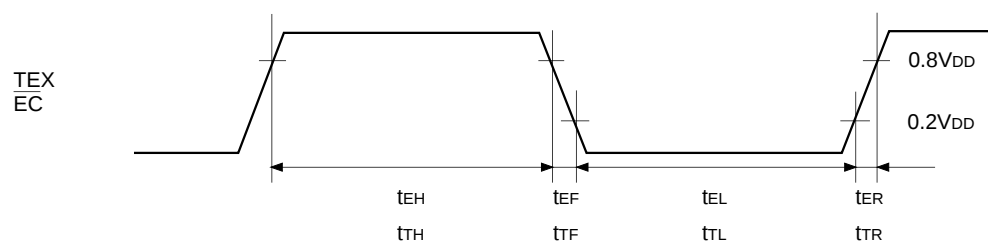


Fig. 3. Event count clock timing



(2) Serial transfer (CH0)

(Ta = -10 to +75°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{\text{CS0}} \downarrow \rightarrow \overline{\text{SCK0}}$ delay time	t_{DCSK}	$\overline{\text{SCK0}}$	Chip select transfer mode ($\overline{\text{SCK0}}$ = output mode)		$t_{\text{sys}} + 200$	ns
$\overline{\text{CS0}} \uparrow \rightarrow \overline{\text{SCK0}}$ floating delay time	t_{DCSKF}	$\overline{\text{SCK0}}$	Chip select transfer mode ($\overline{\text{SCK0}}$ = output mode)		$t_{\text{sys}} + 200$	ns
$\overline{\text{CS0}} \downarrow \rightarrow \text{SO0}$ delay time	t_{DCSO}	SO0	Chip select transfer mode		$t_{\text{sys}} + 200$	ns
$\overline{\text{CS0}} \downarrow \rightarrow \text{SO0}$ floating delay time	t_{DCSOF}	SO0	Chip select transfer mode		$t_{\text{sys}} + 200$	ns
$\overline{\text{CS0}}$ high level width	t_{WHCS}	$\overline{\text{CS0}}$	Chip select transfer mode	$t_{\text{sys}} + 200$		ns
$\overline{\text{SCK0}}$ cycle time	t_{KCY}	$\overline{\text{SCK0}}$	Input mode	$2t_{\text{sys}} + 200$		ns
			Output mode	$16000/f_c$		ns
$\overline{\text{SCK0}}$ high and low level widths	t_{KH} t_{KL}	$\overline{\text{SCK0}}$	Input mode	$t_{\text{sys}} + 100$		ns
			Output mode	$8000/f_c - 50$		ns
SI0 input setup time (against $\overline{\text{SCK0}} \uparrow$)	t_{SIK}	SI0	$\overline{\text{SCK0}}$ input mode	100		ns
			$\overline{\text{SCK0}}$ output mode	200		ns
SI0 input hold time (against $\overline{\text{SCK0}} \uparrow$)	t_{KSI}	SI0	$\overline{\text{SCK0}}$ input mode	$t_{\text{sys}} + 200$		ns
			$\overline{\text{SCK0}}$ output mode	100		ns
$\overline{\text{SCK0}} \downarrow \rightarrow \text{SO0}$ delay time	t_{KSO}	SO0	$\overline{\text{SCK0}}$ input mode		$t_{\text{sys}} + 200$	ns
			$\overline{\text{SCK0}}$ output mode		100	ns

Note 1) t_{sys} indicates three values according to the contents of the clock control register (address; 00FEH) upper 2 bits (CPU clock selection).

t_{sys} [ns] = $2000/f_c$ (Upper 2-bit = "00"), $4000/f_c$ (Upper 2-bit = "01"), $16000/f_c$ (Upper 2-bit = "11")

Note 2) The load of $\overline{\text{SCK0}}$ output mode and SO0 output delay time is 50pF + 1TTL.

Serial transfer (CH0)

(Ta = -10 to +75°C, VDD = 3.0 to 3.6V, VSS = 0V)

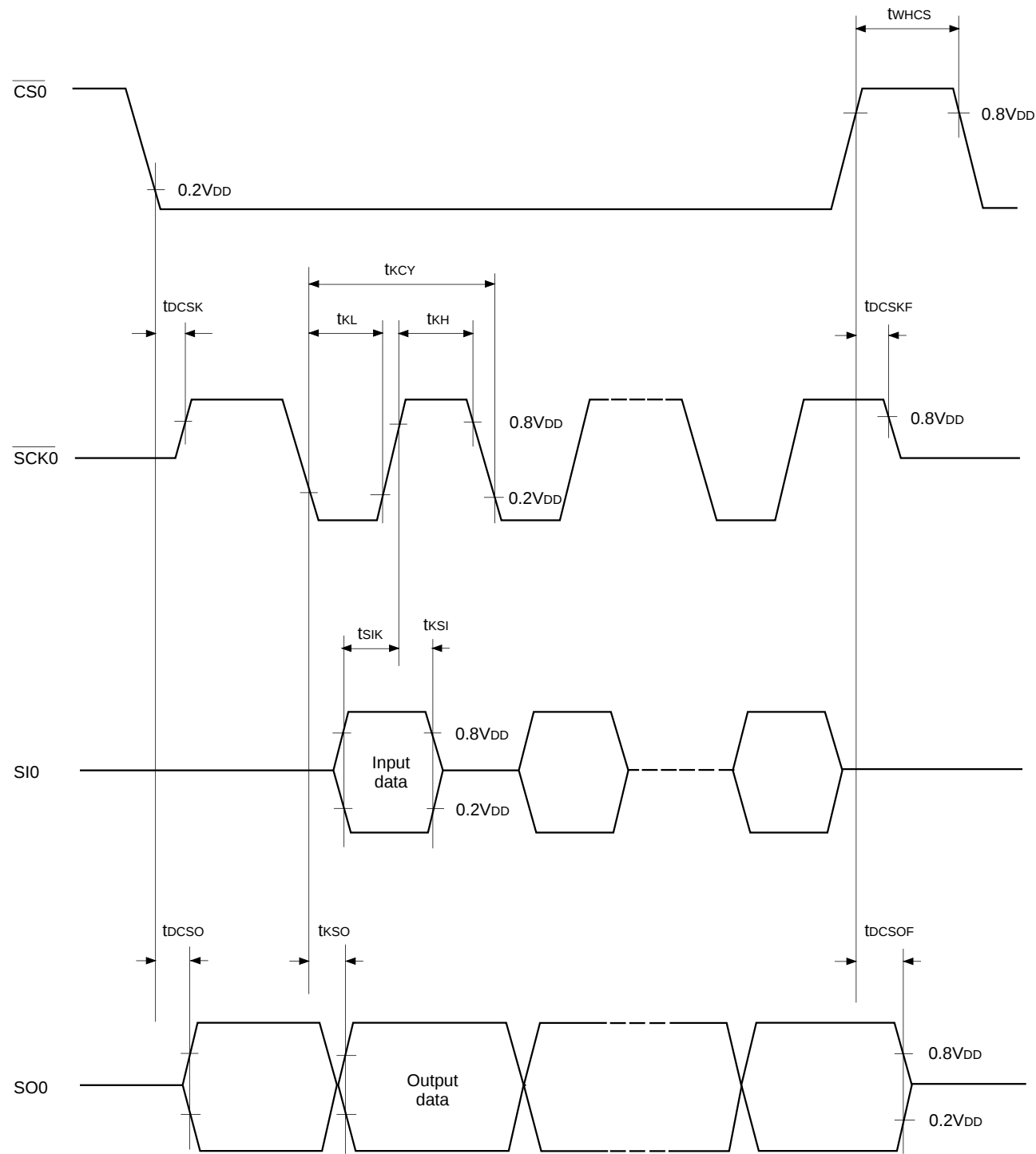
Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{\text{CS0}} \downarrow \rightarrow \overline{\text{SCK0}}$ delay time	t_{DCSK}	$\overline{\text{SCK0}}$	Chip select transfer mode ($\overline{\text{SCK0}}$ = output mode)		$t_{\text{sys}} + 250$	ns
$\overline{\text{CS0}} \uparrow \rightarrow \overline{\text{SCK0}}$ floating delay time	t_{DCSKF}	$\overline{\text{SCK0}}$	Chip select transfer mode ($\overline{\text{SCK0}}$ = output mode)		$t_{\text{sys}} + 200$	ns
$\overline{\text{CS0}} \downarrow \rightarrow \text{SO0}$ delay time	t_{DCSO}	SO0	Chip select transfer mode		$t_{\text{sys}} + 250$	ns
$\overline{\text{CS0}} \uparrow \rightarrow \text{SO0}$ floating delay time	t_{DCSOF}	SO0	Chip select transfer mode		$t_{\text{sys}} + 200$	ns
$\overline{\text{CS0}}$ high level width	t_{WHCS}	$\overline{\text{CS0}}$	Chip select transfer mode	$t_{\text{sys}} + 200$		ns
$\overline{\text{SCK0}}$ cycle time	t_{KCY}	$\overline{\text{SCK0}}$	Input mode	$2t_{\text{sys}} + 200$		ns
			Output mode	$16000/f_c$		ns
$\overline{\text{SCK0}}$ high and low level widths	t_{KH} t_{KL}	$\overline{\text{SCK0}}$	Input mode	$t_{\text{sys}} + 100$		ns
			Output mode	$8000/f_c - 100$		ns
SI0 input setup time (against $\overline{\text{SCK0}} \uparrow$)	t_{SIK}	SI0	$\overline{\text{SCK0}}$ input mode	100		ns
			$\overline{\text{SCK0}}$ output mode	200		ns
SI0 input hold time (against $\overline{\text{SCK0}} \uparrow$)	t_{KSI}	SI0	$\overline{\text{SCK0}}$ input mode	$t_{\text{sys}} + 200$		ns
			$\overline{\text{SCK0}}$ output mode	100		ns
$\overline{\text{SCK0}} \downarrow \rightarrow \text{SO0}$ delay time	t_{KSO}	SO0	$\overline{\text{SCK0}}$ input mode		$t_{\text{sys}} + 250$	ns
			$\overline{\text{SCK0}}$ output mode		100	ns

Note 1) t_{sys} indicates three values according to the contents of the clock control register (address; 00FEH) upper 2 bits (CPU clock selection).

t_{sys} [ns] = $2000/f_c$ (Upper 2-bit = "00"), $4000/f_c$ (Upper 2-bit = "01"), $16000/f_c$ (Upper 2-bit = "11")

Note 2) The load of $\overline{\text{SCK0}}$ output mode and SO0 output delay time is 50pF.

Fig. 4. Serial transfer CH0 timing



Serial transfer (CH1)(Ta = -10 to +75°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V)

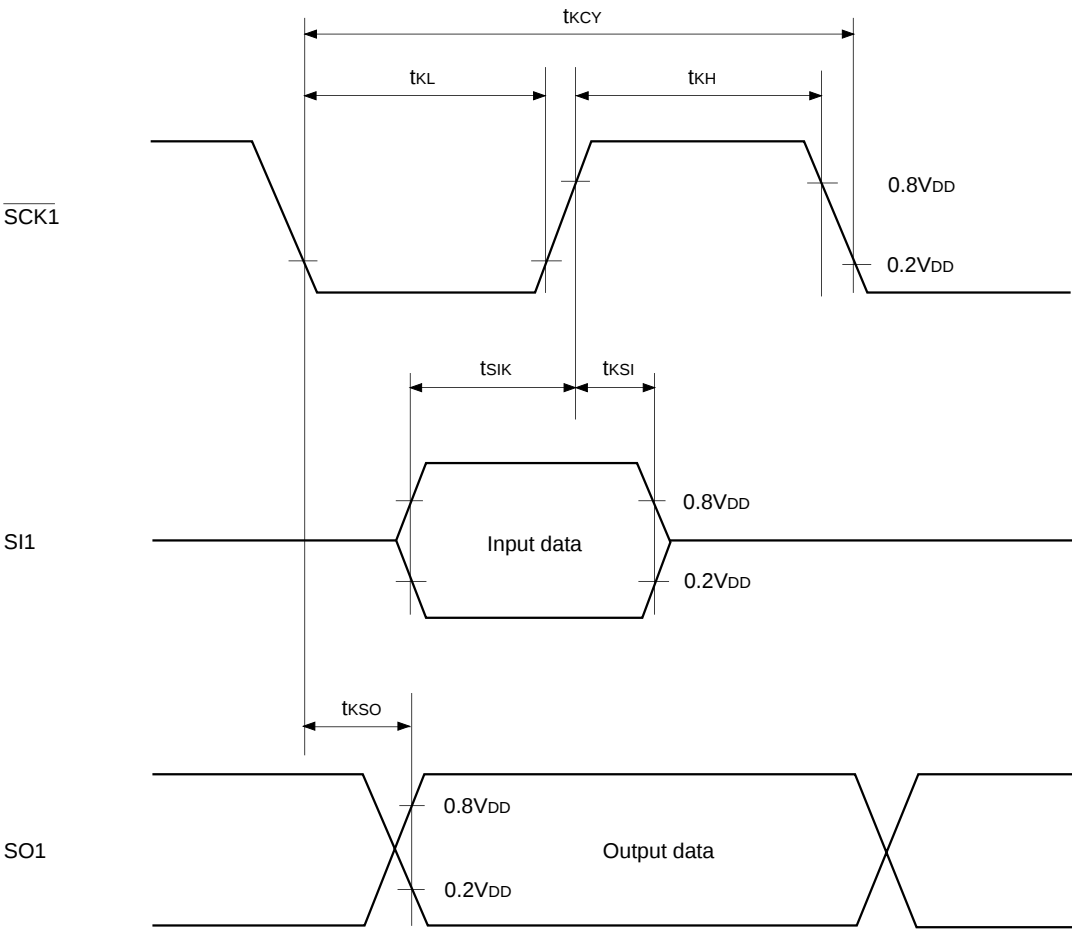
Item	Symbol	Pins	Conditions	Min.	Max.	Unit
$\overline{\text{SCK1}}$ cycle time	t_{KCY}	$\overline{\text{SCK1}}$	Input mode	1000		ns
			Output mode	16000/fc		ns
$\overline{\text{SCK1}}$ high and low level widths	t_{KH} t_{KL}	$\overline{\text{SCK1}}$	Input mode	400		ns
			Output mode	8000/fc – 50		ns
SI1 input setup time (against $\overline{\text{SCK1}}$ ↑)	t_{SIK}	SI1	$\overline{\text{SCK1}}$ input mode	100		ns
			$\overline{\text{SCK1}}$ output mode	200		ns
SI1 input hold time (against $\overline{\text{SCK1}}$ ↑)	t_{KSI}	SI1	$\overline{\text{SCK1}}$ input mode	200		ns
			$\overline{\text{SCK1}}$ output mode	100		ns
$\overline{\text{SCK1}}$ ↓ → SO1 delay time	t_{KSO}	SO1	$\overline{\text{SCK1}}$ input mode		200	ns
			$\overline{\text{SCK1}}$ output mode		100	ns

Note) The load of $\overline{\text{SCK1}}$ output mode and SO1 output delay time is 50pF + 1TTL.**Serial transfer (CH1)**(Ta = -10 to +75°C, V_{DD} = 3.0 to 3.6V, V_{SS} = 0V)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
$\overline{\text{SCK1}}$ cycle time	t_{KCY}	$\overline{\text{SCK1}}$	Input mode	1000		ns
			Output mode	16000/fc		ns
$\overline{\text{SCK1}}$ high and low level widths	t_{KH} t_{KL}	$\overline{\text{SCK1}}$	Input mode	400		ns
			Output mode	8000/fc – 100		ns
SI1 input setup time (against $\overline{\text{SCK1}}$ ↑)	t_{SIK}	SI1	$\overline{\text{SCK1}}$ input mode	100		ns
			$\overline{\text{SCK1}}$ output mode	200		ns
SI1 input hold time (against $\overline{\text{SCK1}}$ ↑)	t_{KSI}	SI1	$\overline{\text{SCK1}}$ input mode	200		ns
			$\overline{\text{SCK1}}$ output mode	100		ns
$\overline{\text{SCK1}}$ ↓ → SO1 delay time	t_{KSO}	SO1	$\overline{\text{SCK1}}$ input mode		250	ns
			$\overline{\text{SCK1}}$ output mode		100	ns

Note) The load of $\overline{\text{SCK1}}$ output mode and SO1 output delay time is 50pF.

Fig. 5. Serial transfer CH1 timing



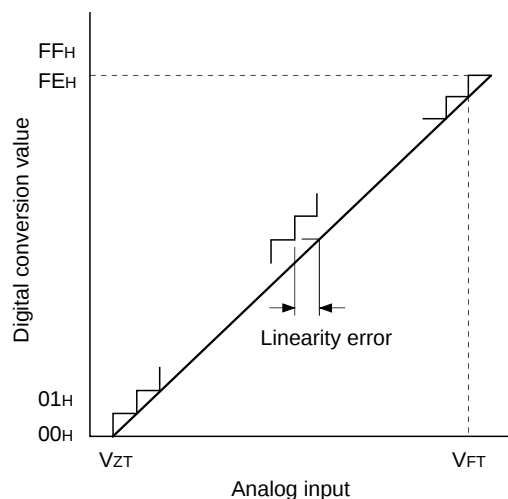
(3) A/D converter characteristics ($T_a = -10$ to $+75^\circ\text{C}$, $V_{DD} = AV_{DD} = 4.5$ to 5.5V , $AV_{REF} = 4.0$ to AV_{DD} , $V_{SS} = AV_{SS} = 0\text{V}$)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			$T_a = 25^\circ\text{C}$ $V_{DD} = AV_{DD} = AV_{REF} = 5.0\text{V}$ $V_{SS} = AV_{SS} = 0\text{V}$			± 1	LSB
Absolute error						± 2	LSB
Conversion time	t_{CONV}			$160/f_{\text{ADC}}^*$			μs
Sampling time	t_{SAMP}			$12/f_{\text{ADC}}^*$			μs
Reference input voltage	V_{REF}	AV_{REF}	$V_{DD} = AV_{DD} = 4.5$ to 5.5V	$AV_{DD} - 0.5$		AV_{DD}	V
Analog input voltage	V_{IAN}	AN0 to AN11		0			V
AVREF current	I_{REF}	AV_{REF}	Operating mode		0.6	1.0	mA
	I_{REFS}		SLEEP mode STOP mode 32kHz operating mode			10	μA

($T_a = -10$ to $+75^\circ\text{C}$, $V_{DD} = AV_{DD} = 3.0$ to 3.6V , $AV_{REF} = 2.7$ to AV_{DD} , $V_{SS} = AV_{SS} = 0\text{V}$)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			$T_a = 25^\circ\text{C}$ $V_{DD} = AV_{DD} = AV_{REF} = 3.3\text{V}$ $V_{SS} = AV_{SS} = 0\text{V}$			± 1	LSB
Absolute error						± 2	LSB
Conversion time	t_{CONV}			$160/f_{\text{ADC}}^*$			μs
Sampling time	t_{SAMP}			$12/f_{\text{ADC}}^*$			μs
Reference input voltage	V_{REF}	AV_{REF}	$V_{DD} = AV_{DD} = 3.0$ to 3.6V	$AV_{DD} - 0.3$		AV_{DD}	V
Analog input voltage	V_{IAN}	AN0 to AN11		0			V
AVREF current	I_{REF}	AV_{REF}	Operating mode		0.4	0.7	mA
	I_{REFS}		SLEEP mode STOP mode 32kHz operating mode			10	μA

Fig. 6. Definitions of A/D converter terms



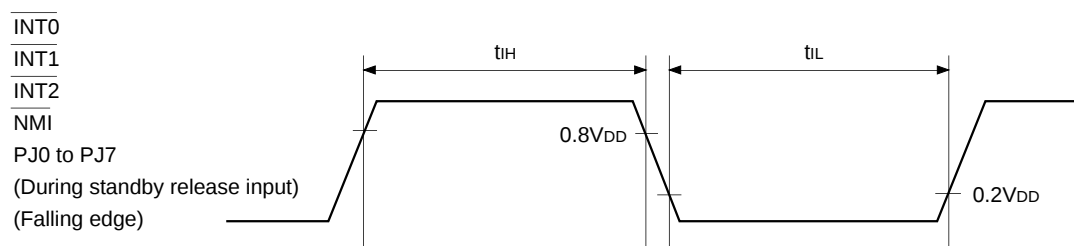
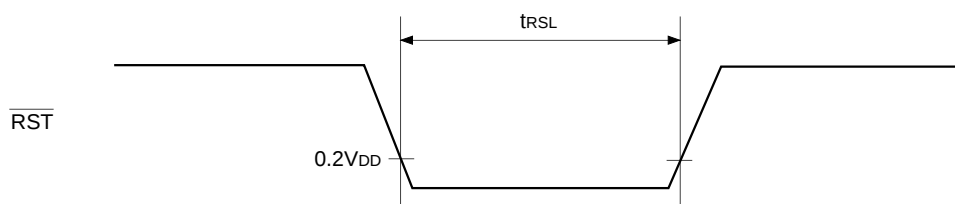
* The value of f_{ADC} is as follows by selecting ADC operation clock (MSC: Address 01FFH bit 0).

When PS2 is selected, $f_{\text{ADC}} = f_c/2$

When PS1 is selected, $f_{\text{ADC}} = f_c$

(4) Interruption, reset input(Ta = -10 to +75°C, V_{DD} = 3.0 to 5.5V, V_{SS} = 0V)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
External interruption high and low level widths	t _{IH} t _{IL}	INT0 INT1 INT2 NMI PJ0 to PJ7		1		μs
Reset input low level width	t _{RSL}	RST		32/fc		μs

Fig. 7. Interruption input timing**Fig. 8. Reset input timing****(5) Others**(Ta = -10 to +75°C, V_{DD} = 3.0 to 5.5V, V_{SS} = 0V)

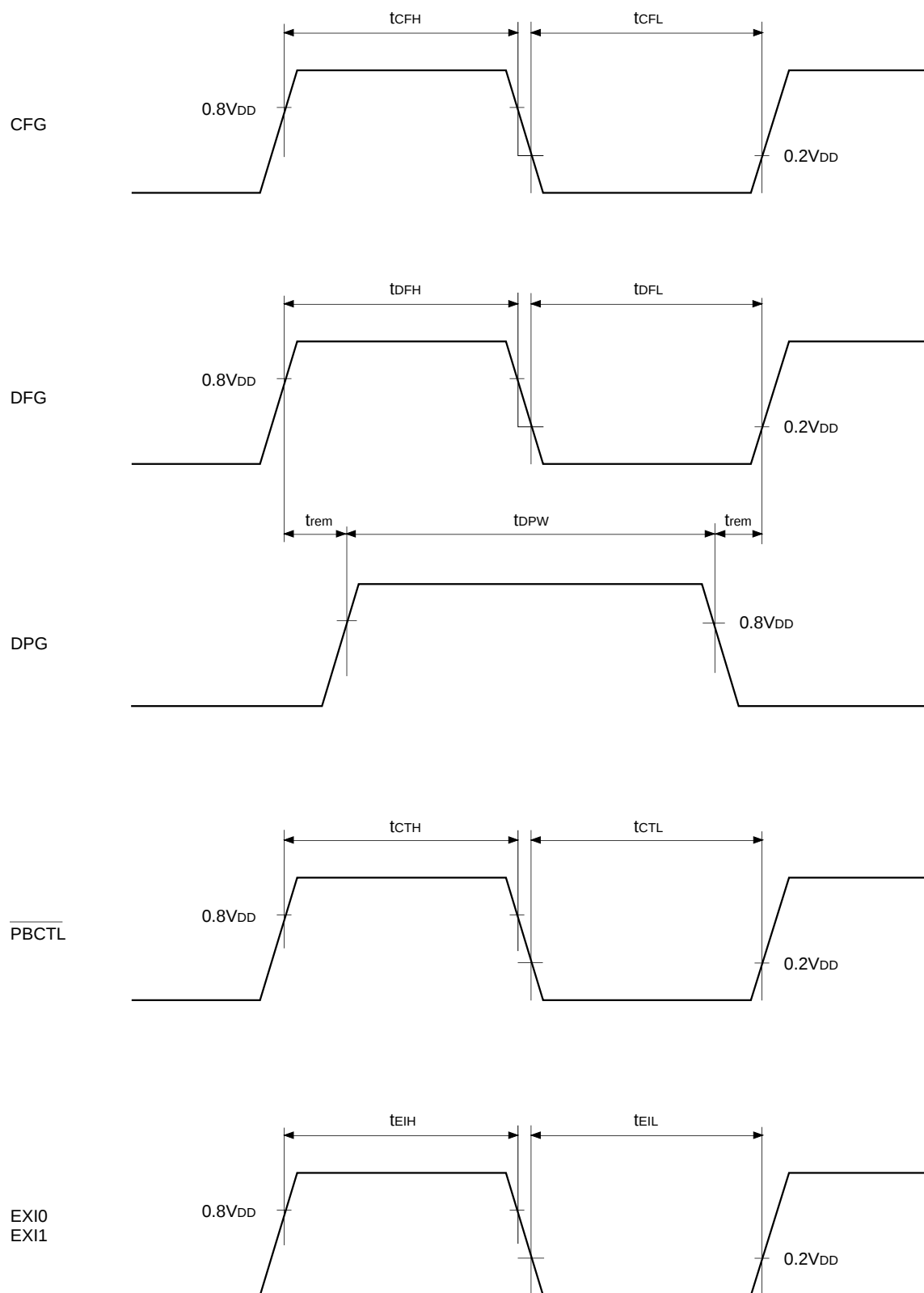
Item	Symbol	Pins	Conditions	Min.	Max.	Unit
CFG input high and low level widths	t _{CFH} t _{CFL}	CFG		t _{FRC} × 24 + 200		ns
DFG input high and low level widths	t _{DFH} t _{DFL}	DFG		t _{FRC} × 8 + 200		ns
DPG minimum pulse width	t _{DPW}	DPG		50		ns
DPG minimum removal time	t _{rem}	DPG		50		ns
PBCTL input high and low level widths	t _{CTH} t _{CTL}	PBCTL	t _{sys} = 2000/fc	t _{FRC} × 8 + 200 + t _{sys}		ns
EXI input high and low level widths	t _{EIH} t _{EIL}	EXI0 EXI1	t _{sys} = 2000/fc	t _{FRC} × 8 + 200 + t _{sys}		ns

Note) t_{sys} indicates three values according to the contents of the clock control register (address; 00FEH) upper 2 bits (CPU clock selection).

t_{sys} [ns] = 2000/fc (Upper 2-bit = "00"), 4000/fc (Upper 2-bit = "01"), 16000/fc (Upper 2-bit = "11")

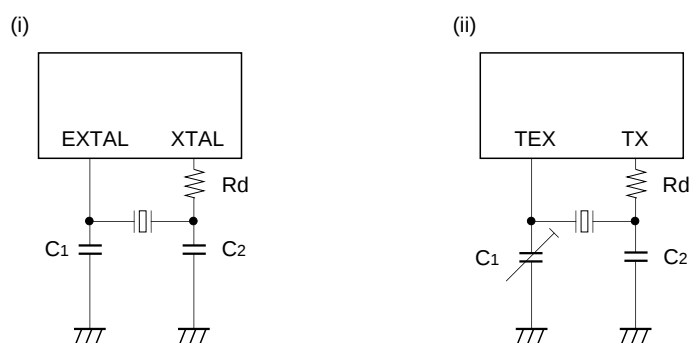
t_{FRC} [ns] = 1000/fc

Fig. 9. Other timings



Supplement

Fig. 10. Recommended oscillation circuit



Manufacturer	Model	fc (MHz)	C ₁ (pF)	C ₂ (pF)	Rd (Ω)	Circuit example
RIVER ELETEC CO., LTD.	HC-49/U03	8.00	10	10	0	(i)
		10.00				
		12.00	5	5		
		16.00				
KINSEKI LTD.	HC-49/U (-S)	8.00	16	12	0	(i)
		10.00	16	12		
		12.00	12	12		
		16.00	12	12	0	
	P3	32.768kHz	30	18	470k	(ii)

Those marked with an asterisk (*) signify types with built-in ground capacitance (C₁, C₂).

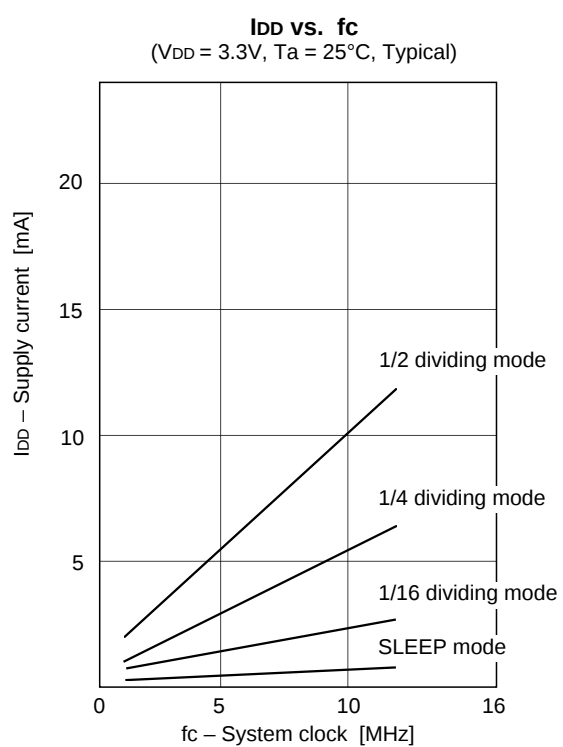
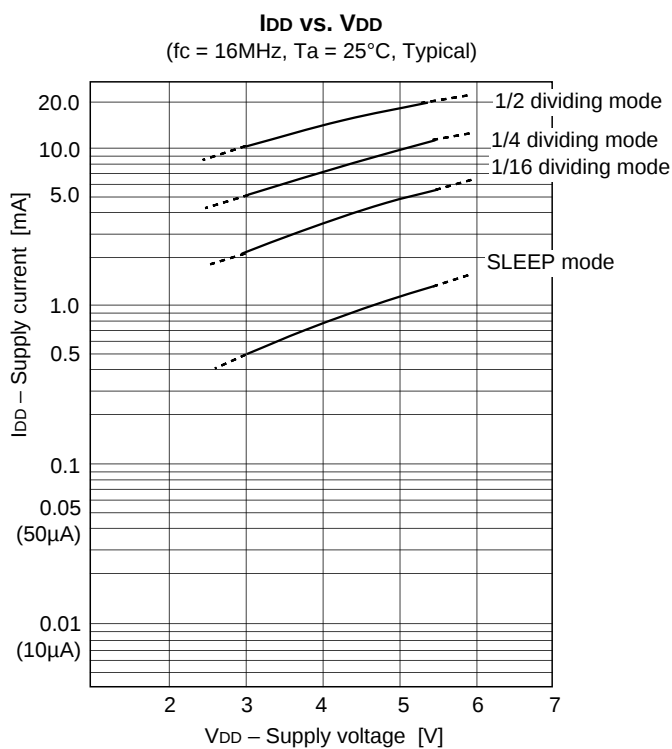
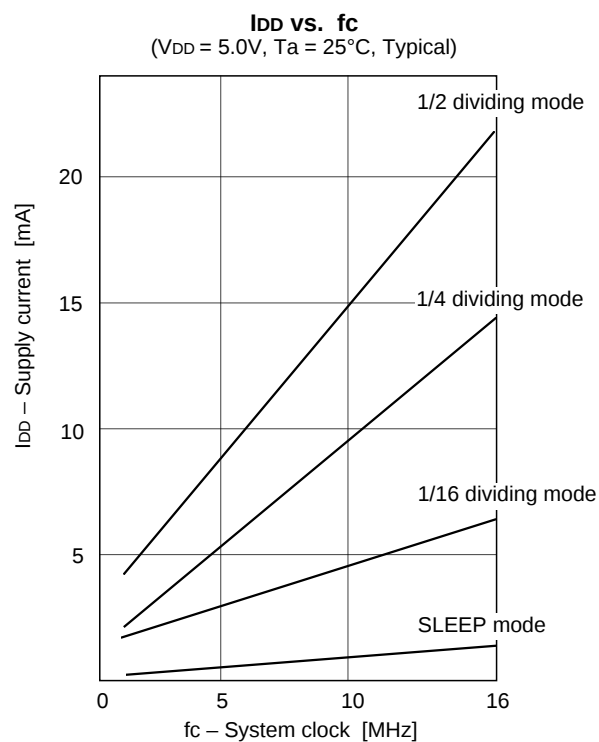
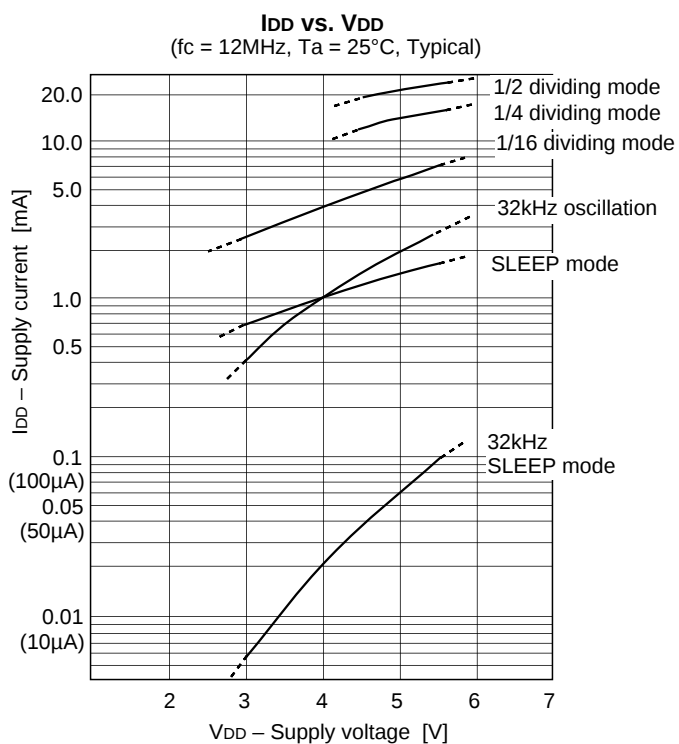
Selection Guide

Option item	Mask product								PROM product			
	CXP 80712A	CXP 80716A	CXP 80720A	CXP 80724A	CXP 80732A	CXP 80740A	CXP 87740A	CXP 87748A	CXP87748 AQ-1-□□□	CXP87748 AR-1-□□□	CXP87748 AQ-2-□□□	CXP87748 AR-2-□□□
Package	100-pin plastic QFP/LQFP								100-pin plastic QFP	100-pin plastic LQFP	100-pin plastic QFP	100-pin plastic LQFP
ROM capacitance	12K byte	16K byte	20K byte	24K byte	32K byte	40K byte	40K byte	48K byte	PROM 48K byte			
RAM capacitance	800 byte						1344 byte		1344 byte			
Reset pin pull- up resistor	Existent/Non-Existent								Existent			
Input circuit format*	CMOS schmitt/TTL schmitt								TTL schmitt		CMOS schmitt	

* In PG4/SYNC0 pin and PG5/SYNC1 pin.

However, TTL schmitt can not be selected when the supply voltage (V_{DD}) ranges from 3.0V to 5.5V.

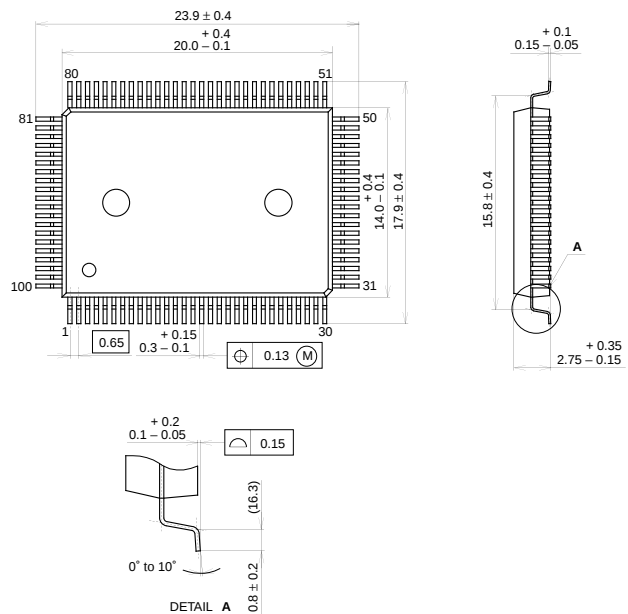
Characteristics Curve



Package Outline

Unit: mm

100PIN QFP (PLASTIC)

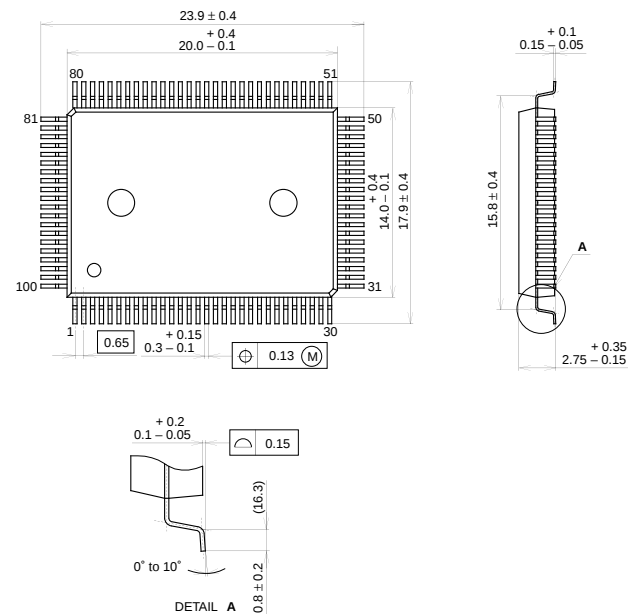


PACKAGE STRUCTURE

SONY CODE	QFP-100P-L01
EIAJ CODE	QFP100-P-1420
JEDEC CODE	

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.7g

100PIN QFP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	QFP-100P-L01
EIAJ CODE	QFP100-P-1420
JEDEC CODE	

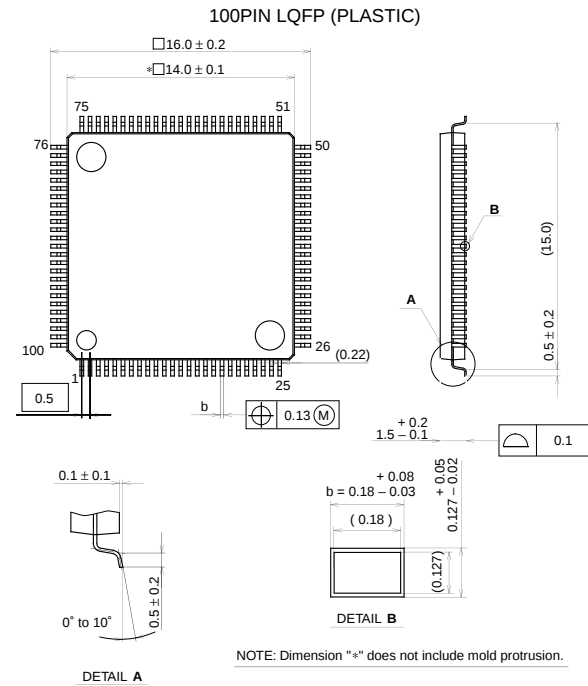
PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.7g

LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	42 ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18μm

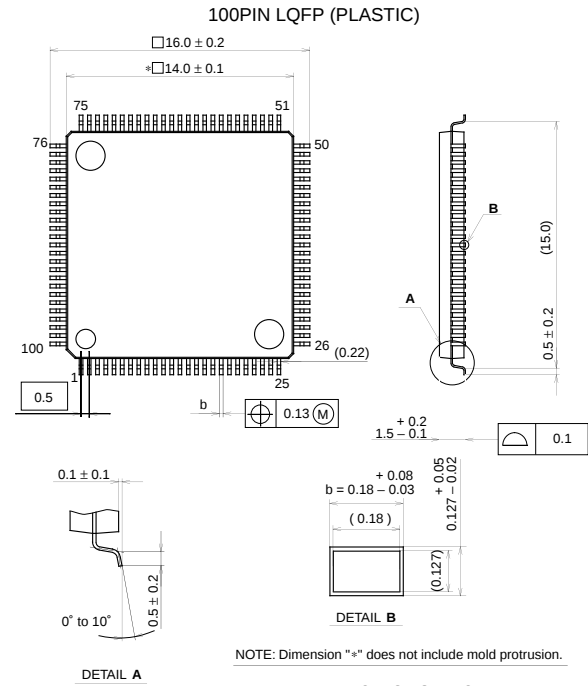
Package Outline

Unit: mm



SONY CODE	LQFP-100P-L01
EIAJ CODE	P-LQFP100-14x14-0.5
JEDEC CODE	

PACKAGE STRUCTURE	
PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 / COPPER ALLOY
PACKAGE MASS	0.7g



SONY CODE	LQFP-100P-L01
EIAJ CODE	P-LQFP100-14x14-0.5
JEDEC CODE	

PACKAGE STRUCTURE	
PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 / COPPER ALLOY
PACKAGE MASS	0.7g

LEAD PLATING SPECIFICATIONS	
ITEM	SPEC.
LEAD MATERIAL	42 ALLOY
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PLATING THICKNESS	5-18μm