To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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RJJ0601JPE

Silicon P Channel MOS FET
High Speed Power Switching

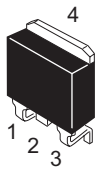
REJ03G1603-0100
Rev.1.00
Nov 21, 2007

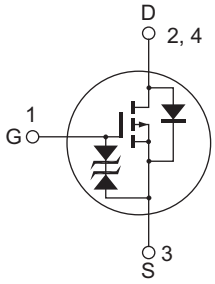
Features

- Low on-resistance
  $R_{DS(on)}$ = 8.2 mΩ typ.
- Capable of 4.5 V gate drive
- High speed switching

Outline

RENESAS Package code: PRSS0004AE-B
(Package name: LDPAK(S)-(1))





1. Gate
2. Drain
3. Source
4. Drain

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Value	Unit
Drain to source voltage	V_{DSS}	–60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	–90	A
Drain peak current	I_D (pulse) Note1	–360	A
Body-drain diode reverse drain current	I_{DR}	–90	A
Avalanche current	I_{AP} Note3	–40	A
Avalanche energy	E_{AR} Note3	137	mJ
Channel dissipation	Pch Note2	90	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Notes: 1. PW ≤ 10 µs, duty cycle ≤ 1%
2. Value at Tc = 25°C
3. Value at Tch = 25°C, Rg ≥ 50 Ω

Thermal Impedance Characteristics

- Channel to case thermal impedance θch-c: 1.39°C/W

Electrical Characteristics

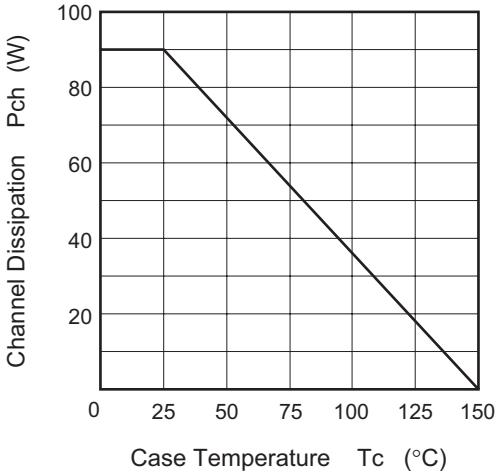
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–60	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–10	µA	V_{DS} = –60 V, V_{GS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–1.0	—	–2.5	V	V_{DS} = –10 V, I_D = –1 mA[Note4]
Forward transfer admittance	$\|y_{fs}\|$	60	100	—	S	I_D = –45 A, V_{DS} = –10 V[Note4]
Static drain to source on state resistance	$R_{DS(on)}$	—	8.2	11	mΩ	I_D = –45 A, V_{GS}= –10 V[Note4]
	$R_{DS(on)}$	—	10	15	mΩ	I_D = –45 A, V_{GS} = –4.5 V[Note4]
Input capacitance	Ciss	—	8800	—	pF	V_{DS} = –10 V, V_{GS} = 0 f = 1 MHz
Output capacitance	Coss	—	950	—	pF	
Reverse transfer capacitance	Crss	—	600	—	pF	
Total gate charge	Qg	—	150	—	nC	V_{DD} = –25 V, V_{GS} = –10 V, I_D = –90 A
Gate to source charge	Qgs	—	25	—	nC	
Gate to drain charge	Qgd	—	23	—	nC	
Turn-on delay time	$t_{d(on)}$	—	25	—	ns	V_{GS} = –10 V, I_D= –45 A, V_{DD} = –30V R_G = 4.7 Ω
Rise time	t_r	—	30	—	ns	
Turn-off delay time	$t_{d(off)}$	—	290	—	ns	
Fall time	t_f	—	135	—	ns	
Body-drain diode forward voltage	V_{DF}	—	–0.96	—	V	I_F = –90 A, V_{GS} = 0
Body-drain diode reverse recovery time	t_{rr}	—	45	—	ns	I_F = –90 A, V_{GS} = 0, di_F/dt = 100 A/µs

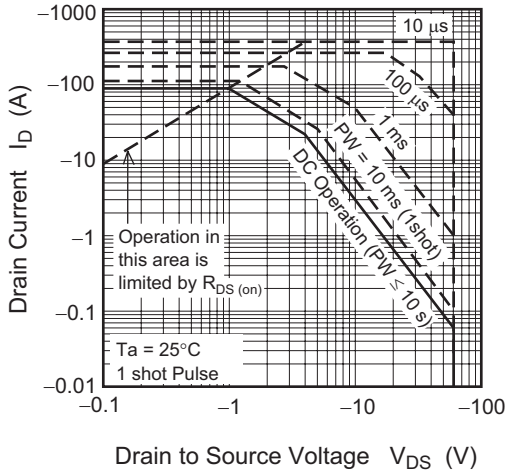
Note: 4. Pulse test

Main Characteristics

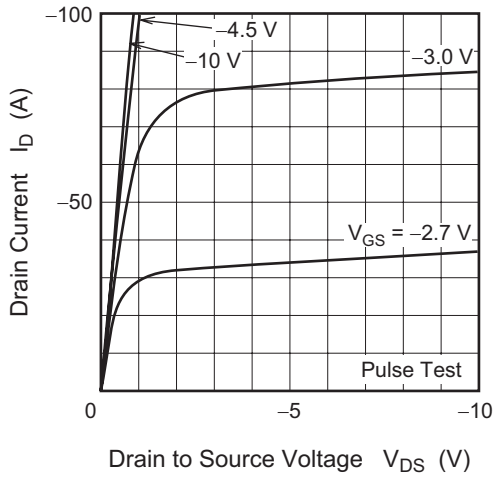
Power vs. Temperature Derating



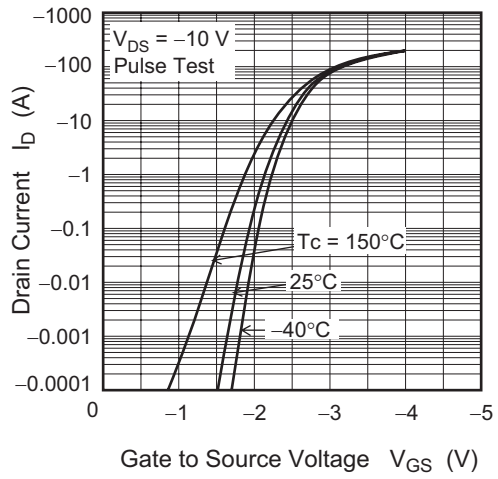
Maximum Safe Operation Area



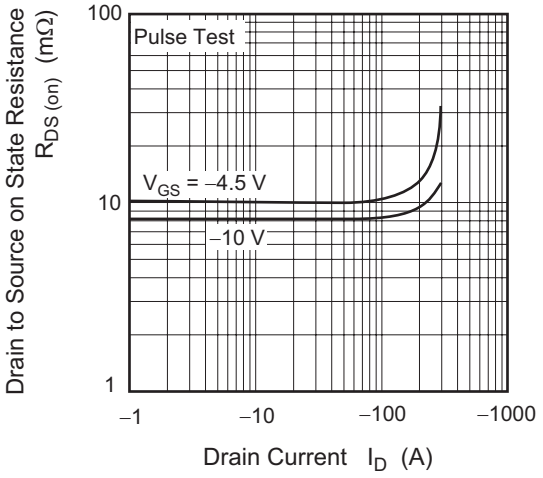
Typical Output Characteristics



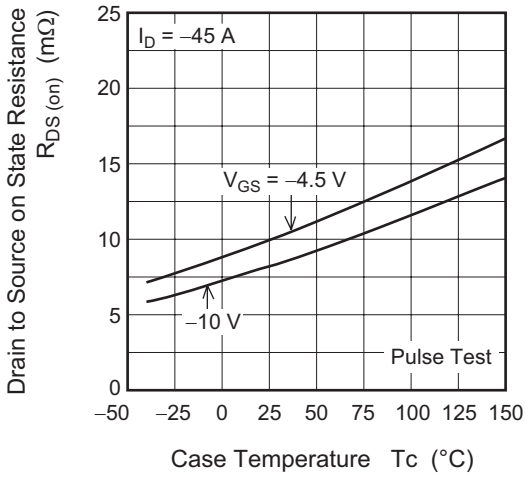
Typical Transfer Characteristics



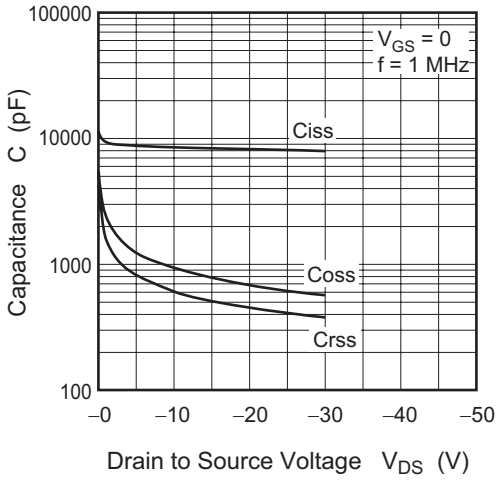
Static Drain to Source on State Resistance vs. Drain Current



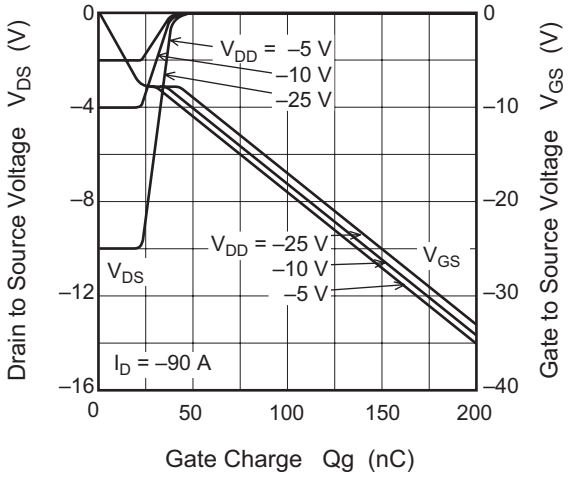
Static Drain to Source on State Resistance vs. Temperature



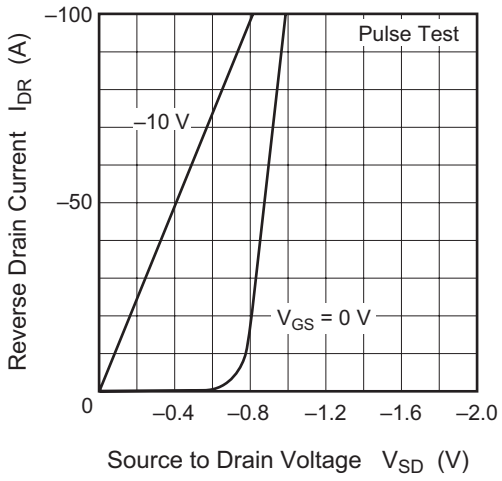
Typical Capacitance vs.
Drain to Source Voltage



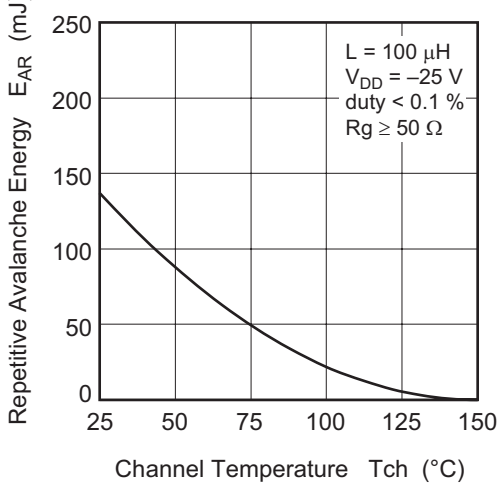
Dynamic Input Characteristics



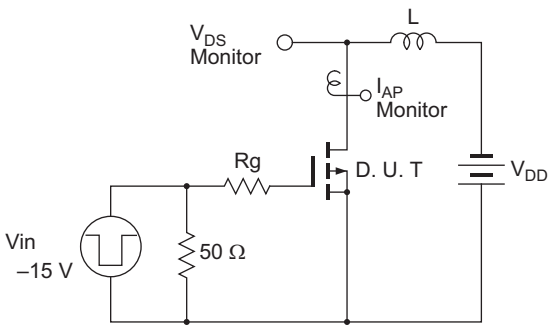
Reverse Drain Current vs.
Source to Drain Voltage



Maximum Avalanche Energy vs.
Channel Temperature Derating

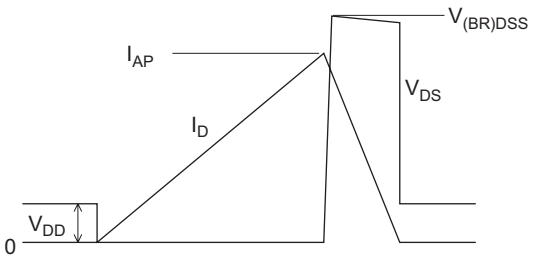


Avalanche Test Circuit

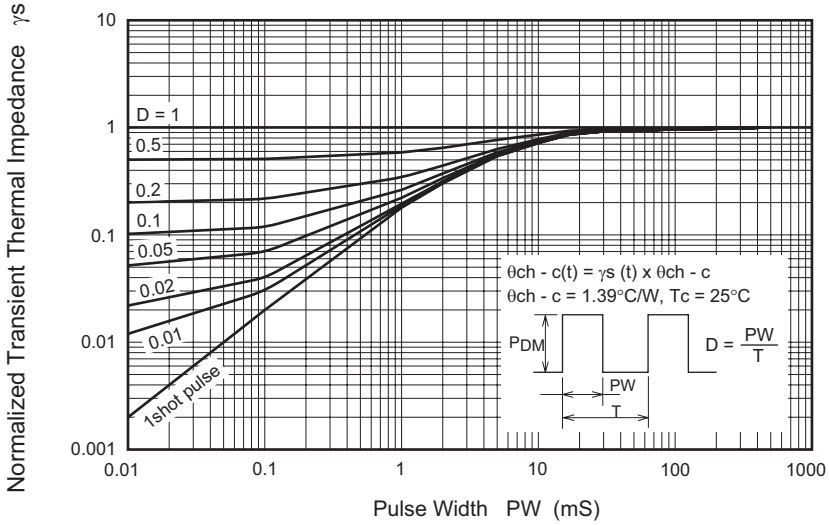


Avalanche Waveform

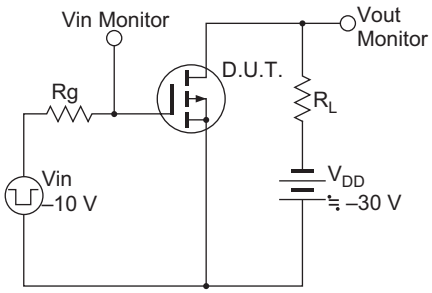
$$E_{AR} = \frac{1}{2} L \bullet I_{AP}^2 \bullet \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



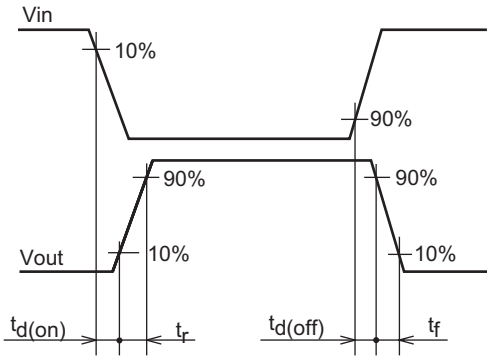
Normalized Transient Thermal Impedance vs. Pulse Width



Switching Time Test Circuit



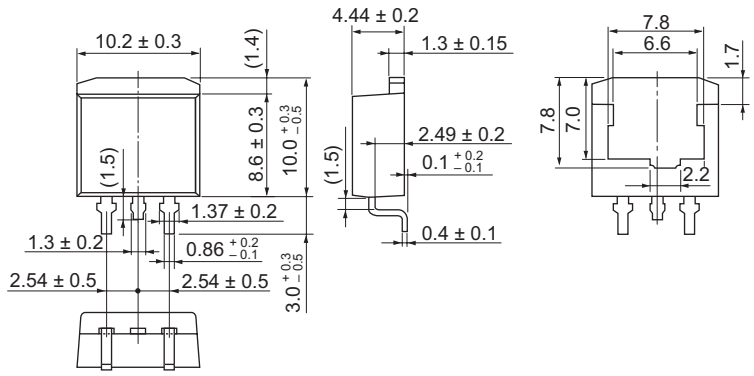
Switching Time Waveform



Package Dimensions

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
LDPAK(S)-(1)	SC-83	PRSS0004AE-B	LDPAK(S)-(1) / LDPAK(S)-(1)V	1.30g

Unit: mm



Ordering Information

Part No.	Quantity	Shipping Container
RJJ0601JPE-00-Q3	1000 pcs	Taping (Dextrorse)
RJJ0601JPE-00-J3	1000 pcs	Taping (Sinistrorse)

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