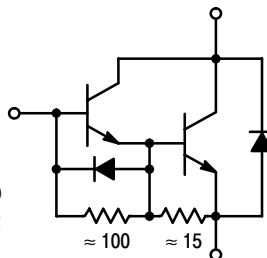**ON Semiconductor**™

SWITCHMODE™ Series NPN Silicon Power Darlington Transistors with Base-Emitter Speedup Diode

The MJ10007 Darlington transistor is designed for high–voltage, high–speed, power switching in inductive circuits where fall time is critical. It is particularly suited for line operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits
- Fast Turn–Off Times
    - 30 ns Inductive Fall Time — 25°C (Typ)
    - 500 ns Inductive Storage Time — 25°C (Typ)
    - Operating Temperature Range –65 to +200°C
- 100°C Performance Specified for:
    - Reversed Biased SOA with Inductive Loads
    - Switching Times with Inductive Loads
    - Saturation Voltages
    - Leakage Currents

MJ10007*

*ON Semiconductor Preferred Device

**10 AMPERE
NPN SILICON
POWER DARLINGTON
TRANSISTORS
400 VOLTS
150 WATTS**
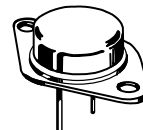
**CASE 1–07
TO–204AA
(TO–3)**

≈ 100   ≈ 15

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	400	Vdc
Collector–Emitter Voltage	V_{CEX}	450	Vdc
Collector–Emitter Voltage	V_{CEV}	500	Vdc
Emitter Base Voltage	V_{EB}	8.0	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	10 20	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	2.5 5.0	Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	150 100 0.86	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.17	°C/W
Maximum Lead Temperature for Soldering Purposes 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%. Designer's and SWITCHMODE are trademarks of ON Semiconductor, Inc.

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (Table 1) ($I_C = 250$ mA, $I_B = 0$, $V_{clamp} = $ Rated V_{CEO})	$V_{CEO(sus)}$	400	—	—	Vdc
Collector–Emitter Sustaining Voltage (Table 1, Figure 12) ($I_C = 1$ A, $V_{clamp} = $ Rated V_{CEX}, $T_C = 100°C$) ($I_C = 5$ A, $V_{clamp} = $ Rated V_{CEX}, $T_C = 100°C$)	$V_{CEX(sus)}$	 450 325	 — —	 — —	Vdc
Collector Cutoff Current ($V_{CEV} = $ Rated Value, $V_{BE(off)} = 1 5$ Vdc) ($V_{CEV} = $ Rated Value, $V_{BE(off)} = 1.5$ Vdc, $T_C = 150°C$)	I_{CEV}	 — —	 — —	 0.25 5.0	mAdc
Collector Cutoff Current ($V_{CE} = $ Rated V_{CEV}, $R_{BE} = 50$ Ω, $T_C = 100°C$)	I_{CER}	—	—	5.0	mAdc
Emitter Cutoff Current ($V_{EB} = 2$ Vdc, $I_C = 0$)	I_{EBO}	—	—	175	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{S/b}$		See Figure 11		
ON CHARACTERISTICS (2)					
DC Current Gain ($I_C = 2.5$ Adc, $V_{CE} = 5.0$ Vdc) ($I_C = 5.0$ Adc, $V_{CE} = 5.0$ Vdc)	h_{FE}	 40 30	 — —	 500 300	—
Collector Emitter Saturation Voltage ($I_C = 5.0$ Adc, $I_B = 250$ mAdc) ($I_C = 10$ Adc, $I_B = 1.0$ Adc) ($I_C = 5.0$ Adc, $I_B = 250$ mAdc, $T_C = 100°C$)	$V_{CE(sat)}$	 — — —	 — — —	 1.9 2.9 2.0	Vdc
Base–Emitter Saturation Voltage ($I_C = 5.0$ Adc, $I_B = 250$ mAdc) ($I_C = 5.0$ Adc, $I_B = 250$ mAdc, $T_C = 100°C$)	$V_{BE(sat)}$	 — —	 — —	 2.5 2.5	Vdc
Diode Forward Voltage (1) ($I_F = 5.0$ Adc)	V_f	—	3.0	5	Vdc
DYNAMIC CHARACTERISTICS					
Small Signal Current Gain ($I_C = 1.0$ Adc, $V_{CE} = 10$ Vdc, $f_{test} = 1.0$ MHz)	h_{fe}	10	—	—	—
Output Capacitance ($V_{CB} = 10$ Vdc, $I_E = 0$, $f_{test} = 100$ kHz)	C_{ob}	60	—	275	pF
SWITCHING CHARACTERISTICS					

Resistive Load (Table 1)

		Symbol	Min	Typ	Max	Unit
Delay Time		t_d	—	0.05	0.2	μs
Rise Time	($V_{CC} = 250$ Vdc, $I_C = 5.0$ A, $I_{B1} = 250$ mA, $V_{BE(off)} = 5.0$ Vdc, $t_p = 50$ μs, Duty Cycle $\leq 2.0\%$)	t_r	—	0.25	0.6	μs
Storage Time		t_s	—	0.5	1.5	μs
Fall Time		t_f	—	0.06	0.5	μs

Inductive Load Clamped (Table 1)

		Symbol	Min	Typ	Max	Unit
Storage Time	($I_C = 5.0$ A(pk), $V_{clamp} = $ Rated V_{CEX}, $I_{B1} = 250$ mA, $V_{BE(off)} = 5.0$ Vdc, $T_C = 100°C$)	t_{sv}	—	0.8	2.0	μs
Crossover Time		t_c	—	0.6	1.5	μs
Storage Time	($I_C = 5.0$ A(pk), $V_{clamp} = $ Rated V_{CEX}, $I_{B1} = 250$ mA, $V_{BE(off)} = 5.0$ Vdc, $T_C = 25°C$)	t_{sv}	—	0.5	—	μs
Crossover Time		t_c	—	0.3	—	μs

(1) The internal Collector–to–Emitter diode can eliminate the need for an external diode to clamp inductive loads.
 Tests have shown that the Forward Recovery Voltage (V_f) of this diode is comparable to that of typical fast recovery rectifiers.

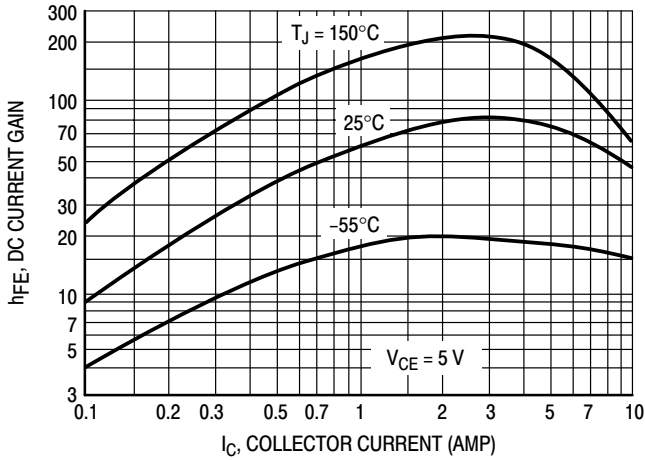(2) Pulse Test: PW = 300 μs, Duty Cycle $\leq 2\%$.
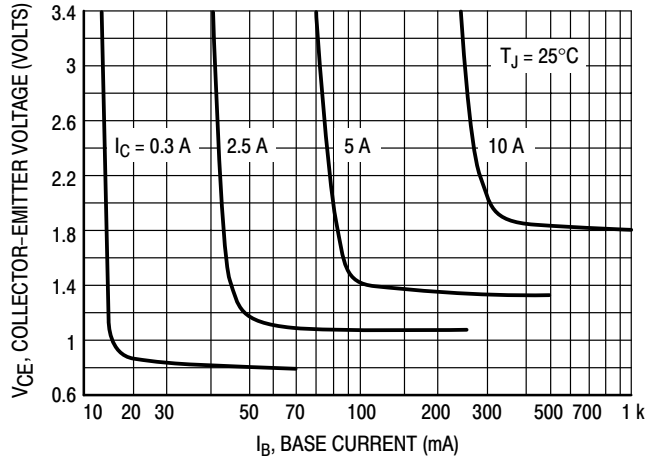
TYPICAL CHARACTERISTICS

Figure 1. DC Current Gain

$T_J = 150°C$ / 25°C / −55°C, $V_{CE} = 5$ V

h_{FE}, DC CURRENT GAIN vs I_C, COLLECTOR CURRENT (AMP)

Figure 2. Collector Saturation Region

$T_J = 25°C$, $I_C = 0.3$ A / 2.5 A / 5 A / 10 A

V_{CE}, COLLECTOR-EMITTER VOLTAGE (VOLTS) vs I_B, BASE CURRENT (mA)
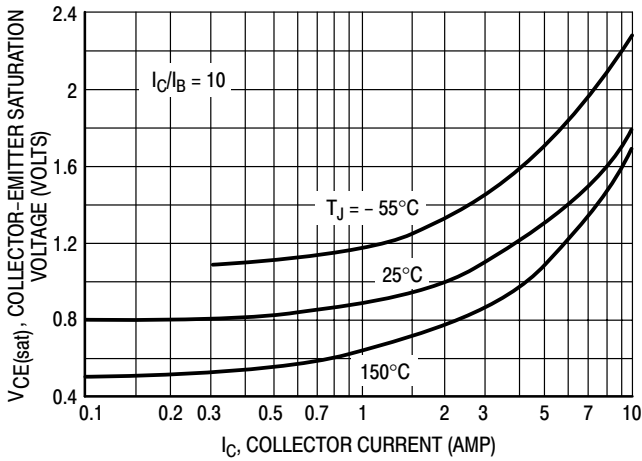
Figure 3. Collector-Emitter Saturation Voltage

$I_C/I_B = 10$, $T_J = -55°C$ / 25°C / 150°C

$V_{CE(sat)}$, COLLECTOR-EMITTER SATURATION VOLTAGE (VOLTS) vs I_C, COLLECTOR CURRENT (AMP)
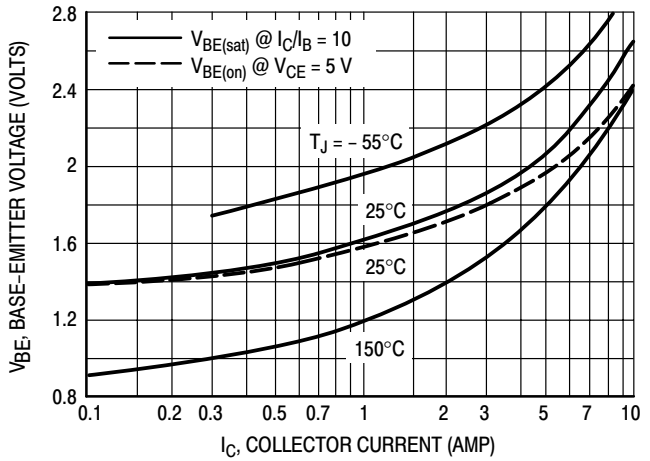
Figure 4. Base-Emitter Voltage

$V_{BE(sat)}$ @ $I_C/I_B = 10$
$V_{BE(on)}$ @ $V_{CE} = 5$ V
$T_J = -55°C$ / 25°C / 25°C / 150°C

V_{BE}, BASE-EMITTER VOLTAGE (VOLTS) vs I_C, COLLECTOR CURRENT (AMP)
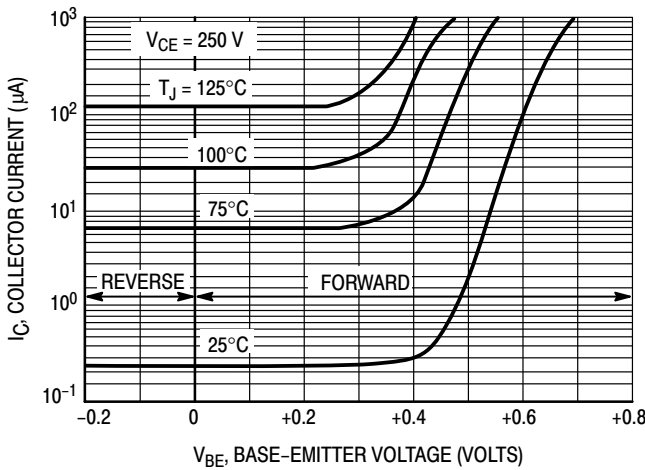
Figure 5. Collector Cutoff Region

$V_{CE} = 250$ V, $T_J = 125°C$ / 100°C / 75°C / 25°C, REVERSE / FORWARD

I_C, COLLECTOR CURRENT (μA) vs V_{BE}, BASE-EMITTER VOLTAGE (VOLTS)
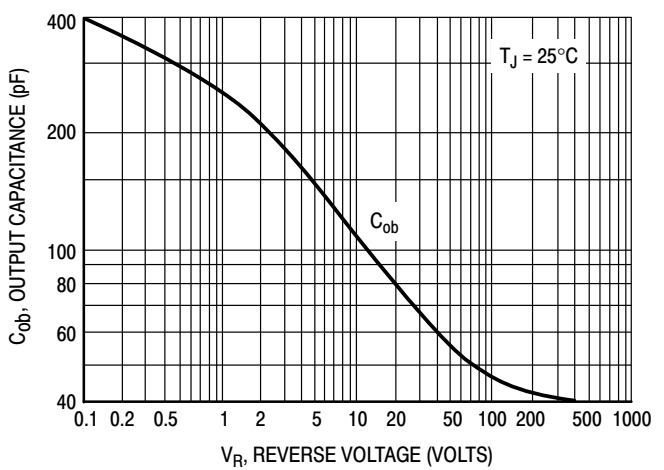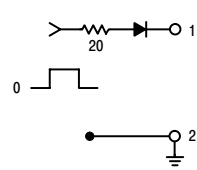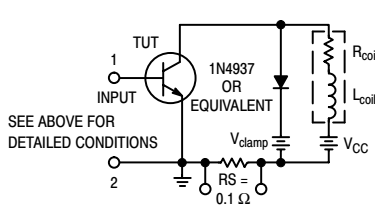
Figure 6. Output Capacitance

$T_J = 25°C$, C_{ob}

C_{ob}, OUTPUT CAPACITANCE (pF) vs V_R, REVERSE VOLTAGE (VOLTS)
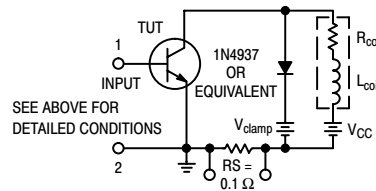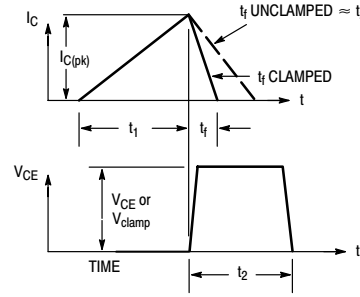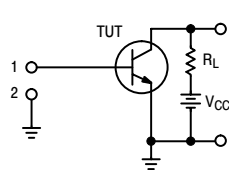
Table 1. Test Conditions for Dynamic Performance

|	$V_{CEO(sus)}$	$V_{CEX(sus)}$ AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	PW Varied to Attain I_C = 250 mA	**INDUCTIVE TEST CIRCUIT**	
CIRCUIT VALUES	L_{coil} = 10 mH, V_{CC} = 10 V R_{coil} = 0.7 Ω V_{clamp} = $V_{CEO(sus)}$	L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V f_o = 500 kHz V_{clamp} = Rated V_{CEX} Value	V_{CC} = 250 V R_L = 50 Ω Pulse Width = 50 μs
TEST CIRCUITS	**INDUCTIVE TEST CIRCUIT**	**OUTPUT WAVEFORMS** t_1 Adjusted to Obtain I_C $t_1 \approx \dfrac{L_{coil}\,(I_{Cpk})}{V_{CC}}$ $t_2 \approx \dfrac{L_{coil}\,(I_{Cpk})}{V_{Clamp}}$ Test Equipment Scope — Tektronix 475 or Equivalent	**RESISTIVE TEST CIRCUIT**
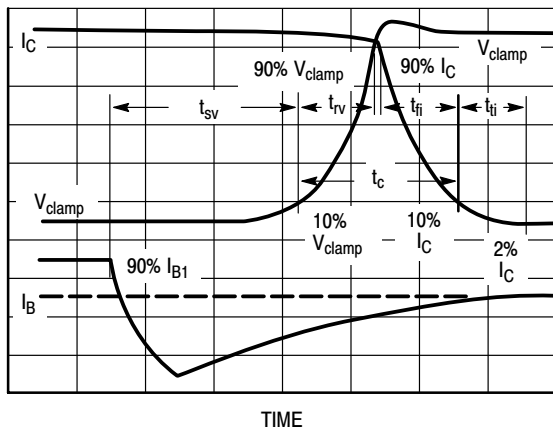
Figure 7. Inductive Switching Measurements

measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the turn–off waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN–222.

$$P_{SWT} = 1/2 \; V_{CC} \; I_C \; (t_c) \; f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.
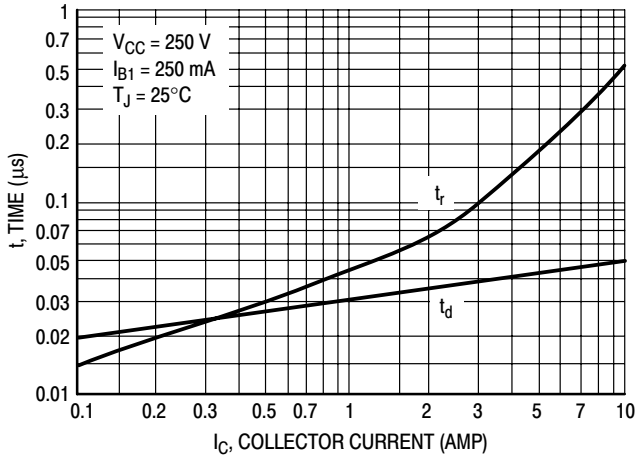
SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate

MJ10007

RESISTIVE SWITCHING PERFORMANCE

Figure 8. Turn–On Time

$V_{CC} = 250$ V
$I_{B1} = 250$ mA
$T_J = 25°C$

t_r
t_d

t, TIME (μs)

I_C, COLLECTOR CURRENT (AMP)

Figure 9. Turn–Off Time

$V_{BE(off)} = 5$ V
$V_{CC} = 250$ V
$I_{B1} = 250$ mA
$T_J = 25°C$

t_s
t_f

t, TIME (μs)

I_C, COLLECTOR CURRENT (AMP)
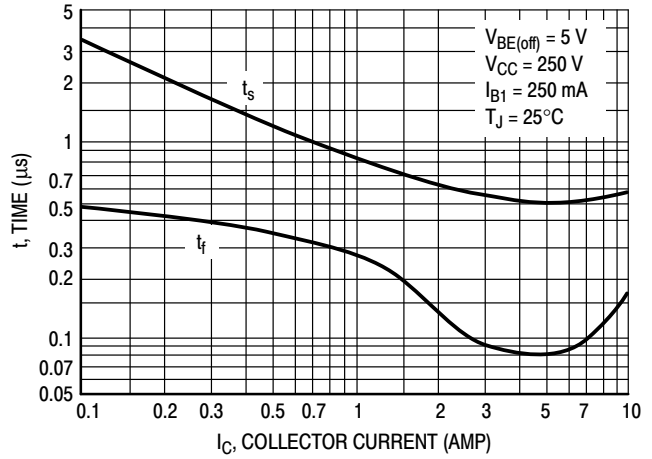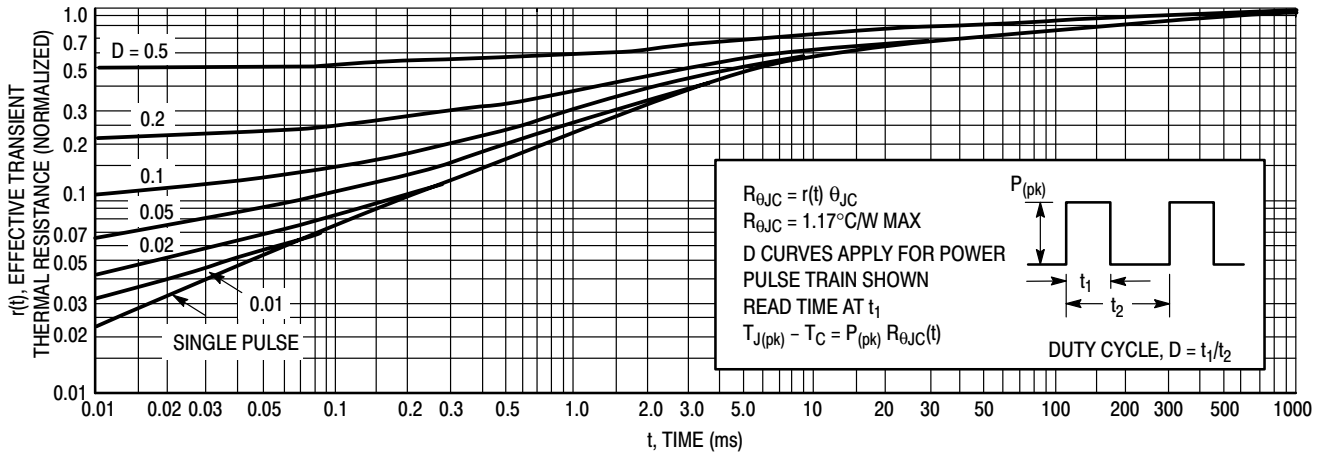
Figure 10. Thermal Response

$r(t)$, EFFECTIVE TRANSIENT THERMAL RESISTANCE (NORMALIZED)

t, TIME (ms)

D = 0.5
0.2
0.1
0.05
0.02
0.01
SINGLE PULSE

$R_{\theta JC} = r(t) \ \theta_{JC}$
$R_{\theta JC} = 1.17°C/W$ MAX
D CURVES APPLY FOR POWER
PULSE TRAIN SHOWN
READ TIME AT t_1
$T_{J(pk)} - T_C = P_{(pk)} \ R_{\theta JC}(t)$

$P_{(pk)}$
t_1
t_2
DUTY CYCLE, D = t_1/t_2

The Safe Operating Area figures shown in Figures 11 and 12 are specified ratings for these devices under the test conditions shown.
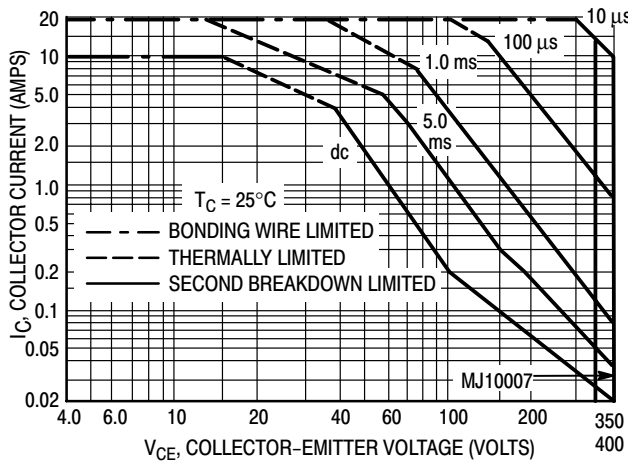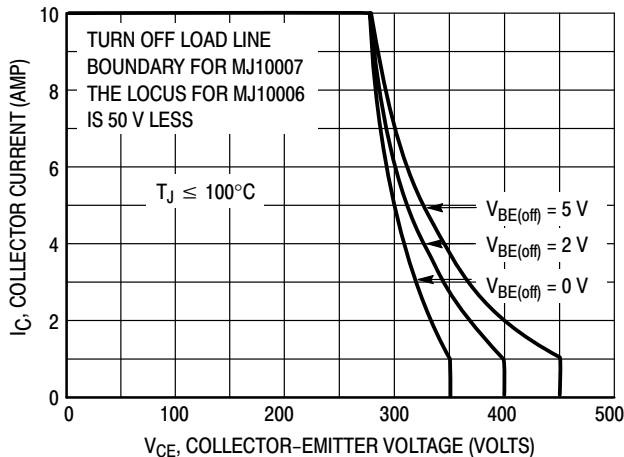

Figure 11. Forward Bias Safe Operating Area
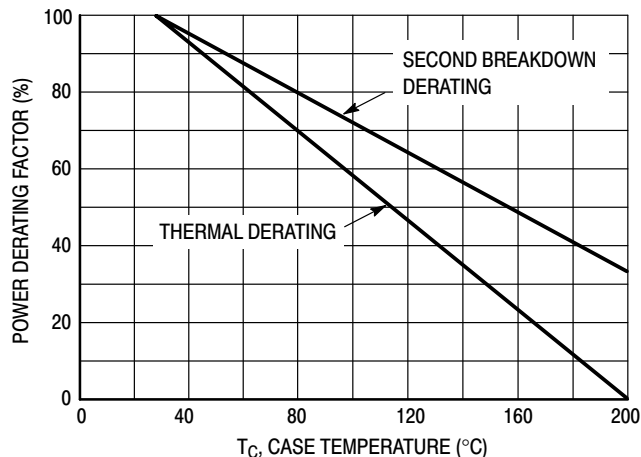

Figure 12. Reverse Bias Switching
Safe Operating Area

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 11 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 11 may be found at any case temperature by using the appropriate curve on Figure 13.

$T_{J(pk)}$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn–off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as $V_{CEX(sus)}$ at a given collector current and represents a voltage–current condition that can be sustained during reverse biased turn–off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 12 gives the complete reverse bias safe operating area characteristics.

Figure 13. Power Derating

MJ10007

PACKAGE DIMENSIONS

TO–204AA (TO–3)
CASE 1–07
ISSUE Z
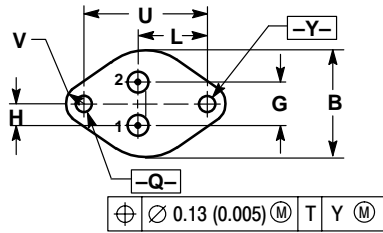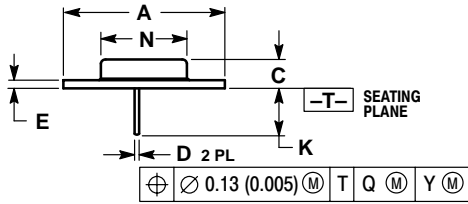
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO–204AA OUTLINE SHALL APPLY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.550 REF		39.37 REF	
B	---	1.050	---	26.67
C	0.250	0.335	6.35	8.51
D	0.038	0.043	0.97	1.09
E	0.055	0.070	1.40	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	---	0.830	---	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

SWITCHMODE is a trademark of Semiconductor Components Industries, LLC.

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