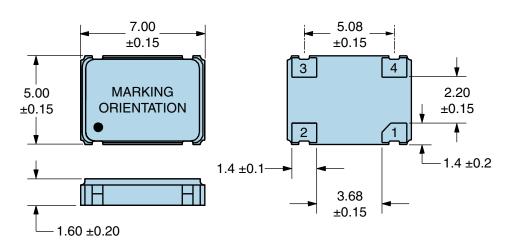


Frequency Tolerance/Stability±50ppm Maximum (Inclusive of all conditions: Calibration Tolerance at 25°C, Frequency Stability over the Operating Temperature Range, Supply Voltage Change, Output Load Change, First Year Aging at 25°CAging at 25°C±50pm/year MaximumOperating Temperature Range-20°C to +70°CSupply Voltage3.3Vdc ±0.3VdcInput Current28mA Maximum (Inclusive of all conditions: Calibration)Output Voltage Logic High (Voh)Vdd-0.4Vdc Minimum (IOH= -8mA)Output Voltage Logic Low (Vol)0.4Vdc Maximum (IOL= +8mA)Rise/Fall Time4nSec Maximum (Measured at 20% to 80% of waveform)Duty Cycle50 ±10(%) (Measured at 50% of waveform)Load Drive Capability15pF MaximumOutput Logic TypeCMOSPin 1 ConnectionTri-State (Disabled Output: High Impedance)Tri-State Input Voltage (Vih and Vii)70% of Vdd Minimum to enable output, 20% of Vdd Maximum to disable output, No Connect to enable output.Standby Current20µA Maximum (Pin 1 = Ground)Disable Current16mA Maximum, ±75pSec TypicalOne Sigma Clock Period Jitter±40pSec MaximumStart Up Time10mSec Maximum	ELECTRICAL SPECIFICATIONS		
Operating Temperature Range, Supply Voltage Change, Output Load Change, First Year Aging at 25°CAging at 25°C±5ppm/year MaximumOperating Temperature Range-20°C to +70°CSupply Voltage3.3Vdc ±0.3VdcInput Current28mA Maximum (Unloaded)Output Voltage Logic High (Voh)Vdd-0.4Vdc Minimum (IOH= -8mA)Output Voltage Logic Low (Vol)0.4Vdc Maximum (IOL= +8mA)Rise/Fall Time4nSec Maximum (Measured at 20% to 80% of waveform)Duty Cycle50 ±10(%) (Measured at 50% of waveform)Load Drive Capability15pF MaximumOutput Logic TypeCMOSPin 1 ConnectionTri-State [Disabled Output: High Impedance)Tri-State Input Voltage (Vih and Vil)70% of Vdd Minimum to enable output, 20% of Vdd Maximum to disable output, No Connect to enable output.Standby Current20µA Maximum (Pin 1 = Ground)Absolute Clock Jitter±125pSec Maximum, ±75pSec TypicalOne Sigma Clock Period Jitter±40pSec Maximum	Nominal Frequency	74.1758MHz	
Operating Temperature Range       -20°C to +70°C         Supply Voltage       3.3Vdc ±0.3Vdc         Input Current       28mA Maximum (Unloaded)         Output Voltage Logic High (Voh)       Vdd-0.4Vdc Minimum (IOH= -8mA)         Output Voltage Logic Low (Vol)       0.4Vdc Maximum (IOL= +8mA)         Rise/Fall Time       4nSec Maximum (Measured at 20% to 80% of waveform)         Duty Cycle       50 ±10(%) (Measured at 50% of waveform)         Load Drive Capability       15pF Maximum         Output Logic Type       CMOS         Pin 1 Connection       Tri-State (Disabled Output: High Impedance)         Tri-State Input Voltage (Vih and Vil)       70% of Vdd Minimum to enable output, 20% of Vdd Maximum to disable output, No Connect to enable output.         Standby Current       20µA Maximum (Pin 1 = Ground)         Disable Current       16mA Maximum, ±75pSec Typical         Absolute Clock Jitter       ±125pSec Maximum, ±75pSec Typical         Cone Sigma Clock Period Jitter       ±40pSec Maximum	Frequency Tolerance/Stability	Operating Temperature Range, Supply Voltage Change, Output Load Change,	
Supply Voltage3.3Vdc ±0.3VdcInput Current28mA Maximum (Unloaded)Output Voltage Logic High (Voh)Vdd-0.4Vdc Minimum (IOH= -8mA)Output Voltage Logic Low (Vol)0.4Vdc Maximum (IOL= +8mA)Rise/Fall Time4nSec Maximum (Measured at 20% to 80% of waveform)Duty Cycle50 ±10(%) (Measured at 50% of waveform)Load Drive Capability15pF MaximumOutput Logic TypeCMOSPin 1 ConnectionTri-State (Disabled Output: High Impedance)Tri-State Input Voltage (Vih and Vil)70% of Vdd Minimum to enable output, 20% of Vdd Maximum to disable output, No Connect to enable output.Standby Current20µA Maximum (Pin 1 = Ground)Absolute Clock Jitter±125pSec Maximum, ±75pSec TypicalOne Sigma Clock Period Jitter±40pSec MaximumStart Up Time10mSec Maximum	Aging at 25°C	±5ppm/year Maximum	
Input Current28mA Maximum (Unloaded)Output Voltage Logic High (Voh)Vdd-0.4Vdc Minimum (IOH= -8mA)Output Voltage Logic Low (Vol)0.4Vdc Maximum (IOL= +8mA)Rise/Fall Time4nSec Maximum (Measured at 20% to 80% of waveform)Duty Cycle50 ±10(%) (Measured at 50% of waveform)Load Drive Capability15pF MaximumOutput Logic TypeCMOSPin 1 ConnectionTri-State (Disabled Output: High Impedance)Tri-State Input Voltage (Vih and Vil)70% of Vdd Minimum to enable output, 20% of Vdd Maximum to disable output, No Connect to enable output.Standby Current20µA Maximum (Pin 1 = Ground)Disable Current16mA Maximum (Pin 1 = Ground)Absolute Clock Jitter±125pSec Maximum, ±75pSec Typical±40pSec Maximum10mSec Maximum	Operating Temperature Range	-20°C to +70°C	
Output Voltage Logic High (Voh)Vdd-0.4Vdc Minimum (IOH= -8mA)Output Voltage Logic Low (Vol)0.4Vdc Maximum (IOL= +8mA)Rise/Fall Time4nSec Maximum (Measured at 20% to 80% of waveform)Duty Cycle50 ±10(%) (Measured at 50% of waveform)Load Drive Capability15pF MaximumOutput Logic TypeCMOSPin 1 ConnectionTri-State (Disabled Output: High Impedance)Tri-State Input Voltage (Vih and Vil)70% of Vdd Minimum to enable output, 20% of Vdd Maximum to disable output, No Connect to enable output.Standby Current20µA Maximum (Pin 1 = Ground)Disable Current16mA Maximum, ±75pSec TypicalOne Sigma Clock Period Jitter±40pSec MaximumStart Up Time10mSec Maximum	Supply Voltage	3.3Vdc ±0.3Vdc	
Output Voltage Logic Low (Vol)0.4Vdc Maximum (IOL= +8mA)Rise/Fall Time4nSec Maximum (Measured at 20% to 80% of waveform)Duty Cycle50 ±10(%) (Measured at 50% of waveform)Load Drive Capability15pF MaximumOutput Logic TypeCMOSPin 1 ConnectionTri-State (Disabled Output: High Impedance)Tri-State Input Voltage (Vih and Vil)70% of Vdd Minimum to enable output, 20% of Vdd Maximum to disable output, No Connect to enable output.Standby Current20µA Maximum (Pin 1 = Ground)Disable Current16mA Maximum (Pin 1 = Ground)Absolute Clock Jitter±125pSec Maximum, ±75pSec TypicalOne Sigma Clock Period Jitter±40pSec MaximumStart Up Time10mSec Maximum	Input Current	28mA Maximum (Unloaded)	
Rise/Fall Time4nSec Maximum (Measured at 20% to 80% of waveform)Duty Cycle50 ±10(%) (Measured at 50% of waveform)Load Drive Capability15pF MaximumOutput Logic TypeCMOSPin 1 ConnectionTri-State (Disabled Output: High Impedance)Tri-State Input Voltage (Vih and Vil)70% of Vdd Minimum to enable output, 20% of Vdd Maximum to disable output, No Connect to enable output.Standby Current20µA Maximum (Pin 1 = Ground)Disable Current16mA Maximum (Pin 1 = Ground)Absolute Clock Jitter±125pSec Maximum, ±75pSec TypicalOne Sigma Clock Period Jitter±40pSec MaximumOutput Time10mSec Maximum	Output Voltage Logic High (Voh)	Vdd-0.4Vdc Minimum (IOH= -8mA)	
Duty Cycle50 ±10(%) (Measured at 50% of waveform)Load Drive Capability15pF MaximumOutput Logic TypeCMOSPin 1 ConnectionTri-State (Disabled Output: High Impedance)Tri-State Input Voltage (Vih and Vil)70% of Vdd Minimum to enable output, 20% of Vdd Maximum to disable output, No Connect to enable output.Standby Current20µA Maximum (Pin 1 = Ground)Disable Current16mA Maximum (Pin 1 = Ground)Absolute Clock Jitter±125pSec Maximum, ±75pSec TypicalOne Sigma Clock Period Jitter±40pSec Maximum	Output Voltage Logic Low (Vol)	0.4Vdc Maximum (IOL= +8mA)	
Load Drive Capability15pF MaximumOutput Logic TypeCMOSPin 1 ConnectionTri-State (Disabled Output: High Impedance)Tri-State Input Voltage (Vih and Vil)70% of Vdd Minimum to enable output, 20% of Vdd Maximum to disable output, No Connect to enable output.Standby Current20µA Maximum (Pin 1 = Ground)Disable Current16mA Maximum (Pin 1 = Ground)Absolute Clock Jitter±125pSec Maximum, ±75pSec TypicalOne Sigma Clock Period Jitter±40pSec MaximumStart Up Time10mSec Maximum	Rise/Fall Time	4nSec Maximum (Measured at 20% to 80% of waveform)	
Output Logic TypeCMOSPin 1 ConnectionTri-State (Disabled Output: High Impedance)Tri-State Input Voltage (Vih and Vil)70% of Vdd Minimum to enable output, 20% of Vdd Maximum to disable output, No Connect to enable output.Standby Current20µA Maximum (Pin 1 = Ground)Disable Current16mA Maximum (Pin 1 = Ground)Absolute Clock Jitter±125pSec Maximum, ±75pSec TypicalOne Sigma Clock Period Jitter±40pSec MaximumStart Up Time10mSec Maximum	Duty Cycle	50 ±10(%) (Measured at 50% of waveform)	
Pin 1 ConnectionTri-State (Disabled Output: High Impedance)Tri-State Input Voltage (Vih and Vil)70% of Vdd Minimum to enable output, 20% of Vdd Maximum to disable output, No Connect to enable output.Standby Current20μA Maximum (Pin 1 = Ground)Disable Current16mA Maximum (Pin 1 = Ground)Absolute Clock Jitter±125pSec Maximum, ±75pSec TypicalOne Sigma Clock Period Jitter±40pSec MaximumStart Up Time10mSec Maximum	Load Drive Capability	15pF Maximum	
Tri-State Input Voltage (Vih and Vil)70% of Vdd Minimum to enable output, 20% of Vdd Maximum to disable output, No Connect to enable output.Standby Current20µA Maximum (Pin 1 = Ground)Disable Current16mA Maximum (Pin 1 = Ground)Absolute Clock Jitter±125pSec Maximum, ±75pSec TypicalOne Sigma Clock Period Jitter±40pSec MaximumStart Up Time10mSec Maximum	Output Logic Type	CMOS	
output.       Standby Current     20µA Maximum (Pin 1 = Ground)       Disable Current     16mA Maximum (Pin 1 = Ground)       Absolute Clock Jitter     ±125pSec Maximum, ±75pSec Typical       One Sigma Clock Period Jitter     ±40pSec Maximum       Start Up Time     10mSec Maximum	Pin 1 Connection	Tri-State (Disabled Output: High Impedance)	
Disable Current       16mA Maximum (Pin 1 = Ground)         Absolute Clock Jitter       ±125pSec Maximum, ±75pSec Typical         One Sigma Clock Period Jitter       ±40pSec Maximum         Start Up Time       10mSec Maximum	Tri-State Input Voltage (Vih and Vil)		
Absolute Clock Jitter     ±125pSec Maximum, ±75pSec Typical       One Sigma Clock Period Jitter     ±40pSec Maximum       Start Up Time     10mSec Maximum	Standby Current	20μA Maximum (Pin 1 = Ground)	
One Sigma Clock Period Jitter     ±40pSec Maximum       Start Up Time     10mSec Maximum	Disable Current	16mA Maximum (Pin 1 = Ground)	
Start Up Time 10mSec Maximum	Absolute Clock Jitter	±125pSec Maximum, ±75pSec Typical	
	One Sigma Clock Period Jitter	±40pSec Maximum	
Storage Temperature Range -55°C to +125°C	Start Up Time	10mSec Maximum	
	Storage Temperature Range	-55°C to +125°C	

ENVIRONMENTAL & MECHANICAL SPECIFICATIONS		
ESD Susceptibility	MIL-STD-883, Method 3015, Class 1, HBM: 1500V	
Fine Leak Test	MIL-STD-883, Method 1014, Condition A	
Flammability	UL94-V0	
Gross Leak Test	MIL-STD-883, Method 1014, Condition C	
Mechanical Shock	MIL-STD-883, Method 2002, Condition B	
Moisture Resistance	MIL-STD-883, Method 1004	
Moisture Sensitivity	J-STD-020, MSL 1	
Resistance to Soldering Heat	MIL-STD-202, Method 210, Condition K	
Resistance to Solvents	MIL-STD-202, Method 215	
Solderability	MIL-STD-883, Method 2003	
Temperature Cycling	MIL-STD-883, Method 1010, Condition B	
Vibration	MIL-STD-883, Method 2007, Condition A	

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### **MECHANICAL DIMENSIONS (all dimensions in millimeters)**



PIN	CONNECTION
1	Tri-State (High Impedance)
2	Ground/Case Ground
3	Output
4	Supply Voltage
	MADKING
LINE	MARKING
LINE 1	MARKING ECLIPTEK

K

#### Suggested Solder Pad Layout

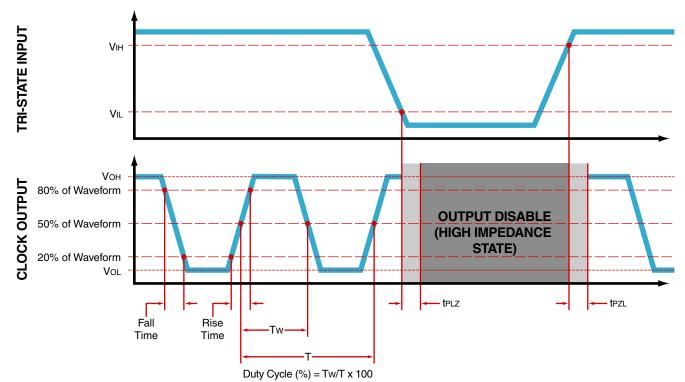
All Dimensions in Millimeters



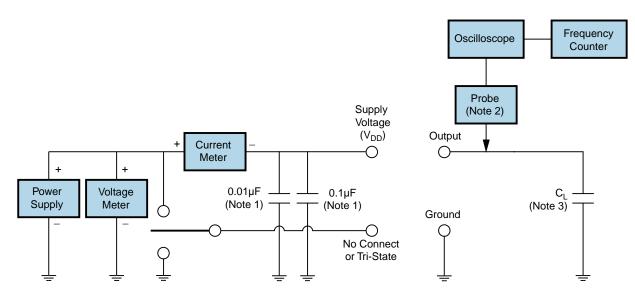
All Tolerances are ±0.1

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Note 1: An external  $0.1\mu$ F low frequency tantalum bypass capacitor in parallel with a  $0.01\mu$ F high frequency ceramic bypass capacitor close to the package ground and V<sub>DD</sub> pin is required.

Note 2: A low capacitance (<12pF), 10X attenuation factor, high impedance (>10Mohms), and high bandwidth (>300MHz) passive probe is recommended.

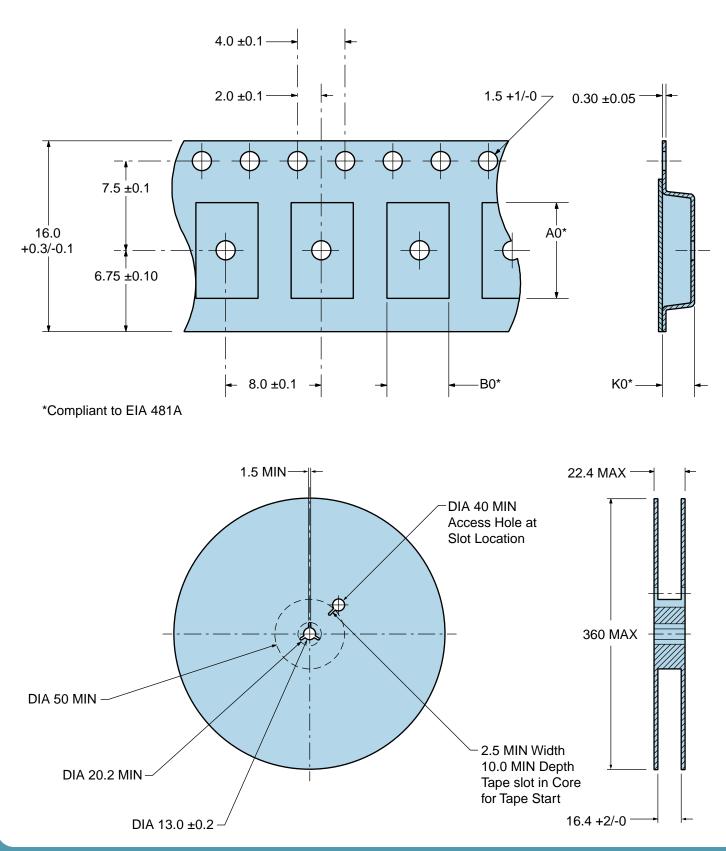
Note 3: Capacitance value  $\dot{C}_L$  includes sum of all probe and fixture capacitance.

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## Tape & Reel Dimensions

Quantity Per Reel: 1,000 Units



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## **Recommended Solder Reflow Methods**

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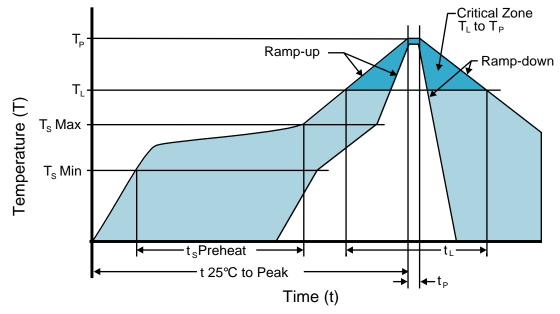
### **High Temperature Infrared/Convection**

$T_s$ MAX to $T_L$ (Ramp-up Rate)	3°C/second Maximum
Preheat	
- Temperature Minimum (Ts MIN)	150°C
- Temperature Typical (T <sub>s</sub> TYP)	175°C
<ul> <li>Temperature Maximum (T<sub>s</sub> MAX)</li> </ul>	200°C
- Time (t <sub>s</sub> MIN)	60 - 180 Seconds
Ramp-up Rate (T <sub>L</sub> to T <sub>P</sub> )	3°C/second Maximum
Time Maintained Above:	
- Temperature (T∟)	217°C
- Time (t∟)	60 - 150 Seconds
Peak Temperature (T <sub>P</sub> )	260°C Maximum for 10 Seconds Maximum
Target Peak Temperature (T <sub>P</sub> Target)	250°C +0/-5°C
Time within 5°C of actual peak ( $t_p$ )	20 - 40 seconds
Ramp-down Rate	6°C/second Maximum
Time 25°C to Peak Temperature (t)	8 minutes Maximum
Moisture Sensitivity Level	Level 1
Additional Notes	Temperatures shown are applied to body of device.



## **Recommended Solder Reflow Methods**

EP2645TS-74.1758M TR



### Low Temperature Infrared/Convection 240°C

$T_s$ MAX to $T_L$ (Ramp-up Rate)	5°C/second Maximum
Preheat	
- Temperature Minimum (T <sub>s</sub> MIN)	N/A
- Temperature Typical (T <sub>s</sub> TYP)	150°C
- Temperature Maximum (T <sub>s</sub> MAX)	N/A
- Time (t <sub>s</sub> MIN)	60 - 120 Seconds
Ramp-up Rate (T⊾ to T <sub>P</sub> )	5°C/second Maximum
Time Maintained Above:	
- Temperature (T∟)	150°C
- Time (t∟)	200 Seconds Maximum
Peak Temperature (T <sub>P</sub> )	240°C Maximum
Target Peak Temperature (T <sub>P</sub> Target)	240°C Maximum 1 Time / 230°C Maximum 2 Times
Time within 5°C of actual peak (t <sub>p</sub> )	10 seconds Maximum 2 Times / 80 seconds Maximum 1 Time
Ramp-down Rate	5°C/second Maximum
Time 25°C to Peak Temperature (t)	N/A
Moisture Sensitivity Level	Level 1
Additional Notes	Temperatures shown are applied to body of device.

#### Low Temperature Manual Soldering

185°C Maximum for 10 seconds Maximum, 2 times Maximum. (Temperatures shown are applied to body of device.)

### High Temperature Manual Soldering

260°C Maximum for 5 seconds Maximum, 2 times Maximum. (Temperatures shown are applied to body of device.)