DENSE-PAC
MICROSYSTEMS

8 Megabit FLASH EEPROM

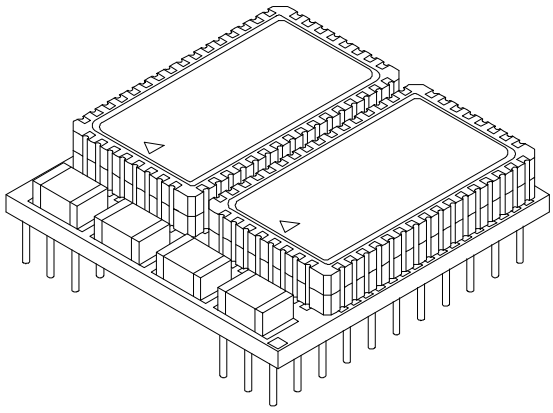
DPZ256X32IV3

DESCRIPTION:

The DPZ256X32IV3 ''VERSA-STACK'' module is a revolutionary new memory subsystem using Dense-Pac Microsystems' ceramic Stackable Leadless Chip Carriers (SLCC) mounted on a co-fired ceramic substrate. It offers 8 Megabits of FLASH EEPROM in a single package envelope of 1.090" x 1.090" x .252".

The DPZ256X32IV3 is built with four SLCC packages each containing two 128K x 8 FLASH memory devices. Each SLCC is hermetically sealed making the module suitable for commercial, industrial and military applications.

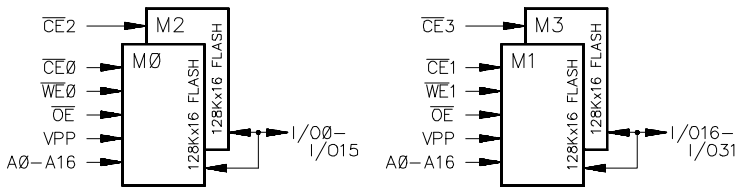
By using SLCCs, the ''Versa-Stack'' family of modules offers a higher board density of memory than available with conventional through-hole, surface mount, module or hybrid techniques.



FEATURES:

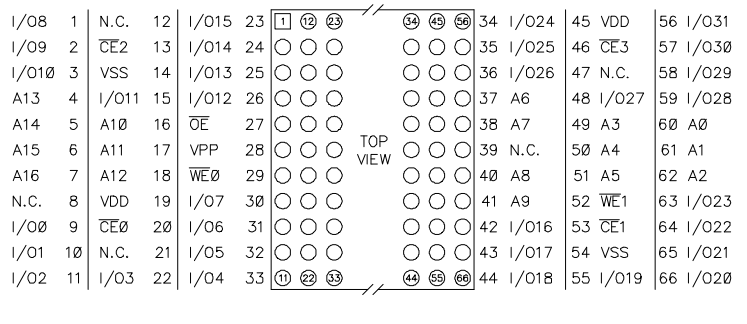
- Organization:
  256K x 32, 512K x 16
- Fast Access Times (max.):
  120, 150, 170, 200, 250ns
- Fully Static Operation
  - No clock or refresh required
- TTL Compatible Inputs and Outputs
- Common Data Inputs and Outputs
- 10,000 Erase/Program Cycles (min.)
- 66 - Pin PGA ''VERSA-STACK'' Package

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES	
A0 - A16	Address Inputs
I/O0 - I/O31	Data Input/Output
$\overline{CE}$0 - $\overline{CE}$3	Chip Enables
$\overline{WE}$0, $\overline{WE}$1	Write Enables
$\overline{OE}$	Output Enable
V_{PP}	Programming Voltage (+12.0V)
V_{DD}	Power (+5V)
V_{SS}	Ground
N.C.	No Connect

PIN-OUT DIAGRAM



DEVICE OPERATION:

The FLASH devices are electrically erasable and programmable memories that function similarly to an EPROM device, but can be erased without being removed from the system and exposed to ultraviolet light. Each 128K x 8 device can be erased individually eliminating the need to re-program the entire module when partial code changes are required.

READ:

With V_{PP} = 0V to V_{DD} (V_{PPLO}), the devices are read-only memories and can be read like a standard EPROM. By selecting the device to be read (see Truth Table and Functional Block Diagram), the data programmed into the device will appear on the appropriate I/O pins.

When V_{PP} = +12.0V ± 0.6V (V_{PPHI}), reads can be accomplished in the same manner as described above but must be preceded by writing $00H^1$ to the command register prior to reading the device. When V_{PP} is raised to V_{PPHI} the contents of the command register default to $00H^1$ and remain that way until the command register is altered.

STANDBY:

When the appropriate $\overline{CE}$'s are raised to a logic-high level, the standby operation disables the FLASH devices reducing the power consumption substantially. The outputs are placed in a high- impedance state, independent of the $\overline{OE}$ input. If the module is deselected during programming or erase, the device upon which the operation was being performed will continue to draw active current until the operation is completed.

PROGRAM:

The programming and erasing functions are accessed via the command register when high voltage is applied to V_{PP}. The contents of the command register control the functions of the memory device (see Command Definition Table).

The command register is not an addressable memory location. The register stores the address, data, and command information required to execute the command. When V_{PP} = V_{PPLO} the command register is reset to $00H^1$ returning the device to the read-only mode.

The command register is written by enabling the device upon which that the operation is to be performed (see Functional Block Diagram). While the device is enabled bring $\overline{WE}$ to a logic-low (V_{IL}). The address is latched on the falling edge of $\overline{WE}$ and data is latched on the rising edge of $\overline{WE}$. Programming is initiated by writing $40H^1$ (program setup command) to the command register. On the next falling edge of $\overline{WE}$ the address to be programmed will be latched, followed by the data being latched on the rising edge of $\overline{WE}$ (see AC Operating and Characteristics Table).

PROGRAM VERIFY:

The FLASH devices are programmed one location at a time. Each location may be programmed sequentially or at random. Following each programming operation, the data written must be verified.

To initiate the program-verify mode, $C0H^1$ must be written to the command register of the device just programmed. The programming operation is terminated on the rising edge of $\overline{WE}$. The program-verify command is then written to the command register.

After the program-verify command is written to the command register, the memory device applies an internally generated margin voltage to the location just written. After waiting 6µs the data written can be verified by doing a read. If true data is read from the device, the location write was successful and the next location may be programmed.

If the device fails to verify, the program/verify operation is repeated up to 25 times.

ERASE:

The erase function is a command-only operation and can only be executed while V_{PP} = V_{PPHI}.

To setup the chip-erase, $20H^1$ must be written to the command register. The chip-erase is then executed by once again writing $20H^1$ to the command register (see AC Operating and Characteristics Table).

To ensure a reliable erasure, all bits in the device to be erased should be programmed to their charged state (data = 00H) prior to starting the erase operation. With the algorithm provided, this operation should typically take 2 seconds.

HIGH PERFORMANCE PARALLEL ERASURE:

Dense-Pac recommends that all users implement the following Intel High Performance Parallel Erase algorithm in order to avoid the possibility of over erasing these parts.

In applications containing more than one FLASH memory, you can erase each device serially or you can reduce total erase time by implementing a parallel erase algorithm. You may save time by erasing all devices at the same time. However, since FLASH memories may erase at different rates, you must verify each device separately. This can be done in a word-wise fashion with the Command Register Reset Command and a special masking algorithm.

Take for example the case of two-device (parallel) erasure. The CPU first writes the data word erase command 2020H twice in succession. This starts erasure. After 10ms, the CPU writes the data word verify command A0A0H to stop erasure and setup erase verification. If both one or both bytes are not erased at the given address, the CPU implements the erase sequence again without incrementing the address.

Suppose at the given address only the low byte verifies FFH data? Could the whole chip be erased? The answer is yes. Rather than check the rest of the low byte addresses independently of the high byte, simply use the reset command to mask the low byte from erasure and erase verification on the next erase loop. In this example the erase command would be 20FFH and the verify command would be A0FFH. Once the high byte verifies at the address, the CPU modifies the command back to the default 2020H and A0A0H, increments to the next address, and then writes the verify command.

See Figure 4 for a conceptual view of the parallel erase flow chart and Figure 4 for the detailed version. These flow charts are for the 16-bit systems and can be expanded for 32-bit designs.

ERASE VERIFY:

The erase operation erases all locations in the device selected in parallel. Upon completion of the erase operation, each location must be verified. This operation is initiated by writing $A0H^1$ to the command register. The address to be verified must be supplied in order to be latched on the falling edge of $\overline{WE}$.

The memory device internally generates a margin voltage and applies it to the addressed location. If FFH is read from the device, it indicates the location is erased. The erase/verify command is issued prior to each location verification to latch the address of the location to be verified. This continues until FFH is not read from the device or the last address for the device being erased is read.

If FFH is not read from the location being verified, an additional erase operation is performed. Verification then resumes from the last location verified. Once all locations in the device being erased are verified, the erase operation is complete. The verify operation should now be terminated by writing a valid command such as program set-up to the command register.

PRODUCT I.D. OPERATION:

The product I.D. operation outputs the manufacturer code (89H) and the device code (B4H). This allows programming equipment to match the device with the proper erase and programming algorithms.

With $\overline{CE}$ and $\overline{OE}$ at a logic low level, raising A9 to V_{ID} (see DC Operating Characteristics) will initiate the operation. The manufacturer's code can then be read from address location 0000H and the device code can be read from address location 0001H.

The I.D. codes can also be accessed via the command register. Following a write of 90H to the command register, a read from address location 0000H outputs the manufacturer's code (89H). A read from address location 0001H outputs the device code (B4H). To terminate the operation, it is necessary to write another valid command into the register.

POWER UP/DOWN PROTECTION:

The FLASH devices are designed to protect against accidental erasure or programming during power transitions. It makes no difference as to which power supply, V_{PP} or V_{DD}, powers up first. Power supply sequencing is not required. Internal circuitry ensures that the command register is reset to the read mode upon power up.

POWER SUPPLY DECOUPLING:

V_{PP} traces should use trace widths and layout considerations comparable to that of the V_{DD} power bus. The V_{PP} supply traces should also be decoupled to help decrease voltage spikes.

While the memory module has high-frequency, low-inductance decoupling capacitors mounted on the substrate connected to V_{DD} and V_{SS}, it is recommended that a 4.7µF to 10µF electrolytic capacitor be placed near the memory module connected across V_{DD} and V_{SS} for bulk

COMMAND DEFINITION TABLE

Command	Bus Cycles Req'd	First Bus Cycle			Second Bus Cycle		
		Operation	Address	Data [1]	Operation	Address	Data [1]
Read Memory	1	Write	X	00H	-	-	-
Setup Erase / Erase	2	Write	X	20H	Write	X	20H
Erase Verify	2	Write	EA	A0H	Read	X	EVD
Setup Program / Program	2	Write	X	40H	Write	PA	PD
Program Verify	2	Write	X	C0H	Read	X	PVD
Reset	2	Write	X	FFH	Write	X	FFH
Read Product I.D. Codes	3	Write	X	90H	Read	IA	ID

EA = Address to Verify
EVD = Data Read from Location EA
IA = Address: 0000H for manufacturing code, 0001H for device code
ID = ID data read from IA during product ID operation
(Manufacturer = 89H, Device = B4H)

PA = Address to Program
PD = Data to be Programmed at Location PA
PVA = Data to be Read from Location PA at Program Verify

TRUTH TABLE

Mode	Description	$\overline{CE}$n	$\overline{WE}$n	$\overline{OE}$	A0	A9	V_{PP}	I/O Pins	Supply Current
READ ONLY	Not Selected	H	X	X	X	X	V_{PPLO}	HIGH-Z	Standby
	Output Disable	L	H	H	X	X	V_{PPLO}	HIGH-Z	Active
	Read	L	H	L	A0	A9	V_{PPLO}	D_{OUT}	Active
	I.D. (Mfr.)	L	H	L	L	V_{ID}	V_{PPLO}	D_{OUT} =89H	Active
	I.D. (Device)	L	H	L	H	V_{ID}	V_{PPLO}	D_{OUT} = B4H	Active
COMMAND PROGRAM	Not Selected	H	X	X	X	X	V_{PPHI}	HIGH-Z	Standby
	Output Disable	L	H	H	X	X	V_{PPHI}	HIGH-Z	Active
	Read	L	H	L	A0	A9	V_{PPHI}	D_{OUT}	Active
	Write	L	L	H	A0	A9	V_{PPHI}	D_{IN}	Active

L = LOW, H = HIGH, X = Don't Care

RECOMMENDED OPERATING RANGE [2]						
Symbol	Characteristic		Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.5	5.0	5.5	V
V_{PP}	Programming Voltage		11.4	12.0	12.6	V
V_{IL}	Input LOW Voltage		-0.5[3]		0.8	V
V_{IH}	Input HIGH Voltage		2.0		V_{DD}+0.5	V
T_A	Operating Temperature	C	0	+25	+70	°C
		I	-40	+25	+85	
		M/B	-55	+25	+125	
V_{ID}	A9 I.D. Input/Output		11.5		13.0	V

ABSOLUTE MAXIMUM RATINGS [7]			
Symbol	Parameter	Value	Unit
T_{STC}	Storage Temperature	-65 to +150	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
V_{ID}	Voltage on A9 [2]	-0.5 to +14.0 [4, 5]	V
I_{OUT}	Output Short Circuit Current	100 [6]	mA
$V_{I/O}$	Input/Output Voltage [2]	-0.5 to +7.0 [3]	V
V_{PP}	V_{PP} Supply Voltage [2] During Erase/Program	-0.5 to +14.0 [4]	V
V_{DD}	Supply Voltage [2]	-0.6 to +7.0 [4]	V

CAPACITANCE [7]: T_A = 25°C, F = 1.0MHz				
Symbol	Parameter	Max.	Unit	Condition
C_{ADR}	Address Input	40	pF	V_{IN}[3] = 0V
C_{CE}	Chip Enable	15		
C_{WE}	Write Enable	25		
C_{OE}	Output Enable	40		
$C_{I/O}$	Data Input/Output	30		

DC OUTPUT CHARACTERISTICS					
Symbol	Parameter	Condition	Min.	Max.	Unit
V_{OH}	HIGH Voltage	I_{OH}= -2.5mA	2.4		V
V_{OL}	LOW Voltage	I_{OL}=5.8mA		0.45	V

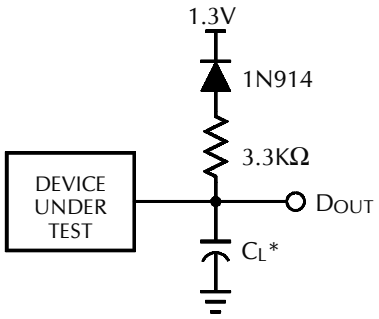
DC OPERATING CHARACTERISTICS: Over operating ranges					
Symbol	Characteristics	Test Conditions	Limits		Unit
			Min.	Max.	
I_{IN}	Input Leakage Current	V_{IN} = 0V to V_{DD}	-8	+8	µA
I_{OUT}	Output Leakage Current	$V_{I/O}$ = 0V to V_{DD}, $\overline{CE}$ or $\overline{OE}$ = V_{IH}, or $\overline{WE}$ = V_{IL}	-20	+20	µA
I_{CC1}	Operating Supply Current	$\overline{CE}$ = V_{IL}, V_{IN} = V_{IL} or V_{IH}, I_{OUT} = 0mA, f = 8MHz		130	mA
I_{CC2}	V_{DD} Programming Current	Programming in Progress		130	mA
I_{CC3}	V_{DD} Erase Current	Erasure in Progress		130	mA
I_{SB1}	Standby Current (TTL)	$\overline{CE}$ = V_{IH}		8	mA
I_{SB2}	Full Standby Supply Current (CMOS)	$\overline{CE}$ = V_{DD} -0.2V		0.8	mA
I_{PPS}	V_{PP} Leakage Current	V_{PP} = V_{PPLO}		80	µA
I_{PP1}	V_{PP} Read Current	V_{PP} = V_{PPHI}		1.6	mA
I_{PP2}	V_{PP} Programming Current	V_{PP} = V_{PPHI}, Programming in Progress		125	mA
I_{PP3}	V_{PP} Erase Current	V_{PP} = V_{PPHI}, Erasure in Progress		125	mA
I_{ID}	A9 I.D. Current	A9 = V_{ID}, $\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}		2.0	mA

AC TEST CONDITIONS	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
Output Timing Reference Levels During Verify	0.8V and +2.4V

OUTPUT LOAD		
Load	**C_L**	**Parameters Measured**
1	100 pF	except t_{DF}, t_{LZ} and t_{OLZ}
2	30pF	t_{DF}, t_{LZ} and t_{OLZ}

Figure 1. Output Load

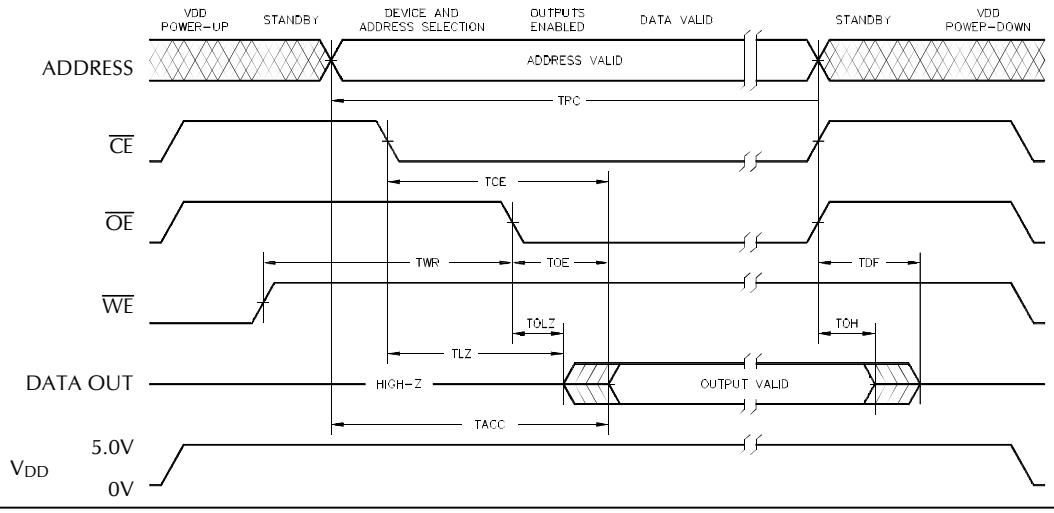
* Including Probe and Jig Capacitance.



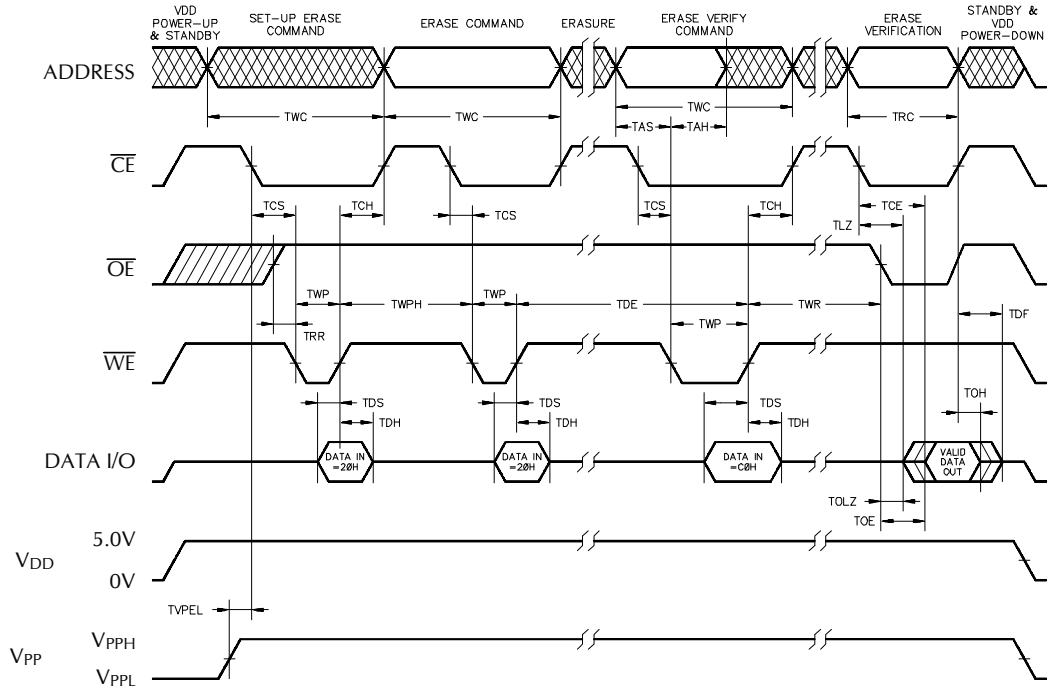
AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges												
No.	**Symbol**	**Parameter**	**120ns**		**150ns**		**170ns**		**200ns**		**250ns**		**Unit**
			Min.	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	
1	t_{RC}	Read Cycle Time	120		150		170		200		250		ns
2	t_{CE}	Chip Enable Access Time		120		150		170		200		250	ns
3	t_{ACC}	Address Access Time		120		150		170		200		250	ns
4	t_{OE}	Output Enable Access Time		50		55		60		60		65	ns
5	t_{LZ}	Chip Enable to Output in LOW-Z [7, 8]	0		0		0		0		0		ns
6	t_{OLZ}	Output Enable to Output in LOW-Z [7, 8]	0		0		0		0		0		ns
7	t_{DF}	Output Disable to Output in HIGH-Z [7, 8]		30		35		40		45		60	ns
8	t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$ Change (whichever occurs first)	0		0		0		0		0		ns

AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE: Over operating ranges												
No.	**Symbol**	**Parameter**	**120ns**		**150ns**		**170ns**		**200ns**		**250ns**		**Unit**
			Min.	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	
9	t_{WC}	Write Cycle Time	120		150		170		200		250		ns
10	t_{AS}	Address Setup Time	0		0		0		0		0		ns
11	t_{AH}	Address Hold Time	60		60		60		60		60		ns
12	t_{DS}	Data Setup Time	50		50		50		50		50		ns
13	t_{DH}	Data Hold Time	10		10		10		10		10		ns
14	t_{WR}	Write Recovery Time before Read	6		6		6		6		6		µs
15	t_{RR}	Read Recover Time before Write	0		0		0		0		0		ns
16	t_{CS}	Chip Enable Setup Time before Write	20		20		20		20		20		ns
17	t_{CH}	Chip Enable Hold Time	0		0		0		0		0		ns
18	t_{WP}	Write Pulse Width [9]	80		80		80		80		80		ns
19	t_{WPH}	Write Pulse Width HIGH [9]	20		20		20		20		20		ns
20	t_{DP}	Duration of Programming Operation	10		10		10		10		10		µs
21	t_{DE}	Duration of Erase Operation	9.5	10.5	9.5	10.5	9.5	10.5	9.5	10.5	9.5	10.5	ms
22	t_{VPEL}	V_{PP} Setup Time to Chip Enable LOW [4]	1.0		1.0		1.0		1.0		1.0		µs

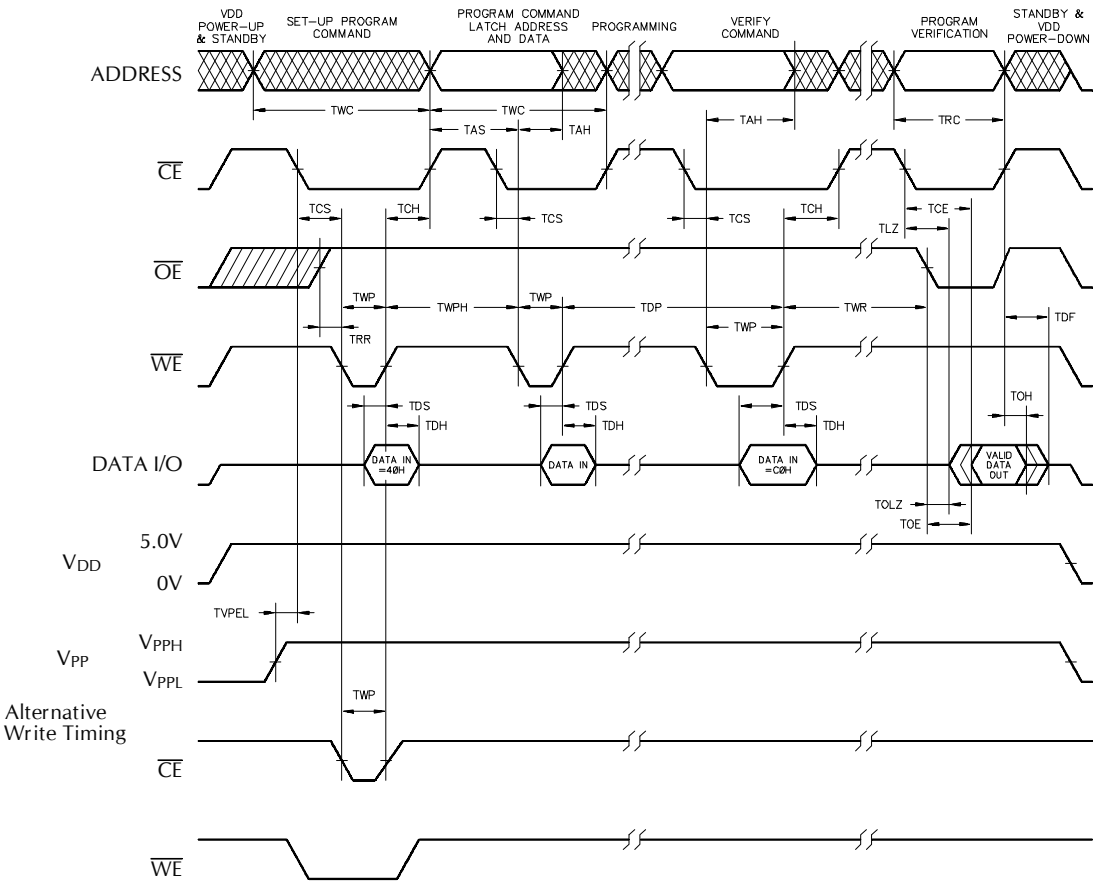
READ CYCLE



ERASE CYCLE



PROGRAMMING CYCLE [9]



NOTES:

1. Each SLCC contains two FLASH memory devices enabled by a common chip enable. Typically this module would be used as a x32 device with $\overline{CE}0$ and $\overline{CE}1$ tied together. When writing commands to the Command Register under these conditions, the command shown in the Command Definition Table should be duplicated to each byte (I/O0 - I/O7, I/O8 - I/O15, I/O16 - I/O23, I/O24 - I/O31) of the module. If the command to be written is 404040H like that for Setup Program/Program, 4040H would be written to the module followed by the 32 bit data. A single device can be programmed or erased by writing the appropriate command to the device the operation is to be performed on while 00H is written to the other devices that are enabled at the same time.
   Care must be taken when doing Program Verify on a single device. Make certain that no other devices are driving the data bus of the devices that are not being verified but are enabled along with the device that is being verified. Any device that is enabled during Program Verify will be driving the data bus with the data that is programmed at that address.
2. All voltages are with respect to V_{SS}.
3. -2.0V min. for pulse width less than 20ns (V_{IL} min. = -0.5V at DC level).
4. Maximum DC voltage on V_{PP} or A9 may over shoot to +14.0V for periods less than 20ns.
5. Output shorted for no more than 1 second. No more than one output shorted at a time.
6. Stresses greater than those under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
7. This parameter is guaranteed and not 100% tested.
8. Transition is measured at the point of ±500mV from steady state voltage.
9. Chip Enable Controlled Writes: Write operations are driven by the valid combination of Chip Enable and Write Enable. In systems where Chip Enable defines the write pulse width (within a longer Write Enable timing waveform) all Set-up, Hold, and inactive Write Enable times should be measured relative to the Chip Enable waveform.

FIGURE 2: WRITE ALGORITHM

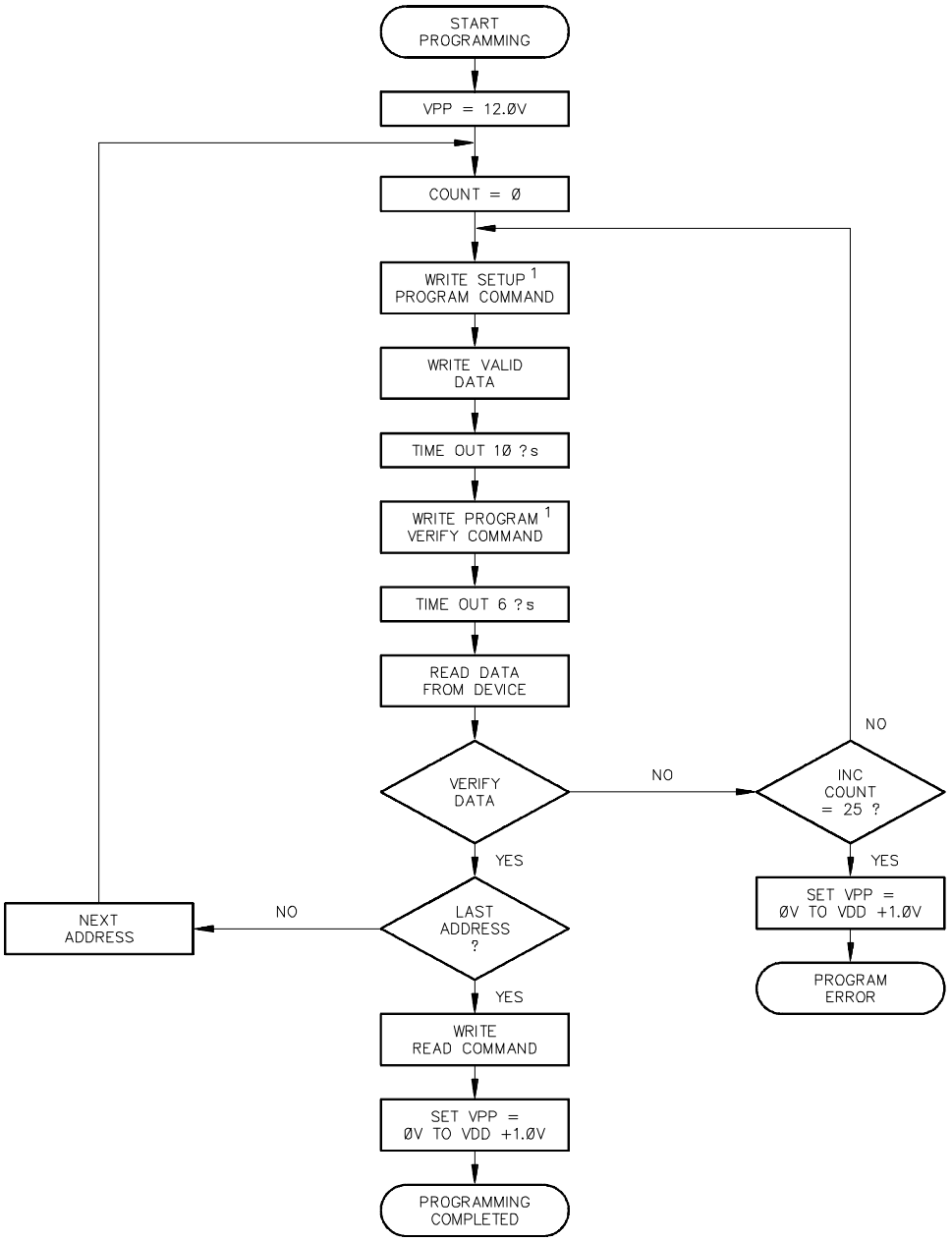


FIGURE 3: ERASE ALGORITHM

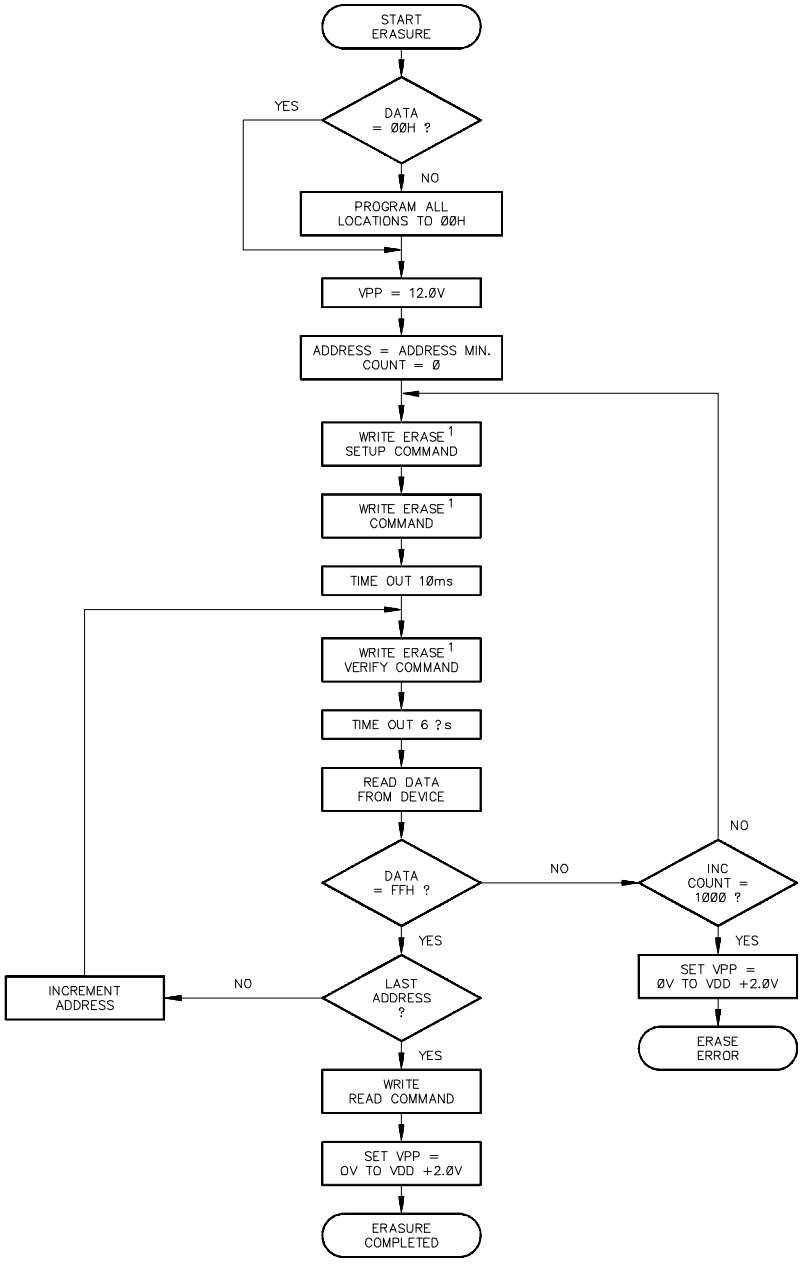


FIGURE 4: HIGH PERFORMANCE PARALLEL ERASURE (Conceptual Device)

NOTE:

[1] You mask the device by substituting a reset command for the erase and verify commands, that way the erased byte idles through the next erase loop.

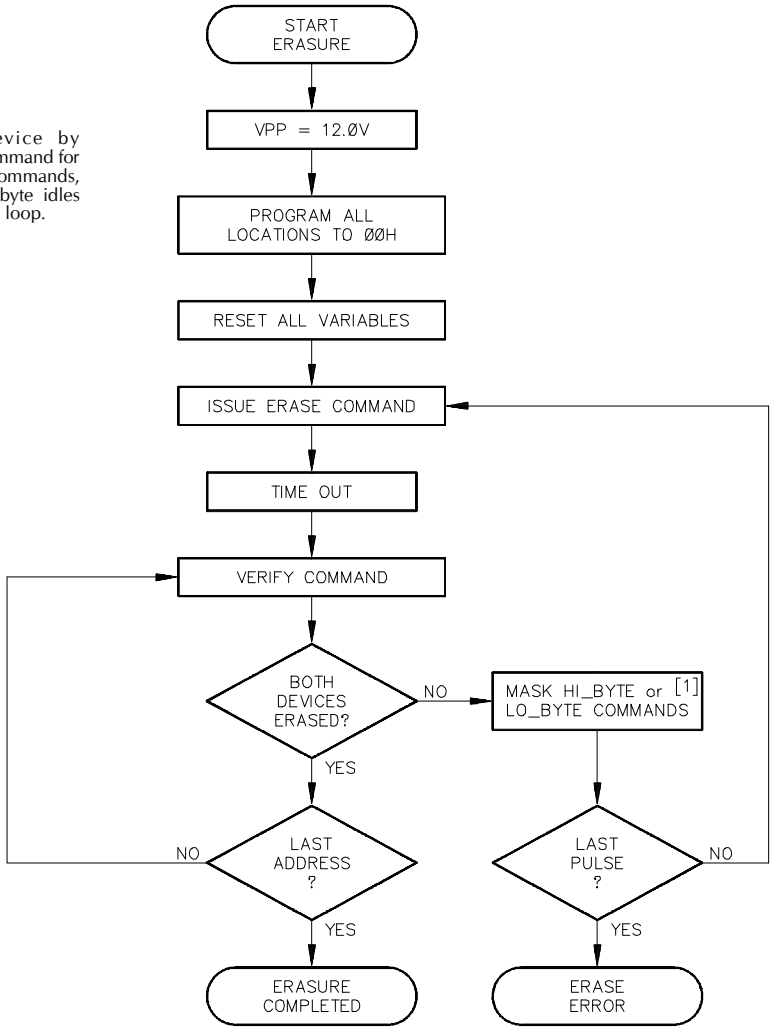


FIGURE 5: PARALLEL ERASE FLOW CHART

NOTES:

[1] Wait for VPP to stabilize.

[2] Use Quick-Pulse Programming algorithm.

[3] Initialize Variables:
PLSCNT_HI = High Byte Pulse Counter
PLSCNT_LO = Low Byte Pulse Counter
FLAG = Erase Error Flag
ADRS = Address
E_COM = Erase Command
V_COM = Verify Command

[4] Erase Verify Command stops erasure.

[5] See Figure 6 for subroutine.

[6] When both devices at ADRS are erased, F_DATA = FFFFH.

[7] Reset commands to default E_COM = 2020H, V_COM = A0A0H before verifying next ADRS.

[8] Reset device for read operation.

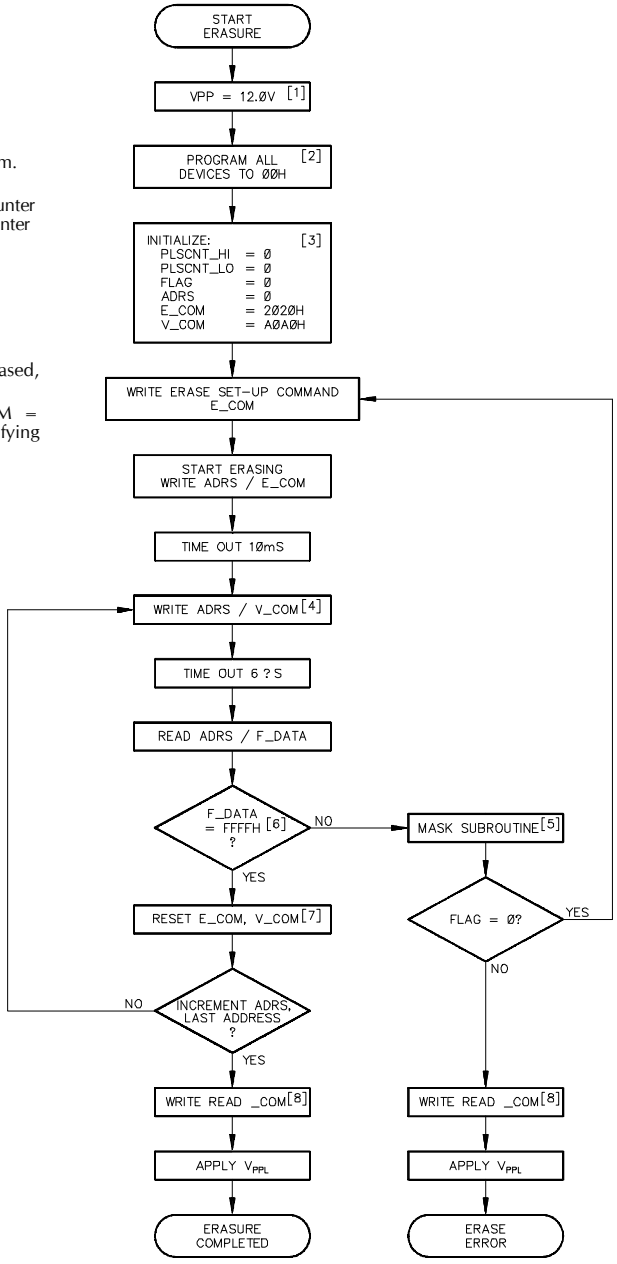


FIGURE 6: DEVICE ERASE VERIFY AND MASK SUBROUTINE

NOTES:

[1] This subroutine masks the High byte or Low Byte of the Erase and Verify commands from executing during the next operation.

[2] Mask the High byte with 00H.

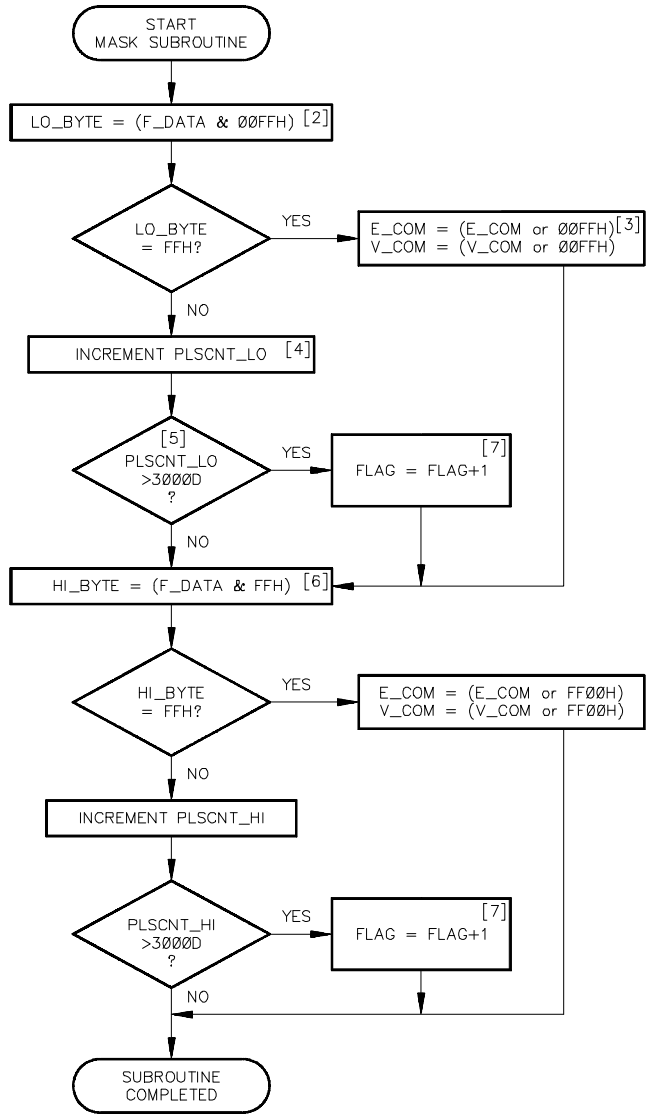
[3] If the Low byte verifies erasure, then mask the next erase and verify commands with FFH (reset).

[4] If the Low byte does not verify, increment its pulse counter.

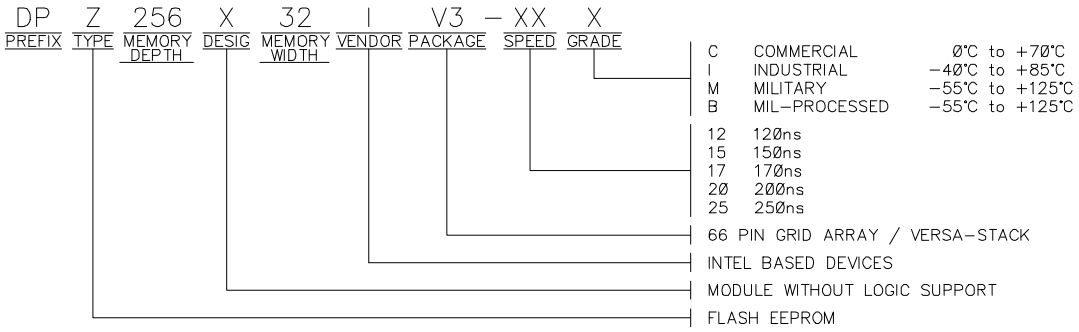
[5] Check for max. count. FLAG = 1 denotes a Low byte error.

[6] Repeat sequence for High byte.

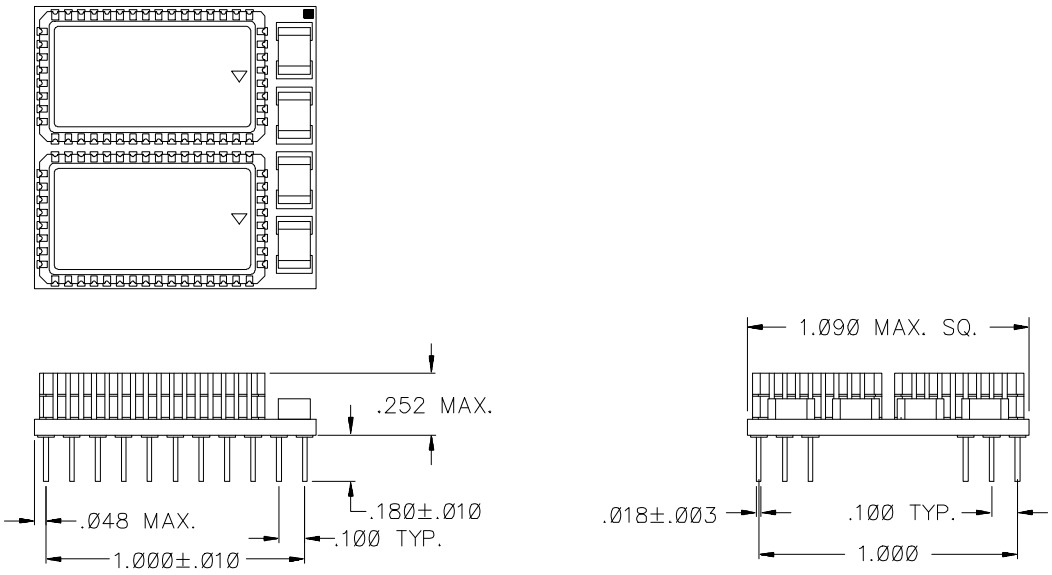
[7] FLAG = 2 denotes a High byte error. FLAG = 3 denotes both High byte and Low byte errors.



ORDERING INFORMATION



MECHANICAL DRAWING



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