AsahiKASEI
ASAHI KASEI EMD

AK2347A

Two-way Radio Audio & Sub-Audio Processor

Features

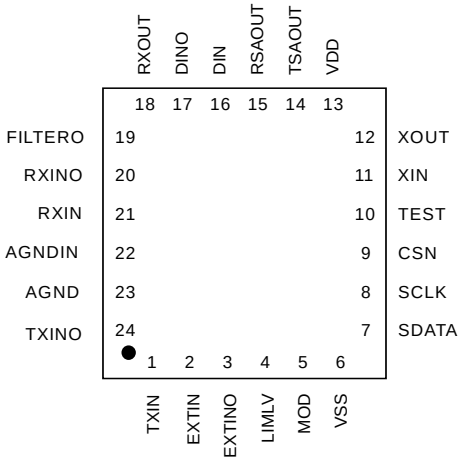
- Audio processing
  - TX and RX amplifier
  - Pre/De-emphasis circuit
  - Compressor and Expander with no external components
  - Scrambler and De-scrambler in frequency inversion type (3.388kHz or 3.290kHz)
  - Limiter with level adjuster
  - Splatter filter for wide and narrow band
  - Digital controlled amplifier for microphone, modulator and demodulator sensitivity

- Sub-Audio filter with level adjuster for CTCSS and DCS
- Low power supply operation: 2.7 to 3,3V
- Wide range operating for temperature: -40 to 85 °C
- Oscillator circuit for 3.6864MHz and 3.579545MHz crystal
- Serial control interface operation
- Compact plastic packaging, 24-pin QFNJ (4.0x4.0x0.75mm 0.5mm pitch)

Description

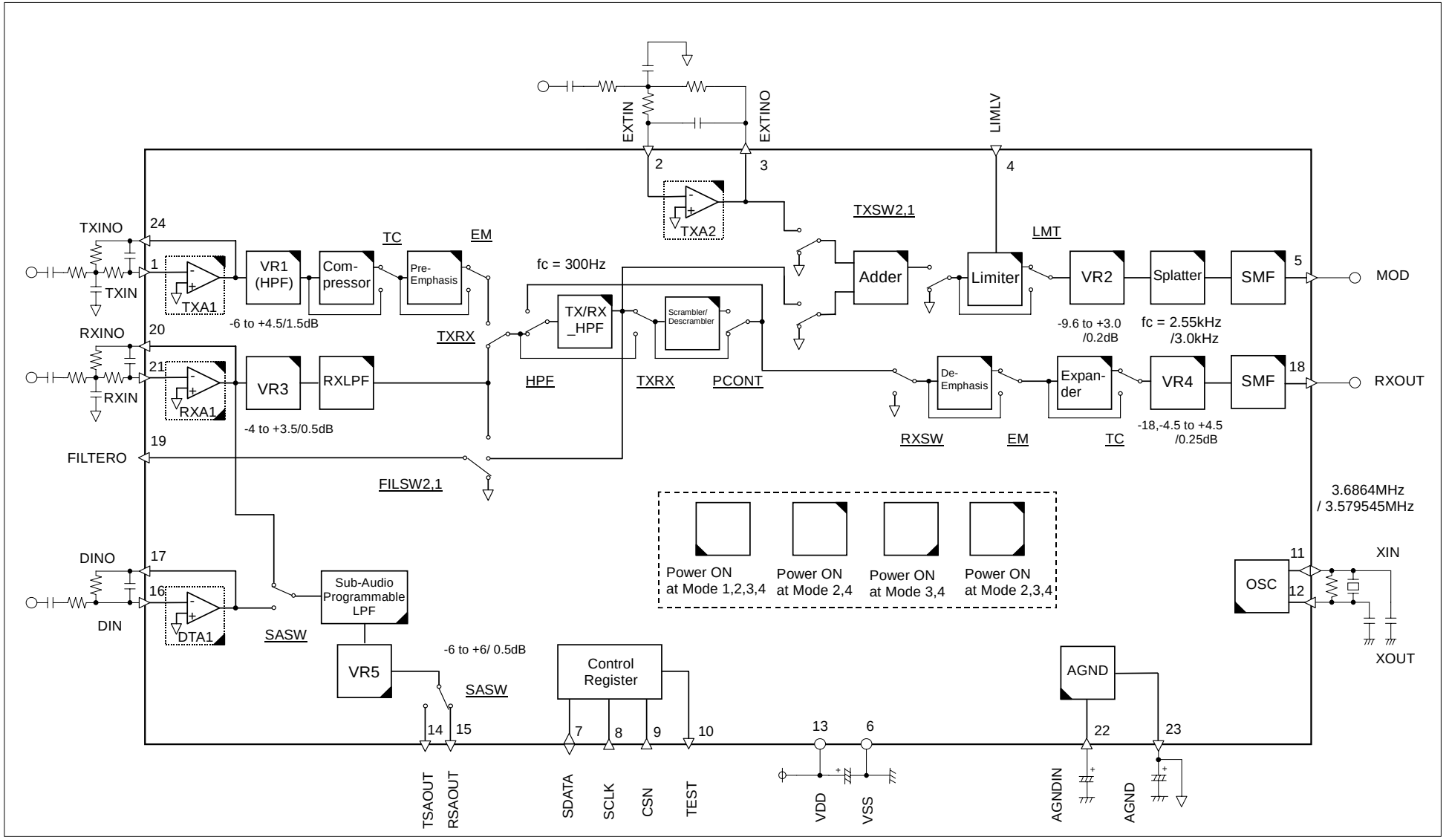
AK2347A includes audio filter, limiter, splatter filter, compandor, scrambler, which is highly integrated two-way radio baseband functions for FRS and LMR.
Audio high-pass filter shows a high attenuation in magnitude response characteristics under 250Hz that supports to eliminate a subaudio tone clearly.
TX limiter for deviation control has a limiting level adjuster by applying a DC voltage via external components. Splatter filter has the magnitude response for narrowband(fc=2.55kHz) and wideband(3.0kHz) to meet various regulatory agencies in the world wide.
Compandor is no adjustment type because it includes all parametric components inside the chip.
Scrambler circuit is composed of frequency inversion circuit by double balanced mixer that has 3.388kHz and 3.290kHz carrier clock.
Sub-Audio filter with level adjuster is available for pre- or post-filter for CTCSS and DCS.
There are four signal level adjusters for microphone, modulator and demodulator sensitivity by digital controlled amplifier (volume).

- Pin Assignment (Top view)



Contents

Block Diagram



Block Functions

Block	Function
TXA1	Operational amplifier for gain adjustment of transmit audio signal and for the filter for preventing aliasing noise of the SCF circuit in the subsequent stage. Use external resistors and capacitors to set the gain to 30dB or less and the cut-off frequency to around 10kHz.
VR1 (HPF)	This circuit controls the volume for adjusting the input level of transmit audio signal. Setting registers: VR12 to VR10, adjustment range: -6.0dB to +4.5dB in 1.5dB steps
Compressor	This circuit compresses the amplitude of transmit audio signal by 1/2 in dB scale. Cross-point: -10dBx. This circuit is turned on and off by the TC register.
Pre-emphasis	This circuit emphasizes the high-frequency component of transmit audio signal to improve the S/N ratio of the modulation signal.
TX/RX_HPF	High-pass filter to eliminate low-frequency components lower than 250Hz which are included in transmit and receive audio signals. This circuit is turned on and off by the HPF register.
Scrambler/ Descrambler	This circuit inverts the spectrum distribution of transmit and receive audio signals with respect to the carrier frequency. The carrier frequency is 3.388kHz or 3.290kHz. The Scrambler/Descrambler or emphasis circuit can be selected using the EM and PCONT registers. These circuits cannot be used at the same time.
TXA2	Operational amplifier for gain adjustment of external tone signal. Use external resistors and capacitors to set the gain to 0dB or less and the cut-off frequency to around 10kHz.
Adder	This circuit adds together the audio signal and external tone input signal. This circuit is controlled by the TXSW2 and TXSW1 register.
Limiter	Amplitude limiting circuit to suppress frequency deviation in the modulation signal. The limit level can be adjusted by applying a DC voltage to the LIMLV pin. When the pin is left open, the level predetermined within the device is output. This circuit is turned on and off by the LMT register.
VR2	This circuit controls the volume for adjusting the output level on the MOD pin. Setting registers: VR25 to VR20, adjustment range: -3.2dB to +3.0dB in 0.2dB steps. For coarse adjustment, switching between -6.4dB and 0dB is possible.
Splatter	Low-pass filter to eliminate high-frequency components higher than 3kHz which are included in the limiter output signal. The cut-off frequency can be adjusted with the SPL register.
SMF	Smoothing filter to eliminate the high-frequency and clock components generated in the SCF circuit.
RXA1	Operational amplifier for gain adjustment of the receive demodulation signal and for the filter for preventing aliasing noise in the SCF circuit in the subsequent stage. Use external resistors and capacitors to set the gain to 20dB or less and the cut-off frequency to around 40kHz.
VR3	This circuit controls the volume for adjusting the input level of the receive demodulation signal. Setting registers: VR33 to VR30, adjustment range: -4.0dB to +3.5dB in 0.5dB steps
RXLPF	Low-pass filter to eliminate high-frequency components higher than 3kHz which are included in the receive demodulation signal.
De-emphasis	This circuit restores the original state of the signal of which high-frequency component has been emphasized by the Pre-emphasis.
Expander	This circuit expands the signal compressed twice by the Compressor in dB scale to restore the original signal state. Cross-point: -10dBx. The Expander is turned on and off with the TC register.
VR4	This circuit controls the volume for adjusting the RX output level. Setting registers: VR45 to VR40 Adjustment range: -18.0dB, -4.5dB to +4.5dB in 0.25dB steps

Block	Function
DTA1	Operational amplifier for gain adjustment of the Sub-Audio LPF input signal and for the filter for preventing aliasing noise in the SCF circuit in the subsequent stage. Use external resistors and capacitors to set the gain to 0dB or less and the cut-off frequency to around 10kHz.
Sub-Audio Programmable LPF	Low-pass filter to eliminate components of the DAT1 signal in the transmit operation and of RXA1 signal in the receive. This circuit is controlled by the SASW register for transmit or receive and by the SA5 to SA0 for cut-off frequency.
VR5	This circuit controls the volume for adjusting the output level from the Sub-Audio LPF signal. Setting registers: VR54 to VR50, adjustment range: -6.0dB to +6.0dB in 0.5dB steps
AGND	This circuit generates the reference voltage (1/2VDD) for internal analog signals.
OSC	This circuit generates a 3.6864MHz or 3.579545MHz reference clock signal from an external resistor and crystal oscillator. This circuit is controlled by the MCKSL register.
Control Register	Control registers set the switch status and volume for level adjustment inside the IC according to the serial input data consisting of 1-bit instruction and 4-bit address and 8-bit data. At power-up, the registers are set to the power-down values by the power-on reset circuit. This circuit has a software reset named RSTN register. (See the description of the registers)

Pin Functions

Pin number	Pin name	Pin type	Power-down status	Function
1	TXIN	AI	Z	Transmit audio signal input pin This pin is the inverting input pin of TXA1. This pin, with resistors and capacitors externally connected, forms a microphone amplifier.
2	EXTIN	AI	Z	External input pin This pin is the inverting input pin of TXA2. This pin, with resistors and capacitors externally connected, forms a amplifier. An external signal such as a tone signal other than the audio signal can be input.
3	EXTINO	AO	*3)	Output pin of TXA2 *1)
4	LIMLV	AI	*4)	Limit level adjustment pin The limit level can be adjusted by applying a DC voltage to this pin. When this pin is left open, the limit level predetermined within the device is set.
5	MOD	AO	Z	Modulated transmit signal output pin *2)
6	VSS	PWR	-	Negative power supply pin Normally, apply 0V.
7	SDATA	DB	Z	Serial data input and output control pin
8	SCLK	DI	Z	Serial data clock input pin
9	CSN	DI	Z	Serial data chip select input This signal is active low.
10	TEST	DO	L	Output pin for testing This pin is assigned to test pin for pre-delivery inspection in factory. Do not connect anything in normal operation.

Pin number	Pin name	Pin type	Power-down status	Function
11	XIN	DB	*5)	Pin for connecting a crystal oscillator A reference clock used within this IC is generated by connecting a 3.6864MHz or 3.579545MHz oscillator between this pin and the adjacent XOUT pin. For detailed information about the connection method and the method for supplying an external clock, see "Recommended External Application Circuits".
12	XOUT	DI	*5)	Pin for connecting a crystal oscillator
13	VDD	PWR	–	Positive power supply pin Connect this pin to a power supply ranging from 2.7V to 3.3V with less noise. Connect a bypass capacitor of 0.1μF or higher between this pin and the VSS pin.
14	TSAOUT	AO	Z	Transmit Sub-Audio signal output pin *2)
15	RSAOUT	AO	Z	Receive Sub-Audio signal output pin *2)
16	DIN	AI	Z	Data input pin This pin is the inverting input pin of DTA1. This pin, with resistors and capacitors externally connected, forms a amplifier. An external signal such as a tone signal through CPU port can be input.
17	DINO	AO	Z	Output pin of DTA1 *1)
18	RXOUT	AO	Z	Receive audio signal output pin *2)
19	FILTERO	AO	Z	RXLPF or TX/RX_HPF block output pin This pin can be used as a monitor pin for a signal such as a tone signal. The output signal on this pin includes a 57.6kHz sampling-clock component. So, perform waveform processing externally as required. *2)
20	RXINO	AO	Z	Output pin of RXA1 *1)
21	RXIN	AI	Z	Demodulated receive signal input pin Inverting input pin of RXA1. This pin, with resistors and capacitors externally connected, forms a pre-filter.
22	AGNDIN	AI	*3)	Analog ground input pin This pin is connected to a capacitor to stabilize the analog ground level.
23	AGND	AO	*3)	Analog ground output pin This pin is connected to a capacitor to stabilize the analog ground level.
24	TXINO	AO	Z	Output pin of TXA1 *1)

Note) A: Analog, D: Digital, PWR: Power, I: Input, O: Output, B: Bi-directional, Z: High-Z, L: Low

*1) Output load requirement: [load impedance] > 30kΩ, [load capacitance] < 50pF
*2) Output load requirement: [load impedance] > 10kΩ, [load capacitance] < 50pF

*3) AGND (=1/2VDD) level
*4) AGND + 0.256(VDD-AGND) level

*5) When XOUT pin is set to low level, XIN pin goes to High-Z.
When XOUT pin is set to high level, XIN pin outputs low level.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Power Supply Voltage	VDD	-0.3	4.6	V
Ground Level	VSS	0	0	V
Input Voltage	V_{IN}	-0.3	VDD+0.3	V
Input Current (Except power supply pin)	I_{IN}	-10	+10	mA
Storage Temperature	T_{stg}	-55	130	°C

Note) All voltages are relative to the VSS pin.

Caution) If the device is used in conditions exceeding these values, the device may be destroyed. Normal operations are not guaranteed in such extreme conditions.

Recommended Operating Conditions

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
Operating Temperature	Ta		−40		85	°C
Power Supply Voltage	VDD		2.7	3.0	3.3	V
Analog Reference Voltage	AGND			1/2VDD		V

Note) All voltages are relative to the VSS pin.

Digital DC Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
High level input voltage	V_{IH1}	SDATA	0.7VDD			V
	V_{IH2}	SCLK, CSN	0.8VDD			
Low level input voltage	V_{IL1}	SDATA			0.3VDD	V
	V_{IL2}	SCLK, CSN			0.2VDD	
High level input current	I_{IH}	V_{IH}=VDD SDATA, SCLK, CSN			10	μA
Low level input current	I_{IL}	V_{IL}=0V SDATA, SCLK, CSN	-10			μA
High level output voltage	V_{OH}	I_{OH}=+0.2mA SDATA	VDD−0.4		VDD	V
Low level output voltage	V_{OL}	I_{OL}=−0.4mA SDATA	0.0		0.4	V

Clock Input Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units	Remarks
Master Clock Frequency	MCK	XIN, XOUT		3.6864 3.579545		MHz	
High level input voltage	V_{MCK1_IH}	XIN	1.5			V	*1)
Low level input voltage	V_{MCK1_IL}	XIN			0.4	V	*1)
Input amplitude	V_{MCK2}	XIN	0.2		1.0	V_{PP}	*2)

*1) When directly connects to XIN pin, refer to "Recommended External Application" 7) Oscillator circuit Fig. 7.
*2) When connects to XIN pin via capacitor, refer to "Recommended External Application" 7) Oscillator circuit Fig. 8.

Current Consumption

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
Current Consumption	IDD0	Mode 0 OSC:OFF, Audio: OFF, Sub-Audio: OFF		0.08	0.14	mA
	IDD1	Mode 1 OSC: ON , Audio: OFF, Sub-Audio: OFF		0.7	1.0	
	IDD2	Mode 2 OSC: ON , Audio: ON , Sub-Audio: OFF		4.5	5.8	
	IDD3	Mode 3 OSC: ON , Audio: OFF, Sub-Audio: ON		1.6	2.1	
	IDD4	Mode 4 OSC: ON , Audio: ON , Sub-Audio: ON		5.3	6.7	

Analog Characteristics

Unless otherwise specified, the following apply: MCK=3.6864MHz, f=1kHz, Emphasis: on, Compandor: on, Scrambler: off, VR1=VR2=VR3=VR4=0dB, HPF=LMT=1 with the external circuit shown in page.28 to 32.
"dBx" is a standardized notation to match the operating voltage and is defined by equation 0dBx = -5+20log(VDD/2)dBm. 0dBm=0.775Vrms.

1) TX Audio system characteristics

Parameter	Condition	Min.	Typ.	Max.	Units	Remarks
Standard input level	@TXINO, EXTINO		-10		dBx	
Absolute gain	TXINO to MOD	-1.5	0	+1.5	dB	
	EXTIN to MOD	-1.5	0	+1.5	dB	
Distortion	EXTIN to MOD, EXTINO=-3dBx When LMT is set to 0 30kHz Low-pass filtering			-35	dB	
Limit level	EXTIN to MOD Without external R adjustment With external R adjustment	-8.6	-7.6	-6.6 -6.6	dBx	
Compressor linearity	TXINO to MOD TXINO=-44dBx TXINO=-50dBx Relative value to 0dB for MOD level of -10dBx TXINO.	-20.0 -24.0	-17.0 -20.0	-14.0 -16.0	dB	
Compressor distortion	TXINO to MOD TXINO=-10dBx 30kHz Low-pass filtering			-35	dB	
Noise level with no signal input	TXINO to MOD C-Message filtering			-36.5	dBm	
VR1 Attenuation error	TXINO to MOD -6.0 dB to 4.5dB, 1.5dB/step	-1.5		+1.5	dB	
VR2 ATT error (VR24,23,22,21,20)	TXINO to MOD -3.2dB to +3.0dB, 0.2dB/step	-0.2		+0.2	dB	
VR2 ATT error (VR25=0)	TXINO to MOD Relative value when -6.4/0dB is set	-6.8	-6.4	-6.0	dB	

2) RX Audio system characteristics

Parameter	Condition	Min.	Typ.	Max.	Units	Remarks
Standard Input Level	@RXINO		-10		dBx	
Absolute gain	RXINO to FILTERO	-1.5	0	+1.5	dB	
	RXINO to RXOUT	-1.5	0	+1.5	dB	
Expander linearity	RXINO to RXOUT RXINO=-25dBx RXINO=-30dBx Relative value to 0dB for RXOUT level of -10dBx RXINO	-33.0 -45.0	-30.0 -40.0	-27.0 -35.0	dB	
Expander distortion	RXINO to RXOUT RXINO=-5dBx 30kHz Low-pass filtering			-35	dB	
Noise level with no signal input	RXINO to RXOUT C-Message Filtering			-70	dBm	

Parameter	Condition	Min.	Typ.	Max.	Units	Remarks
VR3 Attenuation error	RXIN0 to RXOUT -4.0dB to +3.5dB, 0.5dB/step	-0.5		+0.5	dB	
VR4 Attenuation error	RXIN0 to RXOUT -4.5 to +4.5dB, 1.5dB/step	-0.25		+0.25	dB	
VR4 ATT error (VR45…40=0,0,0,0,0,0)	RXIN0 to RXOUT Relative value when –18/0dB is set	-20	-18	-16	dB	

3) Audio Filter Characteristics

3.1) Emphasis: **on**, Compandor: off, Scrambler: off

Parameter	Condition		Min.	Typ.	Max.	Units	Remarks
TX overall characteristics	TXINO to MOD Relative value to gain at 1kHz	250Hz		-57	-40	dB	
		300Hz	-12.5		-9.5	dB	SPL=0 fc=2.55K
		2.5kHz	+6.0		+9.0		
		3.0kHz	+4.5		+8.5		
		6.0kHz		-23	-18		
		300Hz	-12.5		-9.5	dB	SPL=1 fc=3.0K
		2.5kHz	+6.0		+9.0		
		3.0kHz	+7.0		+10.5		
		6.0kHz		-17	-12		
RX overall characteristics	RXINO to RXAF Relative value to gain at 1kHz	250Hz		-38	-26	dB	
		300Hz	+8.5		+11.5		
		3.0kHz	-11.5		-8.5		
		6.0kHz		-52	-40		

3.2) Emphasis: **off**, Compandor: off, Scrambler: off (Design target values)

Parameter	Condition		Min.	Typ.	Max.	Units	Remarks
TX overall characteristics	TXINO to MOD Relative value to gain at 1kHz	250Hz		-50	-38	dB	
		300Hz to 2.0kHz	-1.0		+1.0	dB	SPL=0 fc=2.55K
		2.5kHz	-1.5		+1.0		
		3.0kHz	-4.0		-1.0		
		6.0kHz		-32	-28		
		300Hz to 2.5kHz	-1.0		+1.0	dB	SPL=1 fc=3.0K
		3.0kHz	-1.5		+1.0		
		6.0kHz		-26	-22		
RX overall characteristics	RXINO to RXAF Relative value to gain at 1kHz	250Hz		-49	-38	dB	
		300Hz	-1.5		+1.0		
		350Hz to 3.0kHz	-1.0		+1.0		
		6.0kHz		-38	-28		

- Audio path frequency response for TX

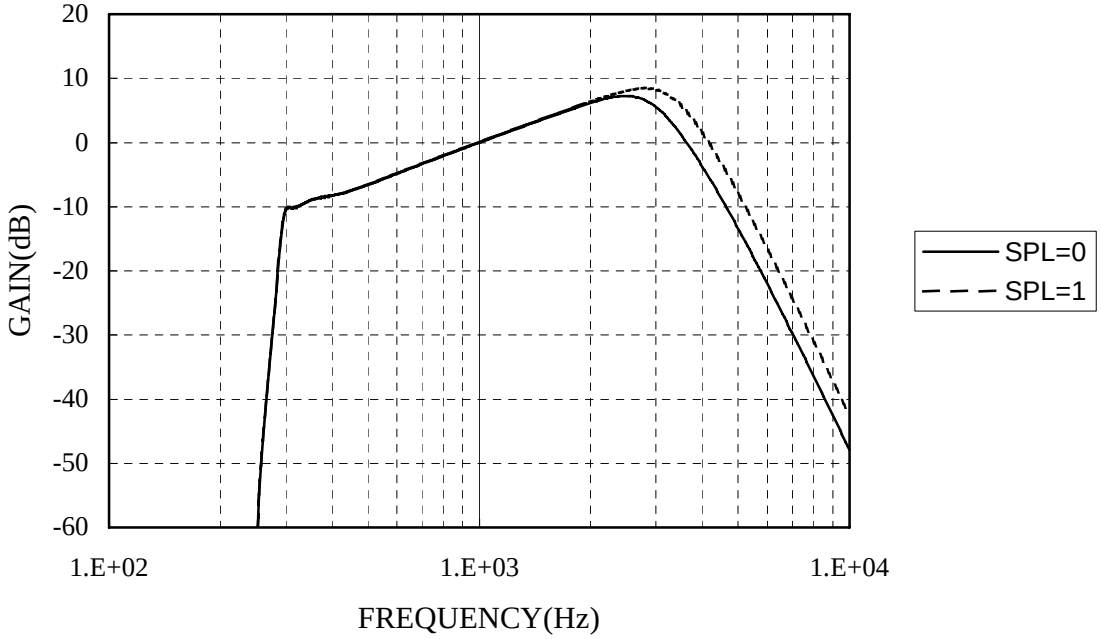


Figure 1: TX overall response with pre-emphasis.

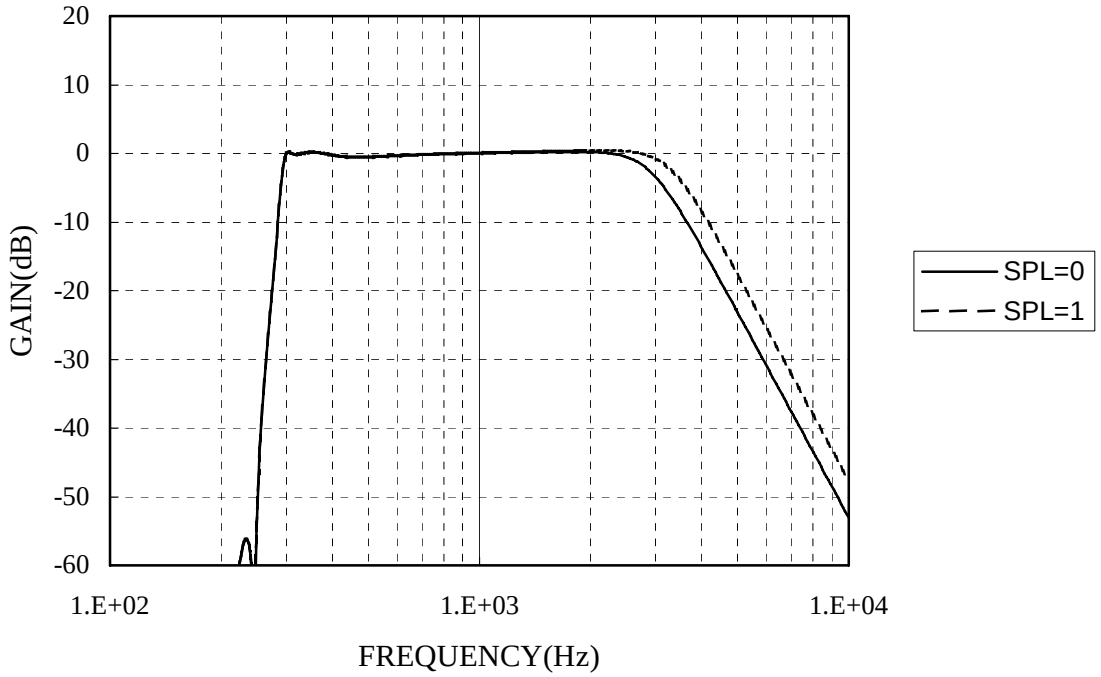


Figure 2: TX overall response without pre-emphasis.

- Audio path frequency response for RX

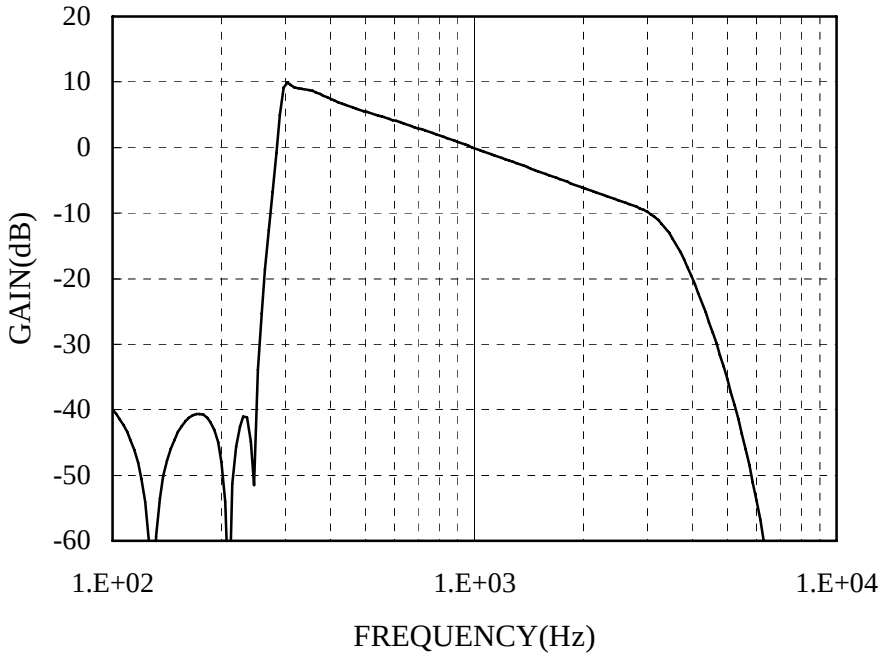


Figure 3: RX overall response with de-emphasis.

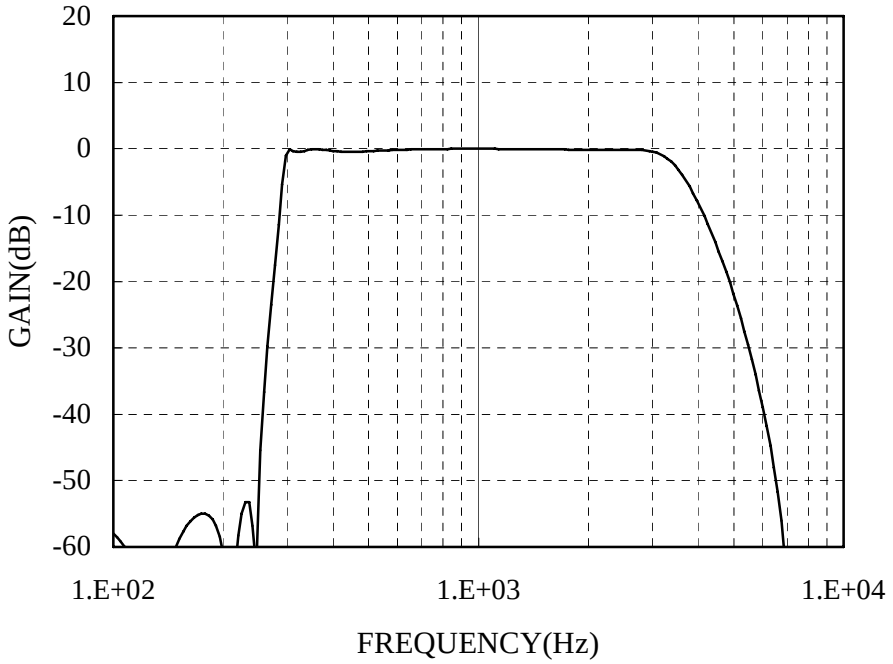


Figure 4: RX overall response without de-emphasis.

4) Scrambler Characteristics

4.1) Scrambler: **on**, Emphasis: off, Compandor: off, MCKSL=1, SCSL=0/1…3.388kHz
MCKSL=0, SCSL=0 …3.290kHz

Parameter	Condition	Min.	Typ.	Max.	Units	Remarks
Carrier frequency			3.388 3.290		kHz	
Modulated output	TXINO to MOD, RXINO to RXOUT Input level 1.0kHz -10dBx Measuring-freq. 2.388kHz (3.388kHz) Measuring-freq. 2.290kHz (3.290kHz)	-12	-10	-8	dBx	
High frequency rejection	TXINO to MOD, RXINO to RXOUT Input level 1.0kHz -10dBx Measuring-freq. 4.388kHz (3.388kHz) Measuring-freq. 4.290kHz (3.290kHz)			-50	dBx	
Carrier signal leakage	TXINO to MOD, RXINO to RXOUT Input level No signal Measuring-freq. 3.388kHz Measuring-freq. 3.290kHz			-50	dBx	
Original signal leakage	TXINO to MOD, RXINO to RXOUT Input level 1.0kHz -10dBx Measuring-freq. 1.0kHz			-50	dBx	

4.2) Scrambler: **on**, Emphasis: off, Compandor: off, MCKSL=0, SCSL=1 (Design target values)

Parameter	Condition	Min.	Typ.	Max.	Units	Remarks
Carrier frequency			3.390		kHz	
Modulated output	TXINO to MOD, RXINO to RXOUT Input level 1.0kHz -10dBx Measuring-freq. 2.390kHz	-12	-10	-8	dBx	
High frequency rejection	TXINO to MOD, RXINO to RXOUT Input level 1.0kHz -10dBx Measuring-freq. 4.390kHz			-50	dBx	
Carrier signal leakage	TXINO to MOD, RXINO to RXOUT Input level No signal Measuring-freq. 3.390kHz			-50	dBx	
Original signal leakage	TXINO to MOD, RXINO to RXOUT Input level 1.0kHz -10dBx Measuring-freq. 1.0kHz			-25	dBx	

5) Sub-Audio filter Characteristics
Unless otherwise specified, the following apply: MCKSL=1, SA5=1, SA4=1, SA3=0, SA2=0, SA1=0, SA0=1(fc=260.9Hz), VR5=0dB, 250.3Hz sinusoidal wave.

5.1) Analog characteristics

Parameter	Condition	Min.	Typ.	Max.	Units	Remarks
Standard input level	@ TSAOUT		-10		dBx	
Transmit CTCSS signal gain	DINO to TSAOUT	-2	0	+2	dB	
Transmit CTCSS signal distortion	DINO to TSAOUT 250.3Hz,Duty50%, 585mVp-p(@3V)rectangular wave 30kHz Low-pass filtering		-37	-32	dB	
Standard input level	@ RSAOUT		-10		dBx	
Receive CTCSS signal gain	RXINO to RSAOUT	-2	0	+2	dB	
Receive CTCSS signal distortion	RXINO to RSAOUT RXINO=-10dBx input 30kHz Low-pass filtering		-37	-32	dB	
VR5 Attenuation error	RXINO to RSAOUT -6.0 to +6.0dB, 0.5dB/step	-0.5		+0.5	dB	

5.2) Filter characteristics

Parameter	Condition		Min.	Typ.	Max.	Units	Remarks
Overall characteristics @fc=260.9Hz	DINO to TSAOUT Relative value to gain at 100Hz	50～240Hz 250Hz 300Hz	-1.0 -1.5		+1.0 +1.0 -38	dB	

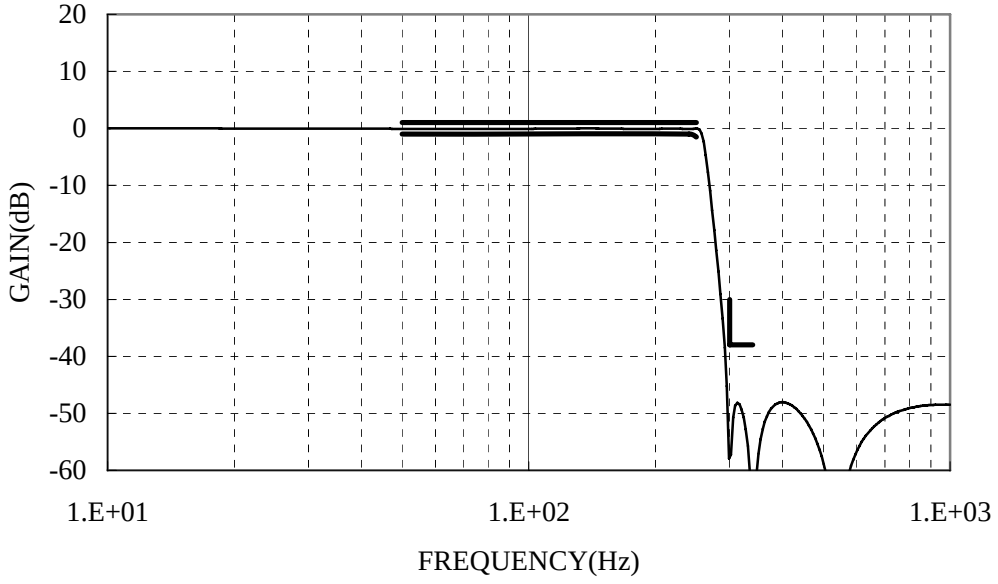
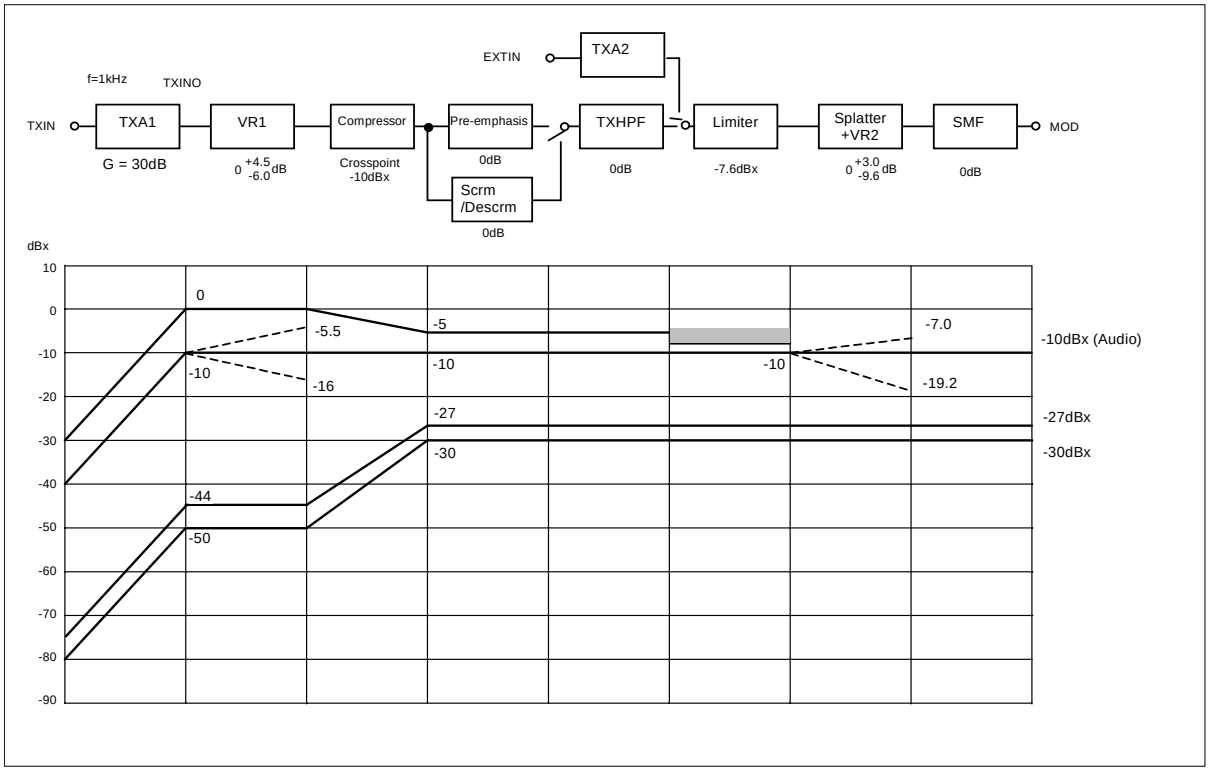


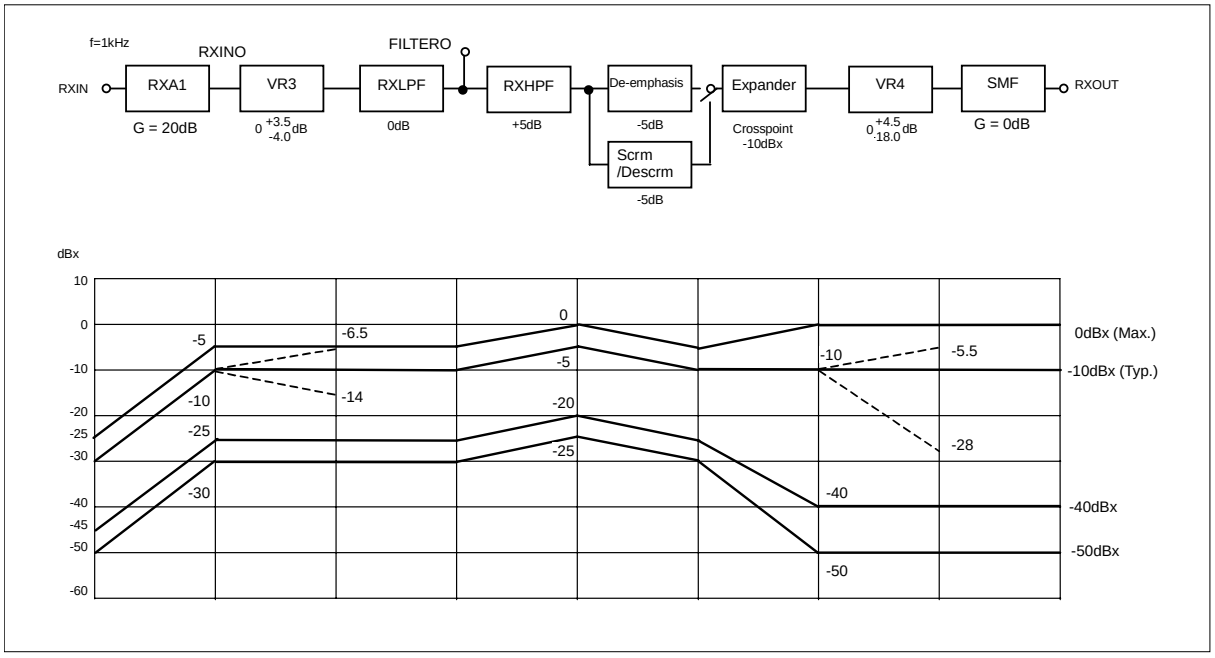
Fig.5 Sub-Audio response characteristics

Level Diagram

1) TX system: TXRX=0



2) RX system: TXRX=1

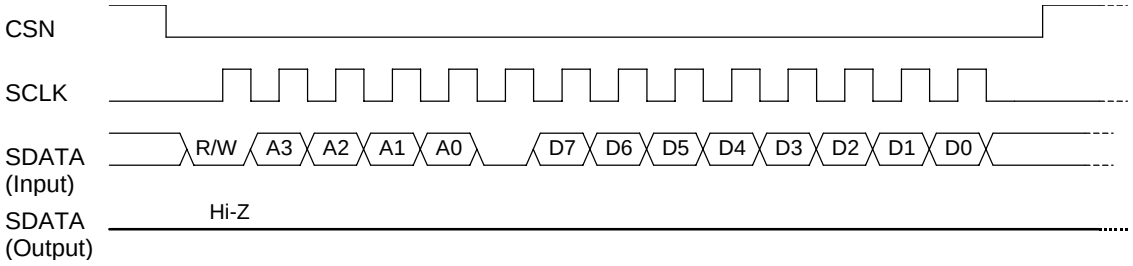


Note) dBx is a standardized notation to match the operating voltage and is defined by equation 0dBx = -5 + 20log(VDD/2)dBm.

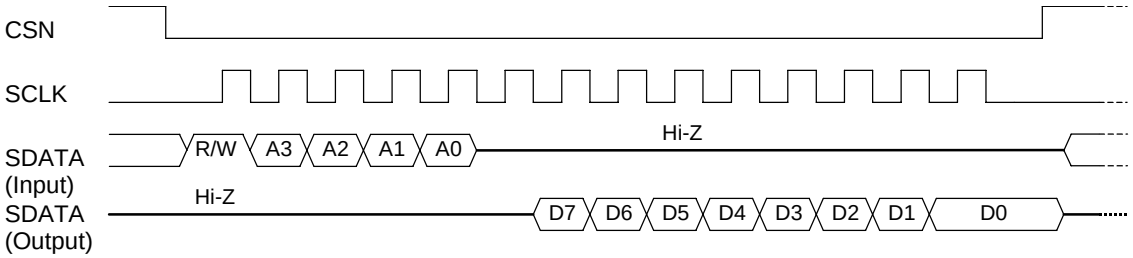
Digital AC timing

1) Serial Interface Timing
AK2347A is connected to a CPU by three-wired interface through CSN, SCLK and SDATA pins, which can make reading and writing data for control registers.
Serial data named SDATA is consist of 1-bit read and write instruction(R/W), 4-bit address (A3 to A0) and 8-bit data(D7 to D0) in one frame.

Write mode



Read mode



R/W : Instruction bit controls to write data to AK2347A or read back from it. When set to low, AK2347A is in write mode. When set to high, AK2347A is in read mode.

A3 to A0: Register address to be accessed.

D7 to D0: Write or read date to be accessed.

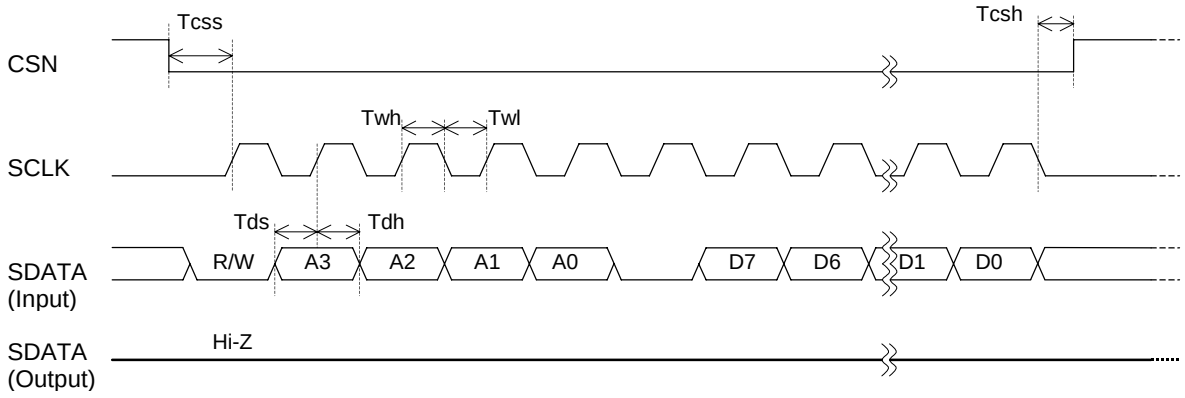
(1) CSN(Chip select) is normally selected high for disable.
When CSN is set to low, serial interface becomes active.

(2) In write mode, instruction, address and data input from SDATA pin are synchronized and latched with the rising edge of 14 iterations of SCLK clock. Set to low between address A0 and data D7.
In read mode, instruction and address are synchronized and latched with the rising edge of 5 iterations of SCLK clock. And the register data are output from SDATA pin synchronized with the falling edge of 9 iterations of SCLK clock. The date between address A0 and data D7 is unstable.
A CPU port to SDATA pin is fixed to High-Z during the interval that SDATA outputs the read data.

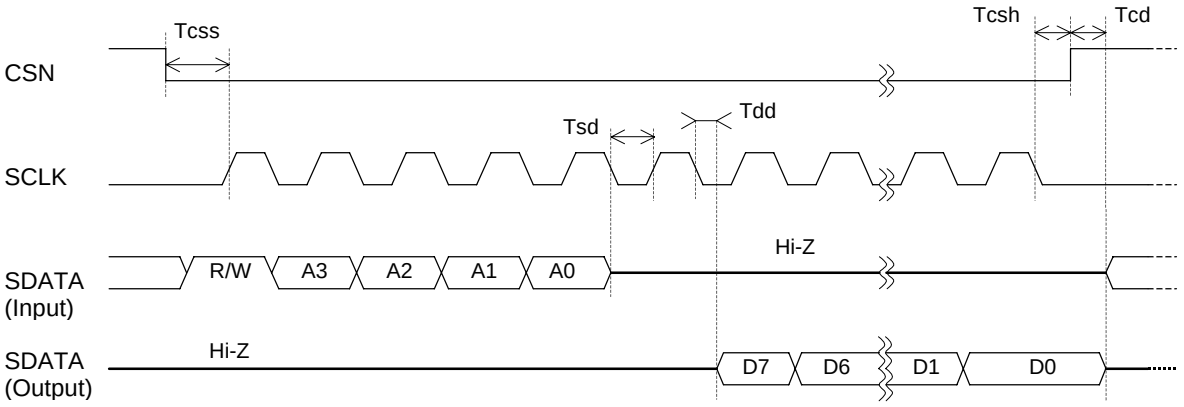
(3) AK2347A assumes that write and read is set by 14 iterations SCLK clock while CSN sets to Low. If SCLK iterations are less or more than 14 clocks, serial data would not set properly.

2) Detail Timing Chart

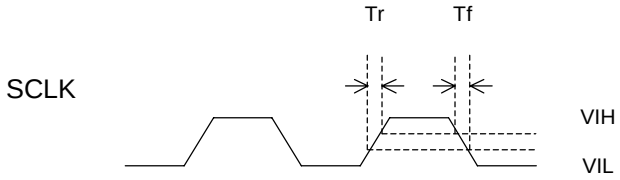
Write mode



Read mode



Rising and falling time



Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
CSN setup time	Tcss		100			ns
SDATA setup time	Tds		100			ns
SDATA hold time	Tdh		100			ns
SCLK high time	Twh		500			ns
SCLK low time	Twl		500			ns
CSN hold time	Tcsh		100			ns
SDATA Hi-Z setup time	Tsd		500			ns
SCLK to SDATA delay time	Tdd	20pF load			500	ns
CSN to SDATA delay time	Tcd	20pF load		100		ns
SCLK rising time	Tr				100	ns
SCLK falling time	Tf				100	ns

Note) In digital input timing, rising time is relative to VIH and falling time is relative to VIL.
In digital output timing, rising time is relative to VOH and falling time is relative to VOL.

Register Function Description

1) Register configuration

Address				Function	Data							
A3	A2	A1	A0		D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	Control register 1	BS3	BS2	BS1	TXRX	TXSW2	TXSW1	RXSW	MCKSL
0	0	0	1	Control register 2	TC	EM	PCONT	SPL	SCSL	LMT	HPF	SASW
0	0	1	0	Volume register 1	VR54	VR53	VR52	VR51	VR50	VR12	VR11	VR10
0	0	1	1	Volume register 2	FILSW2	FILSW1	VR25	VR24	VR23	VR22	VR21	VR20
0	1	0	0	Volume register 3	–	–	–	–	VR33	VR32	VR31	VR30
0	1	0	1	Volume register 4	–	–	VR45	VR44	VR43	VR42	VR41	VR40
0	1	1	0	Sub-Audio frequency	–	–	SA5	SA4	SA3	SA2	SA1	SA0
0	1	1	1	Software-reset & Revision register	–	–	–	RSTN	REVNUM[3:0]			
1	0/1	0/1	0/1	Reserved	X	X	X	X	X	X	X	X

Note1) The mark "–" means that a write to those bits does not have any influence on the LSI operation and read back the writing data.

Note2) All registers except address 0111 are write and readable registers.

Caution) Never access the mark "X" test register and unlisted bits of VR33 to VR30, VR45 to VR40 and SA5 to SA1. If an access is made to these addresses inadvertently, the LSI operation is not guaranteed.

2) Descriptions of registers

2.1) Control register 1

Address				Data							
A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	BS3	BS2	BS1	TXRX	TXSW2	TXSW1	RXSW	MCKSL
When power-down				0	0	0	1	1	1	1	1

2.1.1) Operation mode setting

BS3	BS2	BS1	Mode name	OSC and AGND system	TX and RX audio system	Sub-Audio system
0	0	0	Mode 0 (Power-down)	OFF	OFF	OFF
0	0	1	Mode 1 (standby)	ON	OFF	OFF
0	1	0	Mode 2	ON	ON	OFF
0	1	1	Mode 3	ON	OFF	ON
1	0/1	0/1	Mode 4	ON	ON	ON

2.1.2) TX and RX setting

Data	Item	Function		Remarks
		0	1	
TXRX	TX-RX switch	TX operation *1)	RX operation *2)	*3)
RXSW	RX audio mute	Mute	Normal operation	*4)
MCKSL	Master clock frequency	3.579545MHz	3.6864MHz	

2.1.3) TX path setting

TXSW2	TXSW1	Function	Remarks
1	1	Mute (AGND → Limiter → Splatter)	
0	1	Audio system operation (HPF → Limiter→ Splatter)	
1	0	External signal operation (EXTIN pin → Limiter → Splatter)	
0	0	Audio signal and external signal added together (HPF+EXTIN pin → Adder → Limiter → Splatter)	

*1) When TXRX is set to 0 and RXSW is set to 1, the signal input from the TXIN pin can be output to the RXOUT pin. In this case, because use of the Scrambler/Descrambler is inhibited, be sure to set PCONT to 1.
When RXSW is set to 0, the RXOUT pin output is muted.

*2) When TXRX is set to 1 and TXSW2 and TXSW1 are set to 0 and 1 respectively, the signal input from the RXIN pin can be output to the MOD pin. In this case, because use of the Scrambler/Descrambler is inhibited, be sure to set PCONT to 1. When TXSW2 and TXSW1 are set to 1 and 1 respectively, the MOD pin output is muted.

*3) Set the gain level for each circuit block properly according to the level diagrams on page 15.

*4) If RXSW is set to 0, the FILTERO pin output is not muted.

2.2) Control register 2

Address				Data							
A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	TC	EM	PCONT	SPL	SCSL	LMT	HPF	SASW
When power-down				1	1	1	1	0	1	1	1

Data	Item	Function		Remarks
		0	1	
TC	Compandpr	OFF (Bypass)	ON (Active)	
SPL	Splatter Cut-off frequency	2.55kHz	3.0kHz	
SCSL	Scrambler carrier frequency MCKSL is set to 0	3.290kHz	3.390kHz	
	MCKSL is set to 1	3.388kHz	3.388kHz	
LMT	Limiter	OFF (Bypass)	ON (Active)	
HPF	TX/RX HPF	OFF (Bypass)	ON (Active)	
SASW	Sub-Audio operation	DIN pin → TSAOUT pin	RXIN pin → RSAOUT pin	

EM	PCONT	Function	Remarks
1	1	Emphasis: ON (Active), Scrambler/Descrambler: OFF (Bypass)	
0	1	Emphasis: OFF (Bypass), Scrambler/Descrambler:OFF (Bypass)	
0/1	0	Emphasis: OFF (Bypass), Scrambler/Descrambler:ON (Active)	

2.3) Volume Register 1

Address				Data							
A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	VR54	VR53	VR52	VR51	VR50	VR12	VR11	VR10
When power-down				0	1	1	0	0	1	0	0

VR54	VR53	VR52	VR51	VR50	VR5 gain (dB)
0	0	0	0	0	-6.0
0	0	0	0	1	-5.5
0	0	0	1	0	-5.0
0	0	0	1	1	-4.5
0	0	1	0	0	-4.0
0	0	1	0	1	-3.5
0	0	1	1	0	-3.0
0	0	1	1	1	-2.5
0	1	0	0	0	-2.0
0	1	0	0	1	-1.5
0	1	0	1	0	-1.0
0	1	0	1	1	-0.5
0	1	1	0	0	0.0
0	1	1	0	1	+0.5
0	1	1	1	0	+1.0
0	1	1	1	1	+1.5
1	0	0	0	0	+2.0
1	0	0	0	1	+2.5
1	0	0	1	0	+3.0
1	0	0	1	1	+3.5
1	0	1	0	0	+4.0
1	0	1	0	1	+4.5
1	0	1	1	0	+5.0
1	0	1	1	1	+5.5
1	1	0	0	0	+6.0

VR12	VR11	VR10	VR1 gain (dB)
0	0	0	-6.0
0	0	1	-4.5
0	1	0	-3.0
0	1	1	-1.5
1	0	0	0.0
1	0	1	+1.5
1	1	0	+3.0
1	1	1	+4.5

2.4) Volume Register 2

Address				Data							
A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	FILSW2	FILSW1	VR25	VR24	VR23	VR22	VR21	VR20
When power-down				1	1	1	1	0	0	0	0

FILSW2	FILSW1	Function	Remarks
1	1	FILTERO pin output is muted.	
0	1	RXLPF circuit signal is output on FILTERO pin.	
0/1	0	TX/RX_HPF circuit signal is output on FILTERO pin.	

VR25	VR2 gain (dB)
0	-6.4
1	0.0

VR24	VR23	VR22	VR21	VR20	VR2 gain (dB)
0	0	0	0	0	-3.2
0	0	0	0	1	-3.0
0	0	0	1	0	-2.8
0	0	0	1	1	-2.6
0	0	1	0	0	-2.4
0	0	1	0	1	-2.2
0	0	1	1	0	-2.0
0	0	1	1	1	-1.8
0	1	0	0	0	-1.6
0	1	0	0	1	-1.4
0	1	0	1	0	-1.2
0	1	0	1	1	-1.0
0	1	1	0	0	-0.8
0	1	1	0	1	-0.6
0	1	1	1	0	-0.4
0	1	1	1	1	-0.2
1	0	0	0	0	0.0
1	0	0	0	1	+0.2
1	0	0	1	0	+0.4
1	0	0	1	1	+0.6
1	0	1	0	0	+0.8
1	0	1	0	1	+1.0
1	0	1	1	0	+1.2
1	0	1	1	1	+1.4
1	1	0	0	0	+1.6
1	1	0	0	1	+1.8
1	1	0	1	0	+2.0
1	1	0	1	1	+2.2
1	1	1	0	0	+2.4
1	1	1	0	1	+2.6
1	1	1	1	0	+2.8
1	1	1	1	1	+3.0

2.5) Volume Register 3

Address				Data							
A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	–	–	–	–	VR33	VR32	VR31	VR30
When power-down				–	–	–	–	1	0	0	0

VR33	VR32	VR31	VR30	VR3 gain (dB)
0	0	0	0	-4.0
0	0	0	1	-3.5
0	0	1	0	-3.0
0	0	1	1	-2.5
0	1	0	0	-2.0
0	1	0	1	-1.5
0	1	1	0	-1.0
0	1	1	1	-0.5
1	0	0	0	0.0
1	0	0	1	+0.5
1	0	1	0	+1.0
1	0	1	1	+1.5
1	1	0	0	+2.0
1	1	0	1	+2.5
1	1	1	0	+3.0
1	1	1	1	+3.5

2.6) Volume Register 4

Address				Data							
A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	–	–	VR45	VR44	VR43	VR42	VR41	VR40
When power-down				–	–	0	1	0	0	1	1

VR45	VR44	VR43	VR42	VR41	VR40	VR4 gain (dB)
0	0	0	0	0	0	-18.0
0	0	0	0	0	1	-4.50
0	0	0	0	1	0	-4.25
0	0	0	0	1	1	-4.00
0	0	0	1	0	0	-3.75
0	0	0	1	0	1	-3.50
0	0	0	1	1	0	-3.25
0	0	0	1	1	1	-3.00
0	0	1	0	0	0	-2.75
0	0	1	0	0	1	-2.50
0	0	1	0	1	0	-2.25
0	0	1	0	1	1	-2.00
0	0	1	1	0	0	-1.75
0	0	1	1	0	1	-1.50
0	0	1	1	1	0	-1.25
0	0	1	1	1	1	-1.00
0	1	0	0	0	0	-0.75
0	1	0	0	0	1	-0.50
0	1	0	0	1	0	-0.25
0	1	0	0	1	1	0.00
0	1	0	1	0	0	+0.25
0	1	0	1	0	1	+0.50
0	1	0	1	1	0	+0.75
0	1	0	1	1	1	+1.00
0	1	1	0	0	0	+1.25
0	1	1	0	0	1	+1.50
0	1	1	0	1	0	+1.75
0	1	1	0	1	1	+2.00
0	1	1	1	0	0	+2.25
0	1	1	1	0	1	+2.50
0	1	1	1	1	0	+2.75
0	1	1	1	1	1	+3.00
1	0	0	0	0	0	+3.25
1	0	0	0	0	1	+3.50
1	0	0	0	1	0	+3.75
1	0	0	0	1	1	+4.00
1	0	0	1	0	0	+4.25
1	0	0	1	0	1	+4.50

2.7) Sub-Audio LPF frequency

Address				Data							
A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	–	–	SA5	SA4	SA3	SA2	SA1	SA0
When power-down				–	–	1	1	0	0	0	1

SA5	SA4	SA3	SA2	SA1	SA0	Divide *1)	MCKSL=0(3.579545M)		MCKSL=1(3.6864MHz)	
							Cut-off Frequency (Hz)	Target CTCSS (Hz)	Cut-off Frequency (Hz)	Target CTCSS (Hz)
0	0	0	0	0	0	640	59.4	-	61.1	-
0	0	0	0	0	1	630	60.3	-	62.1	-
0	0	0	0	1	0	620	61.3	-	63.1	-
0	0	0	0	1	1	610	62.3	-	64.1	-
0	0	0	1	0	0	600	63.3	-	65.2	-
0	0	0	1	0	1	590	64.4	-	66.3	-
0	0	0	1	1	0	580	65.5	-	67.5	-
0	0	0	1	1	1	570	66.7	-	68.6	-
0	0	1	0	0	0	560	67.8	-	69.9	-
0	0	1	0	0	1	550	69.1	-	71.1	-
0	0	1	0	1	0	540	70.3	-	72.5	67.0
0	0	1	0	1	1	530	71.7	67.0	73.8	-
0	0	1	1	0	0	520	73.1	-	75.2	69.3
0	0	1	1	0	1	510	74.5	69.3	76.7	71.9
0	0	1	1	1	0	500	76.0	-	78.3	-
0	0	1	1	1	1	490	77.6	71.9	79.8	74.4
0	1	0	0	0	0	480	79.2	-	81.5	-
0	1	0	0	0	1	470	80.6	74.4	83.3	77.0
0	1	0	0	1	0	460	82.6	77.0	85.1	79.7
0	1	0	0	1	1	450	84.4	-	87.0	-
0	1	0	1	0	0	440	86.3	79.7	89.0	82.5
0	1	0	1	0	1	430	88.4	82.5	91.0	85.4
0	1	0	1	1	0	420	90.4	-	93.2	-
0	1	0	1	1	1	410	92.7	85.4	95.5	88.5
0	1	1	0	0	0	400	95.0	88.5	97.8	91.5
0	1	1	0	0	1	390	97.4	91.5	100.3	-
0	1	1	0	1	0	380	100.0	-	103.0	94.8
0	1	1	0	1	1	370	102.7	94.8	105.8	97.4
0	1	1	1	0	0	360	105.6	97.4	108.7	100.0
0	1	1	1	0	1	350	108.6	100.0	111.8	103.5
0	1	1	1	1	0	340	111.8	103.5	115.1	107.2
0	1	1	1	1	1	330	115.1	107.2	118.6	110.9

SA5	SA4	SA3	SA2	SA1	SA0	Divide *1)	MCKSL=0(3.579545M)		MCKSL=1(3.6864MHz)	
							Cut-off Frequency (Hz)	Target CTCSS (Hz)	Cut-off Frequency (Hz)	Target CTCSS (Hz)
1	0	0	0	0	0	320	118.8	110.9	122.3	114.8
1	0	0	0	0	1	310	122.5	114.8	126.2	118.8
1	0	0	0	1	0	300	126.6	118.8	130.5	123.0
1	0	0	0	1	1	290	131.0	123.0	135.0	127.3
1	0	0	1	0	0	280	135.7	127.3	139.8	131.8
1	0	0	1	0	1	270	140.7	131.8	144.9	136.5
1	0	0	1	1	0	260	146.2	136.5	150.5	141.3
1	0	0	1	1	1	250	152.0	141.3	156.5	146.2
1	0	1	0	0	0	240	158.3	146.2 151.4	163.0	151.4
1	0	1	0	0	1	230	165.2	156.7	170.1	156.7 162.2
1	0	1	0	1	0	220	172.7	162.2	177.9	167.9
1	0	1	0	1	1	210	180.9	167.9 173.8	186.4	173.8
1	0	1	1	0	0	200	190.0	179.9	195.6	179.9 186.2
1	0	1	1	0	1	190	200.0	186.2 192.8	205.9	192.8
1	0	1	1	1	0	180	211.1	203.5	217.3	203.5 210.7
1	0	1	1	1	1	170	222.9	210.7	229.6	218.1
1	1	0	0	0	0	160	237.5	218.1 225.7	244.5	225.7 233.6
1	1	0	0	0	1	150	253.2	233.6 241.8	260.9	241.8 250.3
1	1	0	0	1	0	140	271.3	250.3 (254.1)	279.5	(254.1) (268.8)
1	1	0	0	1	1	130	292.4	(268.8)	300.9	-
1	1	0	1	0	0	120	316.7	-	326.0	-
1	1	0	1	0	1	110	345.3	-	355.8	-
1	1	0	1	1	0	100	379.9	-	391.3	-
1	1	0	1	1	1	90	422.2	(403.2)	434.7	(403.2)
1	1	1	0	0	0	80	475.0	-	489.0	-
1	1	1	0	0	1	70	542.7	-	559.1	-

*1) Divide = 10 x [64 – (register setting value)]
This equation states that Divide is divided number of master clock.

2.8) Software reset & revision register

Address				Data							
A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	–	–	–	RSTN	REVNUM[3:0]			
When power-down				–	–	–	1	0	0	1	0

2.8.1) Software rest

When D4: RSTN data is set to 0, software reset is executed and all register data is set to power-down status and. This register is a write only register and set to 1 automatic after completing software reset.

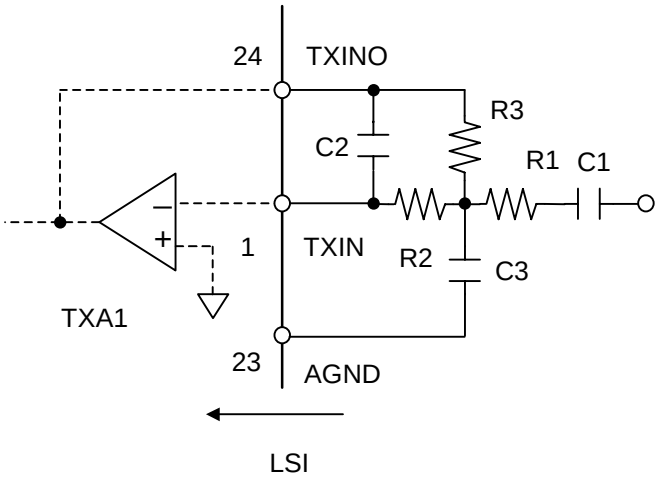
2.8.2) Revision register

When D3 to D0 data is accessed, users can read the number of mask revision.
This register is a read only register.

Recommended External Application Circuits

1) TXA1 amplifier

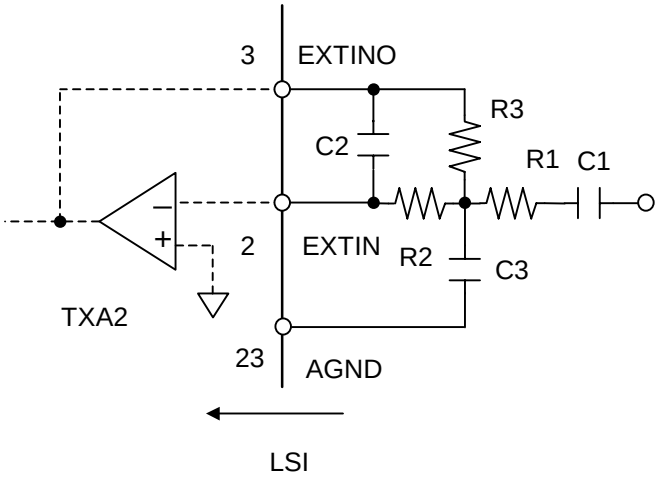
This circuit can be used as the TX microphone amplifier. Set the gain to 30dB or less. If there is a possibility that a high frequency noise component over 100kHz is input, form a first or second order anti-aliasing filter. The following gives a sample configuration of a second order LPF with a gain of 30dB and cut-off frequency of 10kHz:



C1=0.47uF
C2=33pF
C3=2200pF
R1=R2=10kΩ
R3=330kΩ

2) TXA2 amplifier

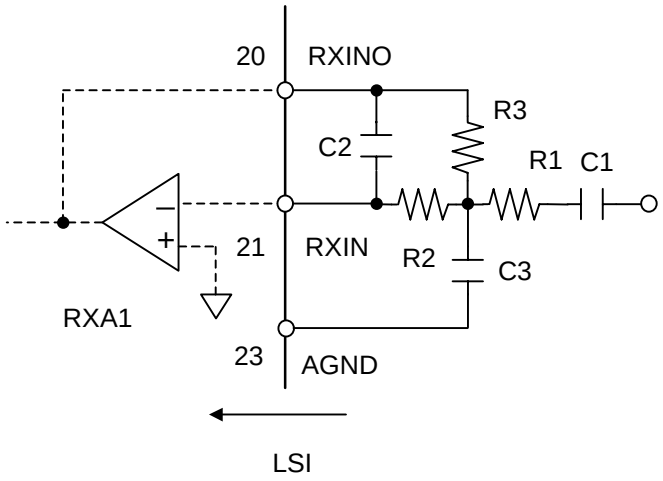
This amplifier is used for adjusting the gain of the tone signal. Set the gain to 0dB or less. For high frequency noise over 100kHz, form an anti-aliasing filter. The following gives a sample configuration of a second order LPF with a gain of 0dB and cut-off frequency of 13kHz:



C1=0.47uF
C2=100pF
C3=470pF
R1=R2=R3=51kΩ

3) RXA1 amplifier

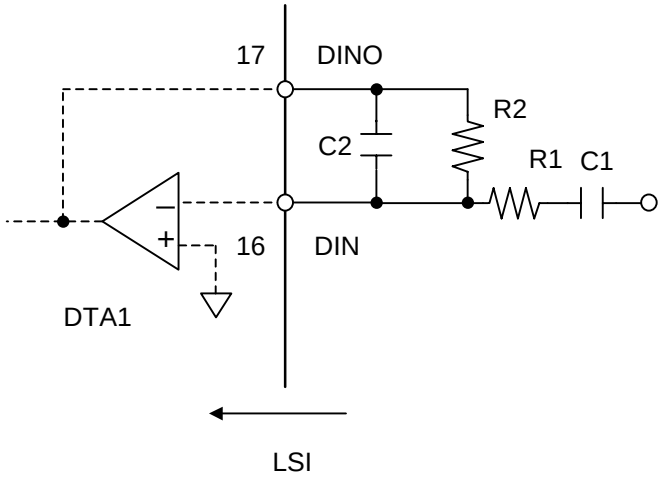
This amplifier is used for adjusting the gain of the RX signal. Set the gain to 20dB or less. For high frequency noise over 100kHz, form an anti-aliasing filter. The following gives a sample configuration of a second order LPF with a gain of 20dB and cut-off frequency of 39kHz:



C1=0.47uF
C2=33pF
C3=560pF
R1=10kΩ
R2=9.1kΩ
R3=100kΩ

4) DTA1 amplifier

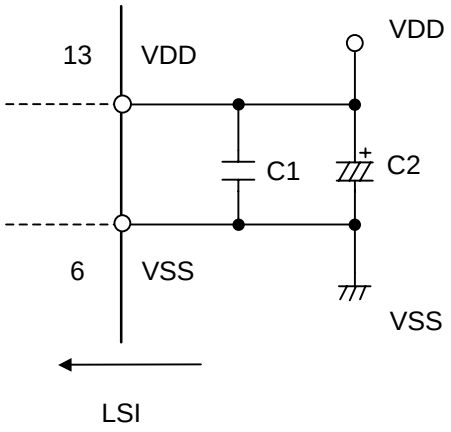
This amplifier is used for adjusting the gain of the signal to Sub-Audio Programmable LPF. Set the gain to 0dB or less. For high frequency noise over 100kHz, form an anti-aliasing filter. The following gives a sample configuration of a second order LPF with a gain of 0dB and cut-off frequency of 7.2kHz:



C1=0.47uF
C2=220pF
R1=R2=100kΩ

5) Power supply stabilizing capacitors

Connect capacitors between VDD and VSS pins to eliminate ripple and noise included in power supply. For maximum effect, the capacitors should be placed at a shortest distance between the pins.

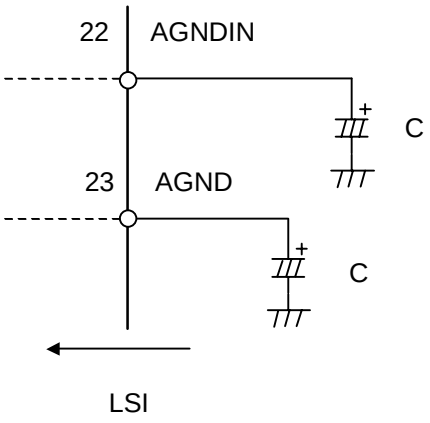


C1=0.1uF (Ceramic cap)

C2=22uF (Electrolytic cap)

6) AGND stabilizing capacitors

It is recommended that capacitors with 0.3μF or lager be connected between VSS and the AGND and AGNDIN pins to stabilize the AGND signal. The capacitors must be placed as close to the pins as possible.



C=1uF (Electrolytic cap)

7) Oscillator circuit

When the built-in oscillator circuit is to be used, connect a 3.6864MHz or 3.579545MHz crystal oscillator and a capacitor as shown in Fig. 6. The internal buffer is designed to allow stable oscillation of a crystal oscillator for the electrical equivalent circuitry with a resonance resistance of 150Ω (Max.) and a shunt capacitance of 5pF (Max.).
It is recommended that 22pF capacitors be connected externally so that the total load capacitance is 16pF (5pF + 22pF//22pF) or less. Place the oscillator, resistor, and capacitors as close to the XIN and XOUT pins as possible.

When an external clock is to be supplied, connect the clock line as shown in Fig. 7 or Fig. 8 according to the clock amplitude level.
The circuit in the first stage of the XIN pin has a constant threshold voltage (0.8V). Therefore, if the high level of the input clock is 1.5V or higher and the low level is 0.4V or lower, connect the clock signal as shown in Fig. 7. If the input clock amplitude (p-p value) is between 0.2V and 1.0V, connect the clock signal as shown in Fig. 8.

When the clock is to be shared with peripheral ICs, the clock must be input and output on the XIN pin. The clock amplitude must not exceed the absolute maximum ratings.

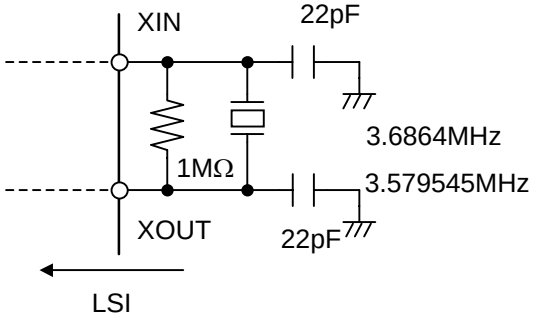


Fig. 6

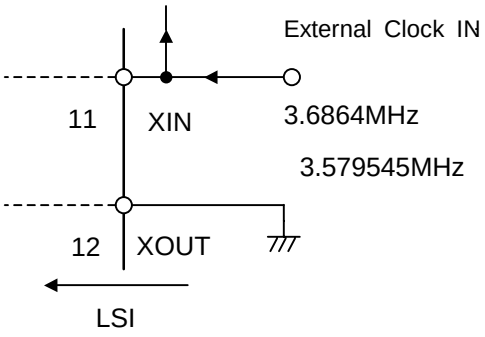


Fig. 7

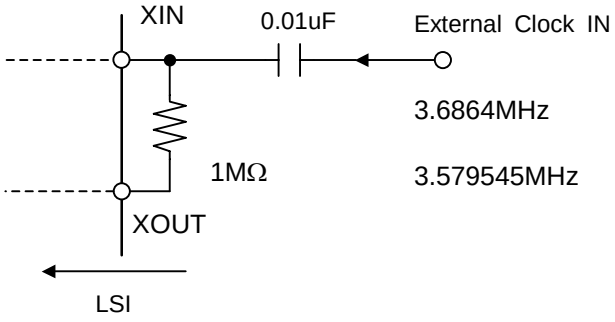


Fig. 8

8) LIMLV pin

The LIMLV pin is used for adjusting the limit level of the limiter circuit. This pin may be left open or may be used by connecting resistors as shown in the figure below.

When the pin is left open, a predetermined limit level can be obtained. The limit level is expressed as follows:

$$HVref = 0.256 \times (VDD - AGND) \quad [Vo\text{-}p]$$

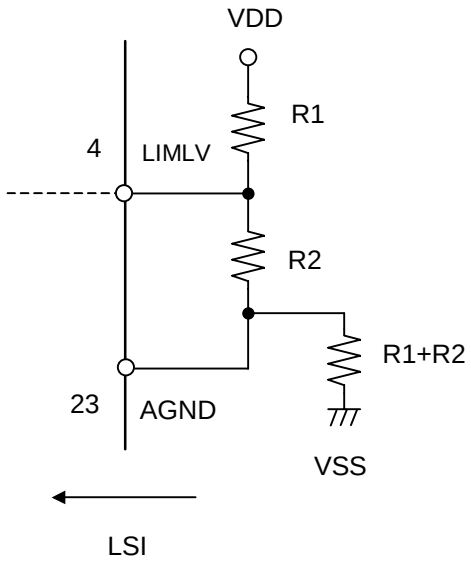
For example, let VDD be 3V. The limit level is calculated as follows:
Hvref = 0.256 × (3.0 - 1.5) = 0.384Vo-p Then, 1.5 ±0.384V is the typical value of the limit level.

When a DC voltage higher than the AGND voltage level (= 1/2VDD) is applied to the pin through resistors, the limit level can be adjusted. The limit level is the difference between LIMLV and AGND and is expressed as AGND ±(LIMLV - AGND).
Let VDD be 3V. The limit level is calculated as follows:

LIMLV=1.6V → 1.5 ±0.1V
1.7V → 1.5 ±0.2V
1.8V → 1.5 ±0.3V
1.9V → 1.5 ±0.4V
1.933V → 1.5 ±0.433V (equivalent to -6.6dBx (Max.))

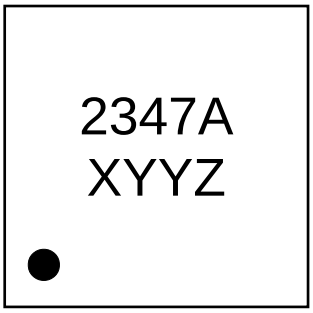
Then, the above values are obtained as the typical limit levels.

Because AGND level is used as the reference level for the limiter circuit operation as mentioned above, when resistors are connected, they should be connected so that VDD and AGND are separated by these resistors to supply a DC level to the LIMLV pin. In addition, make adjustments so that the sum of resistance (R1 + R2) is around 51kΩ.



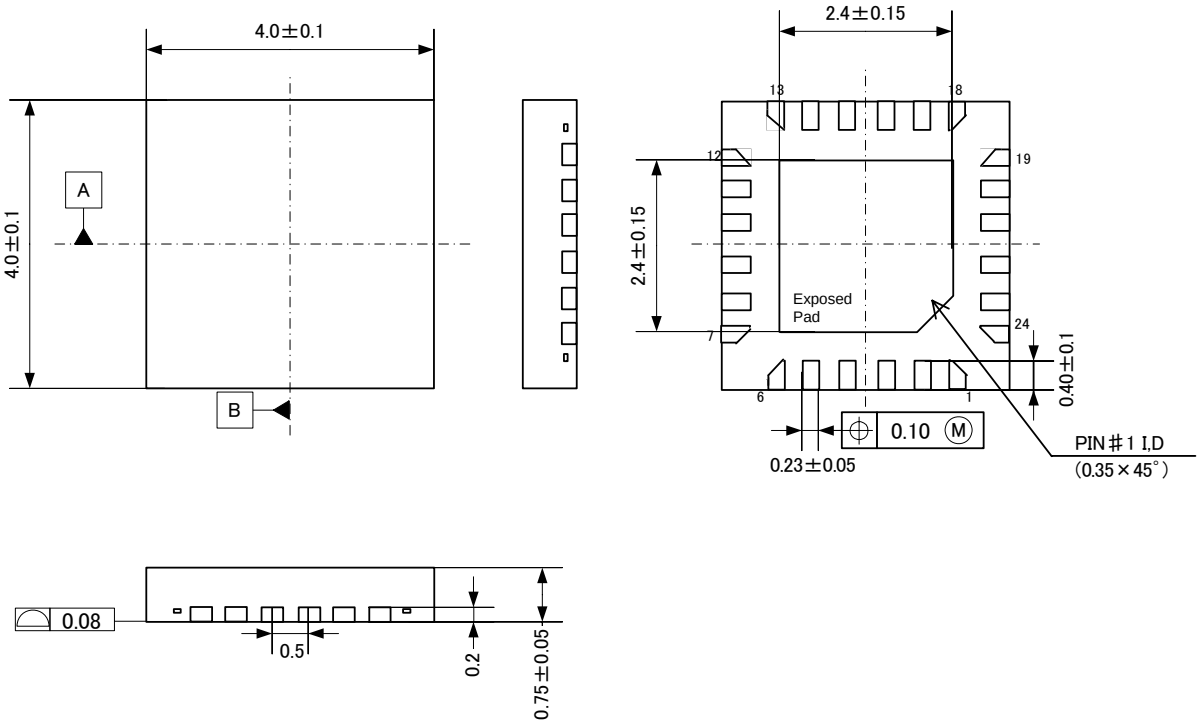
Packaging

- Marking



[Contents of XXXYZ]
XXX : Date of manufacturing
Last digit of the year, 2 digits of week number
Y : Production lot number
Z : Assembly plant code

- 24-pin QFNJ outline dimension



Note: The exposed pad at the center of the back of the package must be connected to VSS or opened.

Important Notice

IMPORTANT NOTICE

- These products and their specifications are subject to change without notice. Before considering any use or application, consult the Asahi Kasei Microsystems Co., Ltd. (AKM) sales office or authorized distributor concerning their current status.
- AKM assumes no liability for infringement of any patent, intellectual property, or other right in the application or use of any information contained herein.
- Any export of these products, or devices or systems containing them, may require an export license or other official approval under the law and regulations of the country of export pertaining to customs and tariffs, currency exchange, or strategic materials.
- AKM products are neither intended nor authorized for use as critical components in any safety, life support, or other hazard related device or system, and AKM assumes no responsibility relating to any such use, except with the express written consent of the Representative Director of AKM. As used here:
  (a) A hazard related device or system is one designed or intended for life support or maintenance of safety or for applications in medicine, aerospace, nuclear energy, or other fields, in which its failure to function or perform may reasonably be expected to result in loss of life or in significant injury or damage to person or property.
  (b) A critical component is one whose failure to function or perform may reasonably be expected to result, whether directly or indirectly, in the loss of the safety or effectiveness of the device or system containing it, and which must therefore meet very high standards of performance and reliability.
- It is the responsibility of the buyer or distributor of an AKM product who distributes, disposes of, or otherwise places the product with a third party to notify that party in advance of the above content and conditions, and the buyer or distributor agrees to assume any and all responsibility and liability for and hold AKM harmless from any and all claims arising from the use of said product in the absence of such notification.