## **VOLTAGE CONTROLLED SAW OSCILLATORS**

Performance Charac	teristics (	TA = -40 °C	to 85 °C)		
Specifications	Sym	Min	Тур	Max	Unit
Center Frequency	f <sub>N</sub>	155.52	-	622.08	MHz
Supply Current	I <sub>EE</sub>	45	55	70	mA
Supply Voltage <sup>1</sup>	V <sub>EE</sub>	-4.5	-5	-5.5	٧
Absolute Pull Range	APR	-50	-	+50	ppm
Total Freq. Deviation	Δf	-400	-	+400	ppm
Output Level Low <sup>2</sup>	v <sub>OL</sub>	-1.95	•	-1.63	٧
Output Level High <sup>2</sup>	v <sub>OH</sub>	-0.98	-	-0.75	٧
Output Rise/Fall Time <sup>3</sup>	T <sub>R/F</sub>	100	250	400	ps
Frequency Stability		-150	•	+150	ppm
Data Symmetry	Sym	45	49/51	55	%
Linearity		-3	-	+3	%
Spurious Suppression		-50	-60	-	dB
V <sub>C</sub> Input Impedance	zc	8	10	12	Ω
V <sub>C</sub> Modulation Bandwidth <sup>4</sup>	BW		500	-	kHz
V <sub>C</sub> Range	v <sub>c</sub>	V <sub>EE</sub>	-	v <sub>cc</sub>	٧
Output Current	l <sub>out</sub>	-	<u>-</u>	20	mA
Absolute Max. VC Range <sup>5</sup>	V <sub>CMX</sub>	V <sub>EE</sub> -0.5		V <sub>CC</sub> +0.5	٧
Absolute Max Output Curren	t <sup>5</sup> I <sub>MAX</sub>	-	-	50	
Storage Temperature <sup>5</sup>	_T <sub>S</sub>	-55	-	125	°C
Soldering Temp. /Time <sup>5</sup>	TLS	•	_	240/10	°C/s
Absolute Max Supply Volt <sup>5</sup>	V <sub>CC</sub> -V <sub>EE</sub>	-8		0	٧
ESD Rating (HBM,CDM)	•	-	-	1k	٧

Mechanical and Envi	ronmental Qualification			
Parameter	Test Method			
Shock and Vibration	MIL-STD-883C, 2002.3, Test A			
Solderability	MIL-STD-883C, 2003.5			
Gross and Fine Leak	MIL-STD-883C, 1014.7, 100%			
Resistance to Solvents	MIL-STD-883C, M2016			

#### **Features**

Voltage Controlled SAW Oscillator

Phase Jitter Typically <12 ps

**Output Frequency Options from 155** 

MHz to 622 MHz

Ideal for Frequency Translation and Timing Recovery Applications

100K ECL/PECL Logic Levels with Fast Transition Times

Complementary Outputs

Low-Frequency Clock Through Feature

**Output Disable Feature** 

Miniature Ceramic SMD Package (SO-28)

### Description

The VCO600A is SAW stabilized, voltage controlled oscillator that operates at the fundamental frequency of the internal SAW filter. The very stable, high-Q, quartz SAW filter enables the device to acheive very low phase jitter performance over a wide operating temperature range. The oscillator is housed in a 28-lead surface-mount package. It has a unique output disable and clock through feature to facilitate on-board testing.

The VCO-600A is available with center frequency options ranging from 155 MHz to 622 MHz, including the common SONET/SDH/ATM frequencies of 155.52 MHz, 311.04 MHz and 622.08 MHz. Typical applications would include phase locked loop circuits for frequency synthesis, frequency translation and timing recovery.

Part Number

<sup>1</sup> The VCO-600A may be configured for PECL operation. All outputs and inputs including  $V_C$  are referenced to  $V_{CC}$ 

Output levels are standard 10K ECL and are fully 100K ECL compatible.

<sup>3</sup> Transition Times are measured from 20% to 80% of a full 10K ECL level swing.

<sup>4</sup> The modulation bandwidth is a function of nominal center frequency and may be adjusted down through the use of an external capacitor on pin 17.

<sup>5</sup> Stresses in excess of the absolute maximum ratings can permanently damage the device. Functional operation is not implied at these or any other conditions in excess of conditions represented in the operational sections of this data sheet. Exposure to absolute maximum ratings for extended periods may adversely affect device reliability.

# Pinout Information

#### Pin Function

- 4 Test Clock In (CLKIN)1
- 10 Negative Supply (V<sub>EE</sub>)
- 12 Positive Supply (V<sub>CC</sub>)
- 17 Modulation Bandwidth Adjust (V<sub>BW</sub>)<sup>2</sup>
- 19 Control Voltage (V<sub>C</sub>)
- 5,6,7,8 No Connect (NC)
  - 21 Output Disable<sup>3</sup>
  - 23 ECL Output (CLKOUT)
  - 25 Complementary ECL Output (CLKOUT)
  - 2,27 Positive Supply (V<sub>CC</sub>)

1,3,9,11, Case Ground (GND)

13,14,15, Case Ground (GND)

16.18.20.22. Case Ground (GND)

24,26,28 Case Ground (GND)

## Standard Frequency (MHz)

155.520

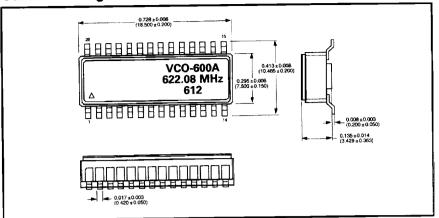
278.528

311.040

622,080

Other frequencies available upon request

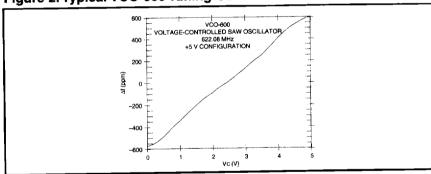
## **Outline Drawing**



## **Absolute Pull Range**

The absolute pull range (APR) is the range of frequencies to which the VCO-600 can be adjusted over the  $-0.5~\rm V$  to  $-4.5~\rm V$  control range on the VC pin. The actual tuning curve, shown in Figure 2, is much wider. APR takes into account all tolerances such as initial setting, temperature, supply, and aging variation. This ensures that the following is true over all operational and lifetime conditions: If the desired clock frequency is within the APR (i.e.,  $\pm 50~\rm ppm$ ), then the device can be set to that frequency by a control voltage within the  $-0.5~\rm V$  to  $-4.5~\rm V$  range. For PLL applications, it is important to note that the loop filter input to  $\rm V_C$  must be capable of covering this range. This is most easily accomplished with CMOS type op amps with rail-to-rail output swing.

Figure 2. Typical VCO-600 Tuning Curve



Notes: The tuning curve, when expressed in parts per million (ppm), is typical of the VCO-600 at other frequencies. The center frequency for this curve is normalized at 2.5 V. In practice, the room temperature center voltage (the voltage that tunes the device to the center frequency) is set to account for temperature and aging variations.

By setting OD low, a test signal may be applied at CLKIN and fed through the VCO-600A to both the CLKOUT and CLKOUT to facilitate on board testing. The test signal input applied at CLKIN may be either an ECL or sinewave signal (up to 1V<sub>PP</sub>, AC coupled). CLKIN is biased internally to V<sub>BB</sub> (V<sub>CC</sub>-1.3V).

<sup>2</sup> An optional capacitor to ground can be placed on VBW to reduce the modulation bandwidth for narrow bandwidth phase-lock loop applications. the modulation bandwidth will be approximately 1/(12000°C) Hz, where C is equal to the capacitance in Farads. If the optional capacitor is not utilized, VBW becomes a no connect and the modulation bandwidth will be approximately equal to the nominal device frequency/1200.

<sup>3</sup> By setting OD low, the outputs are disabled and CLKOUT is held high while  $\overline{\text{CLKOUT}}$  is held low. The threshold for OD is 1.4 V above  $V_{\text{EE}}$ . OD should not be driven above mid supply and during normal operation, should be left floating (use with an open collector or 3-State gate for interfacing with standard logic). If the OD feature is used during normal operation, then CLKIN should be tied through 10k $\Omega$  to GND to avoid any possibility of chatter on the CLKOUT outputs.