surface mount

CMOS COMPATIBLE Wee DIP LOGIC DELAY MODULE

- **CMOS input and outputs**
- **Delays stable and precise**
- **SO-14 pin pattern**
- **Wee DIP package (.235 high)**
- **Available in delays from 20 to 250ns**
- **5 taps—each isolated and with 10 LPST^{2}L fan-out capacity**
- **Fast rise time on all outputs**

design notes

The "Wee DIP Series" Logic Delay Modules developed by Engineered Components Company have been designed to provide precise tapped delays with required driving and pick-off circuitry contained in a single SO-14 surface mount package compatible with CMOS and LPST^{2}L circuits. These logic delay modules are of hybrid construction utilizing the proven technologies of active integrated circuitry and of passive networks utilizing capacitive, inductive and resistive elements. The ICs utilized in these modules are burned-in to level B of MIL-STD-883 to ensure a high MTBF. The MTBF on these modules, when calculated per MIL-HDBK-217 for a 50°C ground fixed environment, is in excess of 3 million hours. Module design includes compensation for propagation delays and incorporates internal termination at the output; no additional external components are needed to obtain the desired delay.

The SMLDM-CMOS is offered in twenty-eight (28) delays from 20ns to 250ns, with each module incorporating taps as shown in the part number table. Delay tolerances are maintained as shown in the accompanying part number table, when tested under the "Test Conditions" shown. Delay time is measured at the +1.5V level on the leading edge. Rise time for all modules is 6ns maximum when measured from 0.75V to 2.4V. Temperature coefficient of delay is approximately ±270 ppm/°C or 3ns, whichever is greater, over the operating temperature range of −40 to +85°C.

These modules accept either logic "1" or logic "0" inputs and reproduce the logic at the selected output tap without inversion. The delay modules are intended primarily for use with positive going pulses and are calibrated to the tolerances shown in the table on rising edge delay; where best accuracy is desired in applications using falling edge timing, it is recommended that a special unit be calibrated for the specific application. Each module output has the capacity of driving up to 2 T^{2}L loads, 10 LPST^{2}L loads or greater than 50 CMOS DC loads.

The "Wee DIP Series" modules are packaged in a SO-14 DIP housing, molded of flame-proof Diallyl Phthalate per MIL-M-14, Type SDG-F, and are fully encapsulated in epoxy resin. Leads meet the solderability requirements of MIL-STD-202, Method 208.

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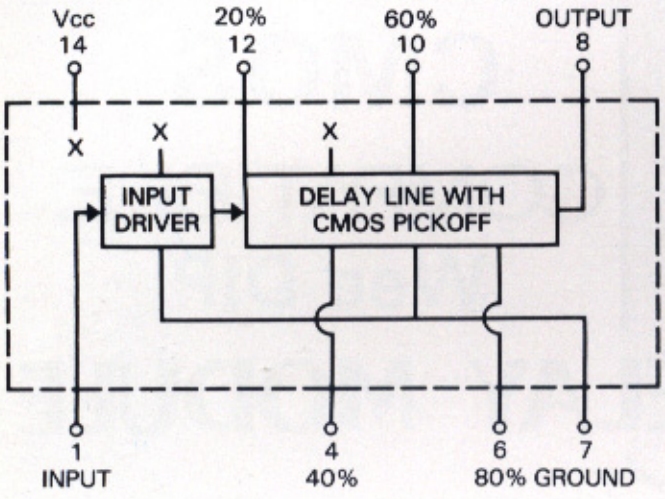
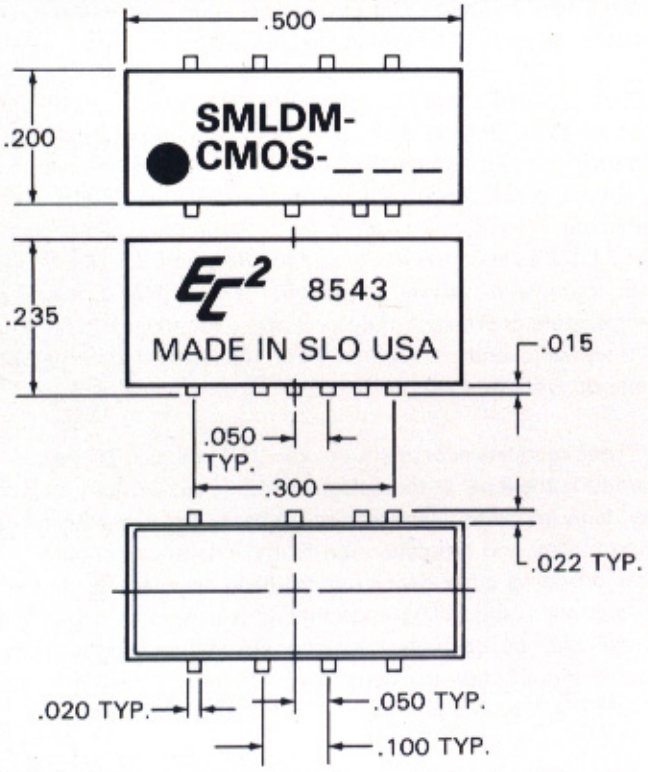
DESIGN NOTES (continued)

Marking consists of manufacturer's logo (EC^2), Federal Supply Code, part number, pin one (1) identification and date code of manufacture. All marking is applied by silk screen process using white epoxy paint in accordance with MIL-STD-130, to meet the permanency of identification required by MIL-STD-202, Method 215.

BLOCK DIAGRAM IS SHOWN BELOW



MECHANICAL DETAIL IS SHOWN BELOW



TEST CONDITIONS

1. All measurements are made at 25°C.
2. V_{CC} supply voltage is maintained at 5.0V DC.
3. All units are tested using a CMOS positive input pulse and one CMOS load at the output being tested.
4. ϕ Input pulse width used is 5 to 10ns longer than full delay of module under test; spacing between pulses (falling edge to rising edge) is three times the pulse width used.

OPERATING SPECIFICATIONS

* V_{CC} supply voltage:	4.5 to 5.5V DC
V_{CC} supply current:	
** Constant "0" in	7 to 13ma typical
Constant "1" in	.1ua typical
Logic 1 input:	
Voltage	2V min.; 5.5V max.
Current	2.4V = 1ua max.
Logic 0 input:	
Voltage	.8V max.
Current	1ua max.
Logic 1 Voltage out:	3.84V min.
Logic 0 Voltage out:	.33V max.
Operating temperature range:	−40 to +85°C.
Storage temperature:	−55 to +125°C.

*Delays decrease or increase approximately 1% or 1ns, whichever is greater, for a respective increase or decrease of 5% in supply voltage.

**7ma typical through SMLDM-CMOS-100, and 13ma typical for parts SMLDM-CMOS-125 and above.

PART NUMBER TABLE

ϕ DELAYS AND TOLERANCES (in ns)					
PART NO.	Tap 1	Tap 2	Tap 3	Tap 4	OUTPUT
SMLDM-CMOS-20	16 ±1	17 ±1	18 ±1	19 ±1	20 ±1
SMLDM-CMOS-22	16 ±1	17.5 ±1	19 ±1	20.5 ±1	22 ±1
SMLDM-CMOS-24	16 ±1	18 ±1	20 ±1	22 ±1	24 ±1
SMLDM-CMOS-26	16 ±1	18.5 ±1	21 ±1	23.5 ±1	26 ±1
SMLDM-CMOS-28	16 ±1	19 ±1	22 ±1	25 ±1	28 ±1
SMLDM-CMOS-32	16 ±1	20 ±1	24 ±1	28 ±1	32 ±1
SMLDM-CMOS-35	15 ±1	20 ±1	25 ±1	30 ±1.5	35 ±1.5
SMLDM-CMOS-39	15 ±1	21 ±1	27 ±1.5	33 ±1.5	39 ±1.5
SMLDM-CMOS-43	15 ±1	22 ±1	29 ±1.5	36 ±1.5	43 ±1.5
SMLDM-CMOS-47	15 ±1	23 ±1	31 ±1.5	39 ±1.5	47 ±1.5
SMLDM-CMOS-51	15 ±1	24 ±1	33 ±1.5	42 ±1.5	51 ±2
SMLDM-CMOS-55	15 ±1	25 ±1	35 ±1.5	45 ±2	55 ±2
SMLDM-CMOS-59	15 ±1	26 ±1	37 ±1.5	48 ±2	59 ±2.5
SMLDM-CMOS-63	15 ±1	27 ±1	39 ±1.5	51 ±2	63 ±2.5
SMLDM-CMOS-67	15 ±1	28 ±1.5	41 ±1.5	54 ±2	67 ±2.5
SMLDM-CMOS-71	15 ±1	29 ±1.5	43 ±1.5	57 ±2	71 ±2.5
SMLDM-CMOS-75	15 ±1	30 ±1.5	45 ±2	60 ±2.5	75 ±2.5
SMLDM-CMOS-80	16 ±1	32 ±1.5	48 ±2	64 ±2.5	80 ±3
SMLDM-CMOS-85	17 ±1	34 ±1.5	51 ±2	68 ±2.5	85 ±3
SMLDM-CMOS-90	18 ±1	36 ±1.5	54 ±2	72 ±2.5	90 ±3
SMLDM-CMOS-95	19 ±1	38 ±1.5	57 ±2	76 ±2.5	95 ±3
SMLDM-CMOS-100	20 ±1	40 ±1.5	60 ±2	80 ±3	100 ±3
SMLDM-CMOS-125	25 ±1	50 ±2	75 ±2.5	100 ±3	125 ±4
SMLDM-CMOS-150	30 ±1.5	60 ±2	90 ±3	120 ±4	150 ±5
SMLDM-CMOS-175	35 ±1.5	70 ±2.5	105 ±4	140 ±5	175 ±5
SMLDM-CMOS-200	40 ±1.5	80 ±3	120 ±4	160 ±5	200 ±6
SMLDM-CMOS-225	45 ±2	90 ±3	135 ±4	180 ±6	225 ±7
SMLDM-CMOS-250	50 ±2	100 ±3	150 ±5	200 ±6	250 ±8

ϕ All modules can be operated with a minimum input pulse width of 40% of full delay and pulse period approaching square wave; since delay accuracies may be somewhat degraded, it is suggested that the module be evaluated under the intended specific operating conditions. Special modules can be readily manufactured to improve accuracies and/or provide customer specified random delay times for specific applications.