N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package			
			TO-3	TO-39	TO-220	Dice†
450V	4Ω	2A	VN0345N1	VN0345N2	VN0345N5	VN0345ND
500V	4Ω	2A	VN0350N1	VN0350N2	VN0350N5	VN0350ND

† MIL visual screening available

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

Features

- ☐ Free from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-channel devices

Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

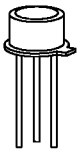
* Distance of 1.6 mm from case for 10 seconds.

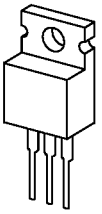
Advanced DMOS Technology

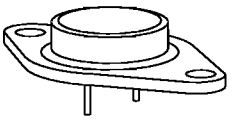
These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options


TO-39


TO-220


TO-3

Note: See package outline section for discrete pinout.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ T_C = 25°C	θ_{ja} °C/W	θ_{jc} °C/W	I_{DR}*	I_{DRM}
TO-3	2.5A	5.0A	100W	30	1.25	2.5A	5.0A
TO-39	0.35A	4.5A	6W	125	20.8	0.35A	4.5A
TO-220	1.5A	5.0A	50W	40	2.5	1.5A	5.0A

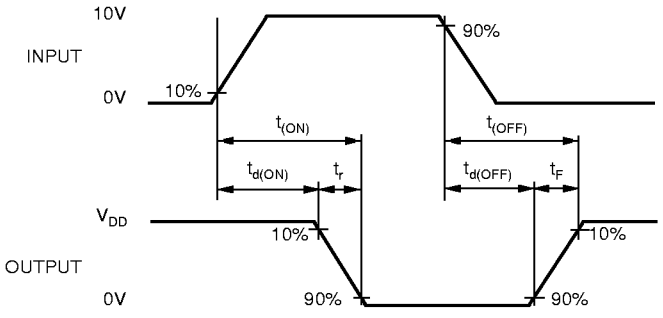
* I_D (continuous) is limited by max rated T_j.

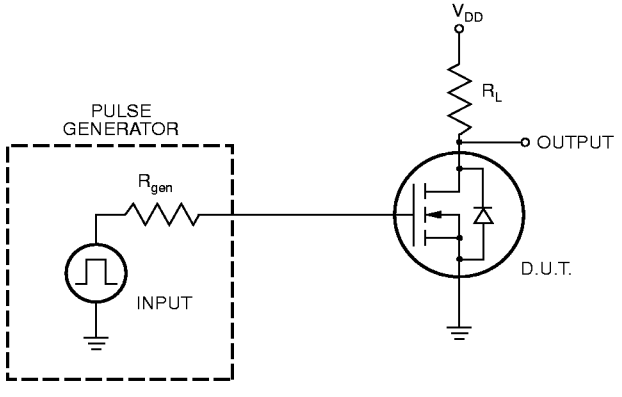
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VN0350	500			V	V_{GS} = 0, I_D = 10mA
		VN0345	450				
$V_{GS(th)}$	Gate Threshold Voltage		2		4	V	V_{GS} = V_{DS}, I_D = 10mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-7.0	-9.0	mV/°C	V_{GS} = V_{DS}, I_D = 10mA
I_{GSS}	Gate Body Leakage				100	nA	V_{GS} = ±20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				100	µA	V_{GS} = 0, V_{DS} = Max Rating
					2.0	mA	V_{GS} = 0, V_{DS} = 0.8 Max Rating, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current			2.6		A	V_{GS} = 5V, V_{DS} = 25V
			2.0	6.5			V_{GS} = 10V, V_{DS} = 25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			3.5		Ω	V_{GS} = 5V, I_D = 0.5A
				2.8	4.0		V_{GS} = 10V, I_D = 0.5A
$\Delta R_{DS(th)}$	Change in $R_{DS(th)}$ with Temperature			1	1.5	%/°C	V_{GS} = 10V, I_D = 0.5A
G_{FS}	Forward Transconductance		500	1000		m℧	V_{DS} = 25V, I_D = 0.5A
C_{ISS}	Input Capacitance			550	650	pF	V_{GS} = 0, V_{DS} = 25V, f = 1 MHz
C_{OSS}	Common Source Output Capacitance			90	125		
C_{RSS}	Reverse Transfer Capacitance			15	50		
$t_{d(ON)}$	Turn-ON Delay Time			8	15	ns	V_{DD} = 25V, I_D = 1A, R_{GEN} = 10Ω
t_r	Rise Time			8	15		
$t_{d(OFF)}$	Turn-OFF Delay Time			65	100		
t_f	Fall Time			15	25		
V_{SD}	Diode Forward Voltage Drop			1.3	1.8	V	V_{GS} = 0, I_{SD} = 1.0A
t_{rr}	Reverse Recovery Time			450		ns	V_{GS} = 0, I_{SD} = 0.5A

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

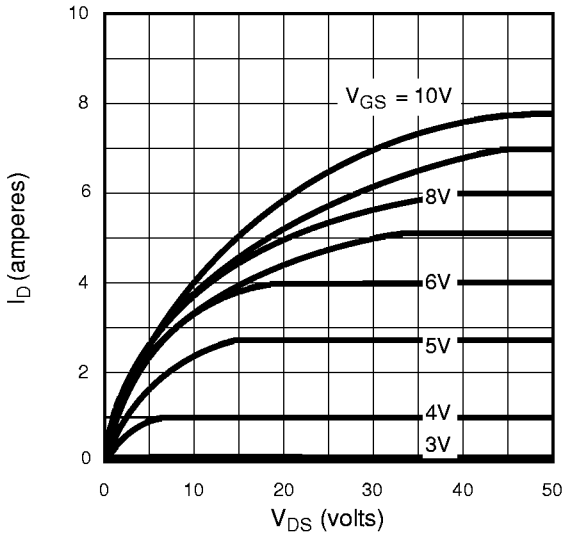
Switching Waveforms and Test Circuit



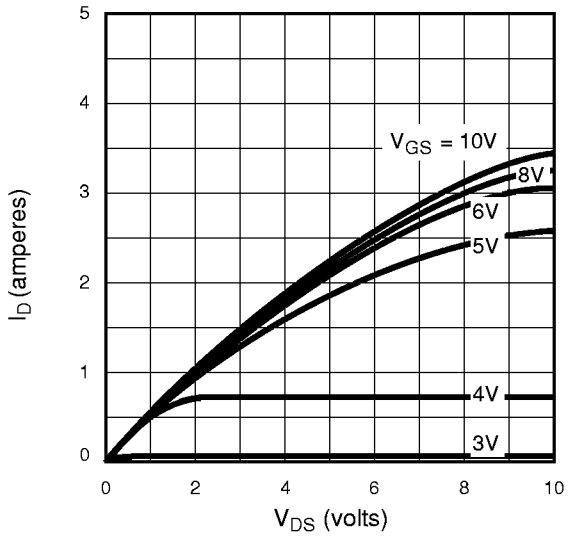


Typical Performance Curves

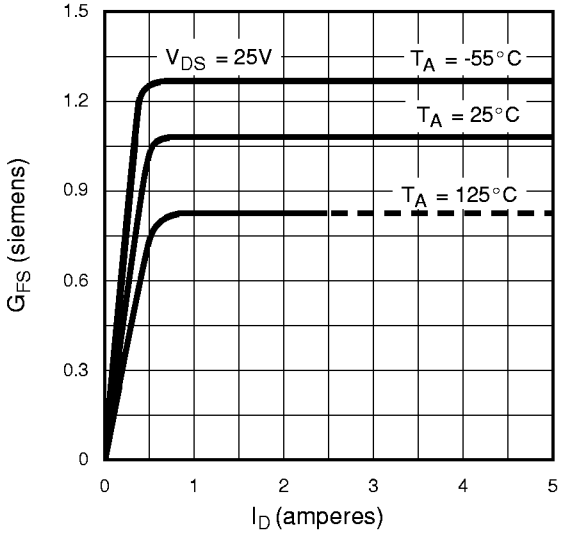
Output Characteristics



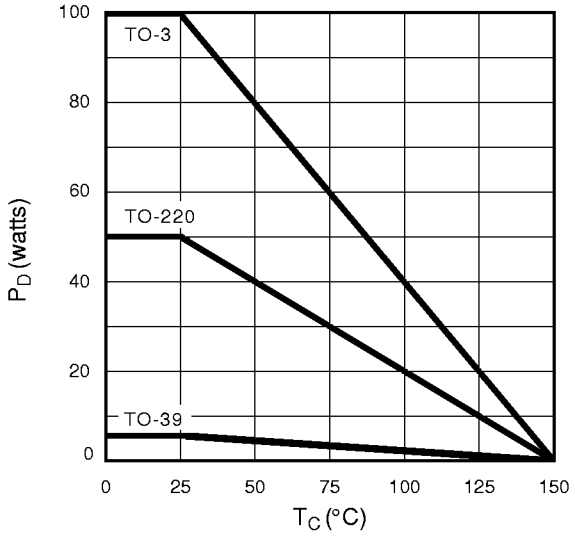
Saturation Characteristics



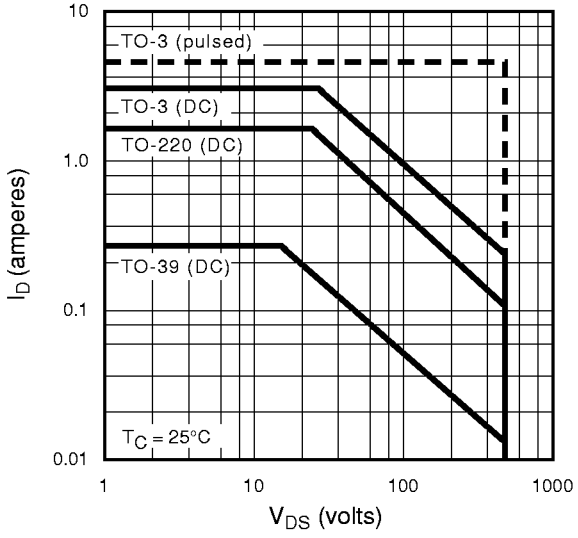
Transconductance vs. Drain Current



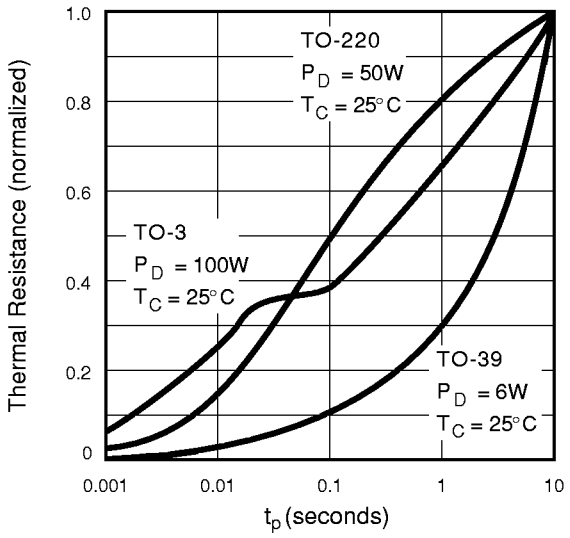
Power Dissipation vs. Case Temperature



Maximum Rated Safe Operating Area

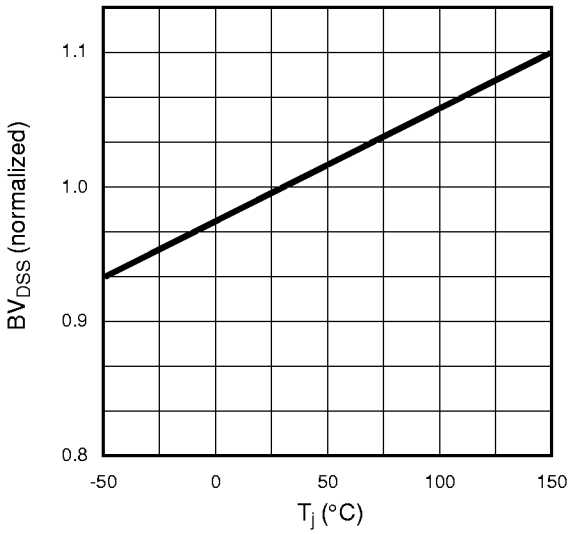


Thermal Response Characteristics

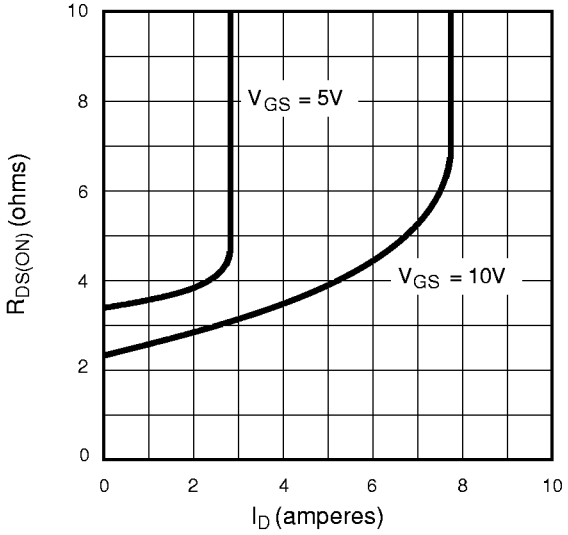


Typical Performance Curves

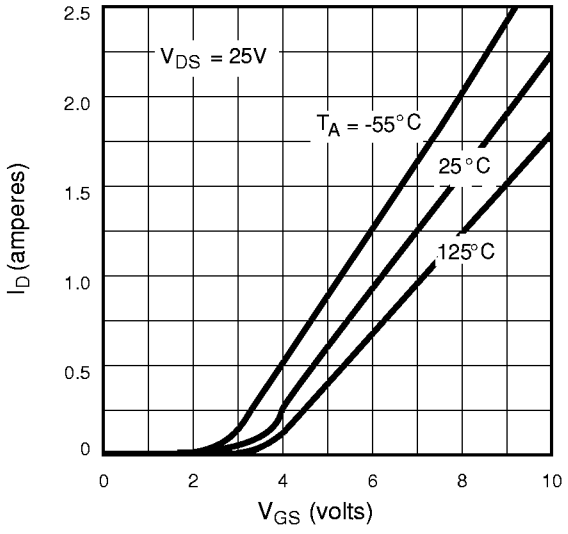
BV_{DSS} Variation with Temperature



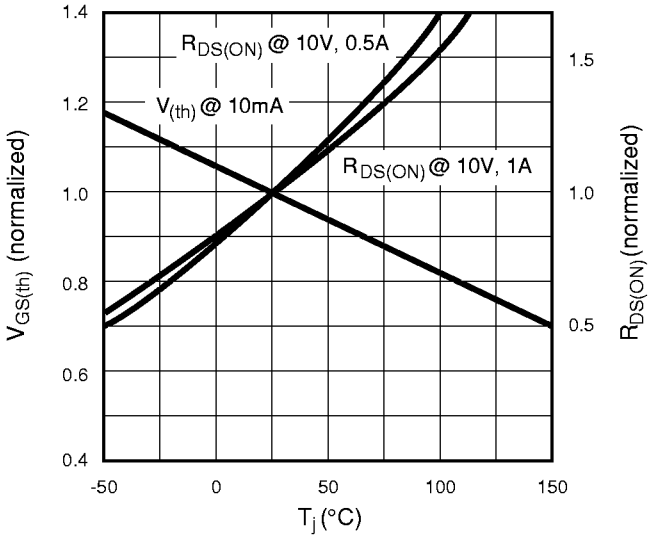
On-Resistance vs. Drain Current



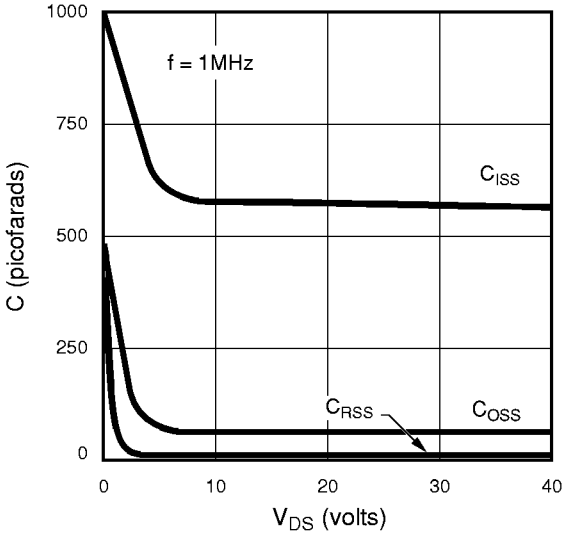
Transfer Characteristics



$V_{(th)}$ and R_{DS} Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics