2M X 32 DRAM DIMM Memory Module

FEATURES

- Performance range:

	t_{RAC}	t_{CAC}	t_{RC}
STI...-60SVG	60ns	20ns	110ns
STI...-70SVG	70ns	20ns	130ns
STI...-80SVG	80ns	20ns	150ns

- Fast Page Mode operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- Self refresh capability
- TTL compatible inputs and outputs
- Single +3.3V ± 10% power supply
- 1024 cycles/128ms refresh
- JEDEC standard pinout
- Gold edge connectors

PIN CONFIGURATION

Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V_{SS}	25	DQ_{12}	49	DQ_{18}
2	DQ_0	26	DQ_{13}	50	DQ_{19}
3	DQ_1	27	DQ_{14}	51	DQ_{20}
4	DQ_2	28	A_7	52	DQ_{21}
5	DQ_3	29	NC	53	DQ_{22}
6	DQ_4	30	V_{CC}	54	DQ_{23}
7	DQ_5	31	A_8	55	NC
8	DQ_6	32	A_9	56	DQ_{24}
9	DQ_7	33	NC	57	DQ_{25}
10	V_{CC}	34	$\overline{RAS}_2$	58	DQ_{26}
11	PD_1	35	DQ_{15}	59	DQ_{28}
12	A_0	36	NC	60	DQ_{27}
13	A_1	37	DQ_{16}	61	V_{CC}
14	A_2	38	DQ_{17}	62	DQ_{29}
15	A_3	39	V_{SS}	63	DQ_{30}
16	A_4	40	$\overline{CAS}_0$	64	DQ_{31}
17	A_5	41	$\overline{CAS}_2$	65	NC
18	A_6	42	$\overline{CAS}_3$	66	PD_2
19	A_{10}	43	$\overline{CAS}_1$	67	PD_3
20	NC	44	$\overline{RAS}_0$	68	PD_4
21	DQ_8	45	NC	69	PD_5
22	DQ_9	46	NC	70	PD_6
23	DQ_{10}	47	$\overline{W}$	71	PD_7
24	DQ_{11}	48	NC	72	V_{SS}

GENERAL DESCRIPTION

The Simple Technology STI322000AD1 is a 2M bits x 32 Dynamic RAM high density memory module. The Simple Technology STI322000AD1 consist of four CMOS 1M x 16 DRAMs in 44-pin TSOP package mounted on a 72-pin glass epoxy substrate. A 0.1µF decoupling capacitor is mounted for each DRAM. A RAS decoder is used to emulate single-bank organization.

The STI322000AD1-xxSVG is a Small Outline Dual In-line Memory Module with self refresh, 3.3 V power supply, and gold edge connections. The STI322000AD1-xxSVG is intended for mounting into 72-pin edge connector sockets.

Pin Names

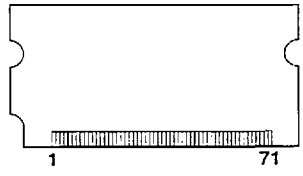
Pin Name	Pin Function
A_0-A_{10}	Address Inputs
DQ_0-DQ_{31}	Data In/Out
$\overline{W}$	Read/Write Input
$\overline{RAS}_0$, $\overline{RAS}_2$	Row Adress Strobe
$\overline{CAS}_0$-$\overline{CAS}_3$	Column Address Strobe
PD_1-PD_7	Presence Detect
V_{CC}	Power (+3.3V)
V_{SS}	Ground
NC	No Connection

Presence Detect Pins

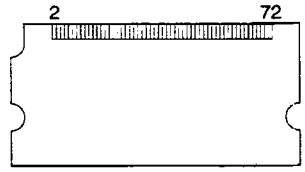
For 2Mx32 Configuration with 1Mx16 Chips:
PD_1=V_{SS}, PD_2=NC, PD_3=V_{SS}, PD_4=NC

Speed			
Pin	**60ns**	**70ns**	**80ns**
PD_5	NC	V_{SS}	NC
PD_6	NC	NC	V_{SS}
Refresh Mode			
Pin	**Self Refresh**		
PD_7	V_{SS}		

Odd numbered pins from pin 1 to pin 71 on front



Even numbered pins from pin 2 to pin 72 on back



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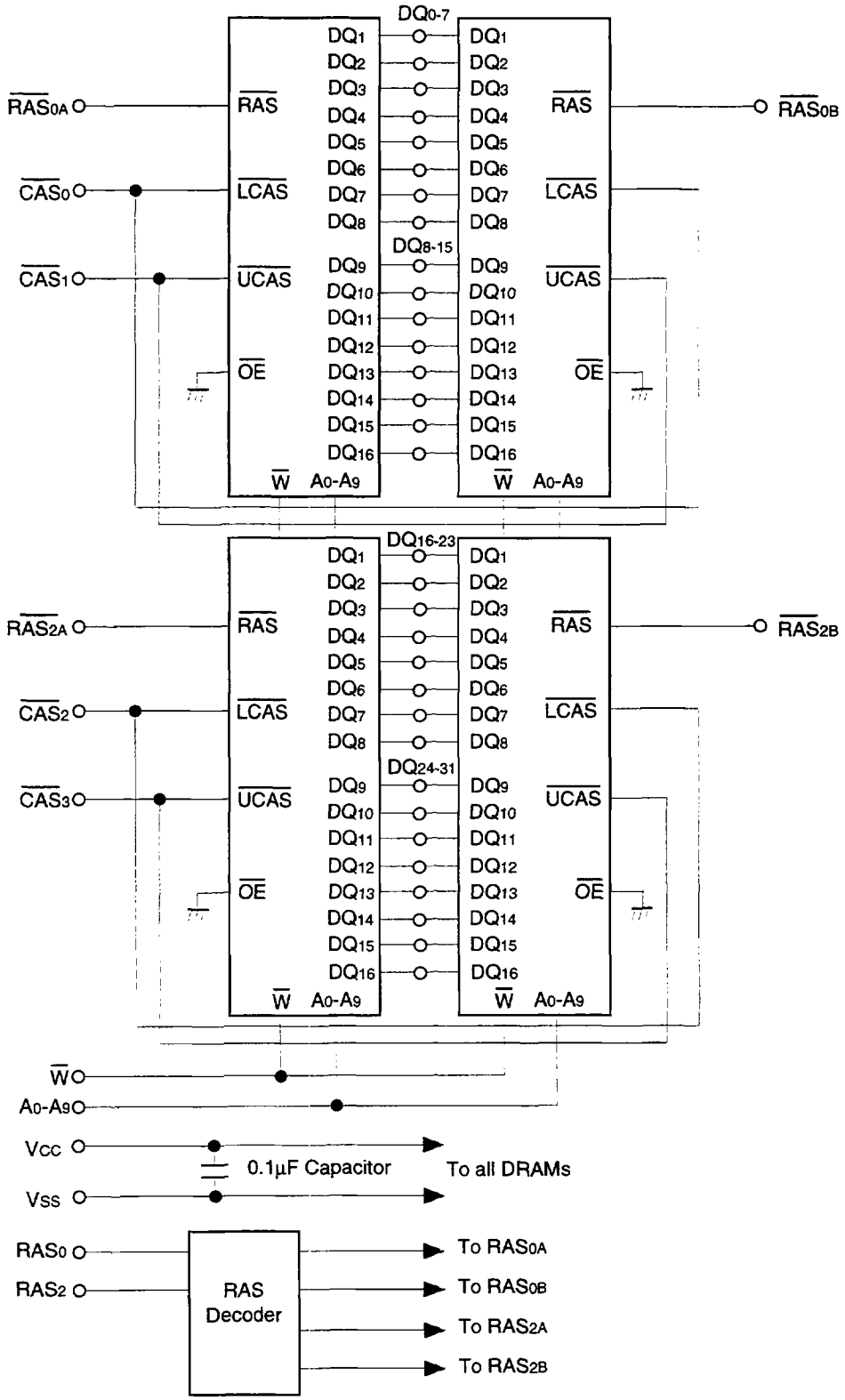
FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to V_{CC}+0.5	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-0.5 to +4.6V	V
Storage Temperature	T_{stg}	-55 to +150	°C
Power Dissipation	P_D	4	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the oprerational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	—	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	-0.3	—	0.8	V

DC AND OPERATION CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @t_{RC}=min.)	STI...-60SVG	I_{CC1}	—	400	mA
	STI...-70SVG		—	360	mA
	STI...-80SVG		—	320	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		I_{CC2}	—	8	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @t_{RC}=min.)	STI...-60SVG	I_{CC3}	—	400	mA
	STI...-70SVG		—	360	mA
	STI...-80SVG		—	320	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Cycling: t_{PC}=min.)	STI...-60SVG	I_{CC4}	—	240	mA
	STI...-70SVG		—	200	mA
	STI...-80SVG		—	160	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)		I_{CC5}	—	800	µA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	STI...-60SVG	I_{CC6}	—	400	mA
	STI...-70SVG		—	360	mA
	STI...-80SVG		—	320	mA
Self Refresh Current ($\overline{RAS}$=$\overline{CAS}$=V_{IL}, DQ_X=W=A_X=V_{CC}-0.2V or 0.2V)		I_{CCS}	—	900	µA
Input Leakage Current (Any input 0≤V_{IN}≤V_{CC}, all other pins not under test=0V)		I_{IL}	-40	40	µA
Output Leakage Current (Data out is disabled, 0≤V_{OUT}≤V_{CC})		I_{OL}	-20	20	µA
Output High Voltage Level (I_{OH}=-2mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL}=2mA)		V_{OL}	—	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC6} are dependent on output loading and cycling rates. Specified values are obtained with the output open. I_{CC} is specified as an average current.

CAPACITANCE (T_A=25 °C)

Item	Symbol	Min	Max	Units
Input Capacitance (A_0-A_{10})	C_{IN1}	—	20	pF
Input Capacitance ($\overline{W}$)	C_{IN2}	—	28	pF
Input Capacitance ($\overline{RAS}_0$, $\overline{RAS}_2$)	C_{IN3}	—	14	pF
Input Capacitance ($\overline{CAS}_0$-$\overline{CAS}_3$)	C_{IN4}	—	7	pF
Input/Output Capacitance ($DQ_{0-7, 8-15, 16-23, 24-31}$)	CDQ_1	—	7	pF

AC CHARACTERISTICS (0 °C≤T_A≤70 °C, V_{CC}=3.3V±10%, See notes 1, 2)

Parameter	Symbol	STI...-60SVG		STI...-70SVG		STI...-80SVG		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3, 4,11
Access time from $\overline{CAS}$	t_{CAC}		20		20		20	ns	3, 4, 5
Access time from column address	t_{AA}		30		35		40	ns	3, 11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		15		ns	
Column address hold referenced to $\overline{RAS}$	t_{AR}	50		55		60		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	15		15		15		ns	
Write command hold referenced to $\overline{RAS}$	t_{WCR}	45		55		60		ns	6
Write command pulse width	t_{WP}	15		15		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		20		20		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10
Data-in hold time	t_{DH}	15		15		15		ns	10
Data-in hold referenced to $\overline{RAS}$	t_{DHR}	50		55		60		ns	6
Refresh period	t_{REF}		128		128		128	ms	

continued on the next page

AC CHARACTERISTICS (continued)

Parameter	Symbol	STI...-60SVG		STI...-70SVG		STI...-80SVG		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ set-up time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CHR}	10		15		15		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40		45	ns	3
Fast Page mode cycle time	t_{PC}	40		45		50		ns	
$\overline{CAS}$ precharge time (fast page)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ pulse width (fast page)	t_{RASP}	60	100,000	70	100,000	80	100,000	ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRP}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRH}	10		10		10		ns	
$\overline{CAS}$ precharge ($\overline{C}$-B-$\overline{R}$ counter test)	t_{CPT}	20		30		30		ns	
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	t_{CHS}	-50		-50		-50		ns	12
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	t_{RPS}	110		130		150		ns	12
$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ self refresh)	t_{RASS}	100		100		100		µs	12

NOTES

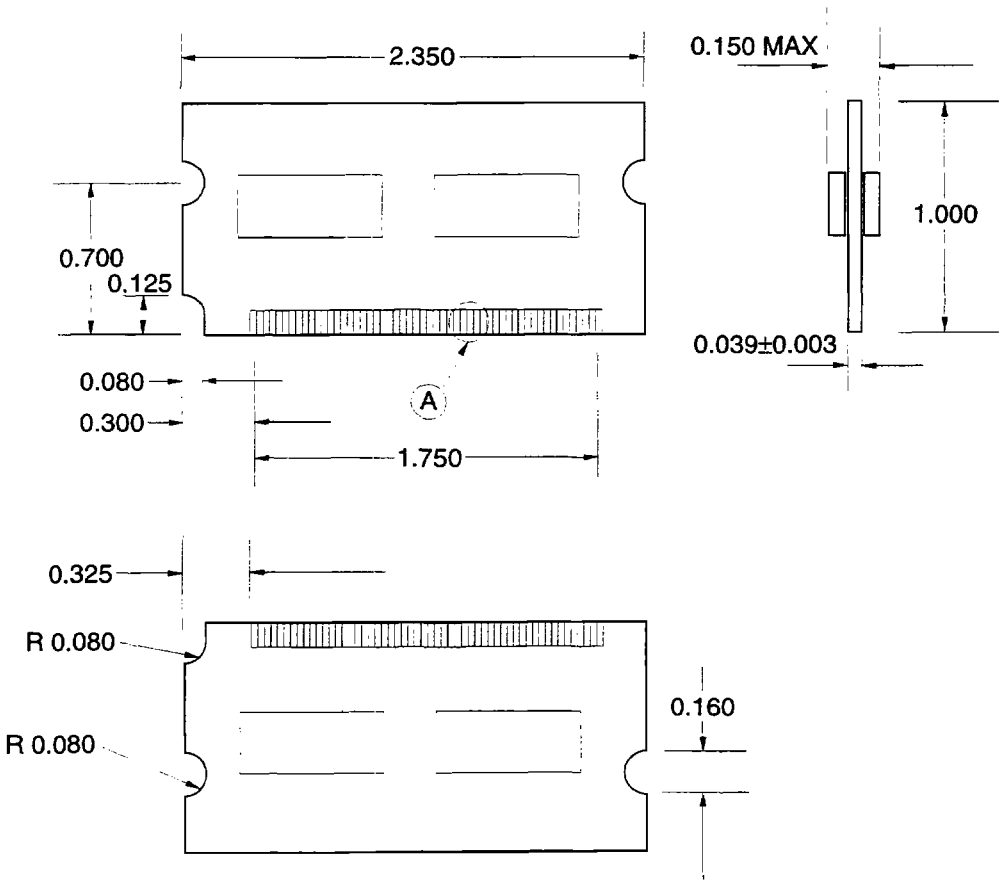
1. An initial pause of 200 µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$, and are assumed to be 5ns for all inputs.
3. Measure with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$.
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are non-restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.
12. 1024 cycle of Burst Refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.

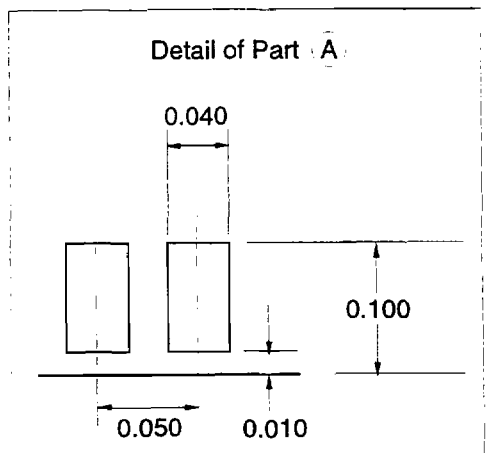
TIMING DIAGRAMS

Please refer to attached Timing Charts I and VI.

PACKAGE DIMENSIONS

Units: Inches





10 millionths minimum gold for DIMMs ordered with gold lead option.

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TOLERANCES: ±0.005 UNLESS OTHERWISE SPECIFIED