MOTOROLA
■ **SEMICONDUCTOR** ■
TECHNICAL DATA

ADVANCE INFORMATION

DUAL SINGLE SUPPLY COMPARATORS

The LMT393 family of comparators are dual, independent voltage comparators capable of single or split-supply operation. These devices are designed to permit a common mode range-to-ground level with single-supply operation. Input offset voltage specifications as low as 5.0 mV make this device an excellent selection for many applications in consumer automotive, and industrial electronics.

* Wide Single-Supply Range — 2.0 Vdc to 36 Vdc
* Split-Supply Range — ±1.0 Vdc to ±18 Vdc
* Very Low Current Drain Independent of Supply Voltage — 0.4 mA
* Low Input Bias Current — 25 nA (Typ)
* Low Input Offset Current — ±5.0 nA (Typ)
* Low Input Offset Voltage — ±5.0 mV (Max)
* Input Common-Mode Voltage Range to Ground
* Differential Input Voltage Range Equal to Power Supply Voltage
* Output Voltage Compatible with DTL, ECL, TTL, MOS and CMOS Logic Levels

MAXIMUM RATINGS (TA = 25°C Unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltages Single Supply Split Supplies	V_{CC} V_{CC}, V_{EE}	36 ±18	Vdc
Input Differential Voltage Range	V_{IDR}	±36	Vdc
Input Common Mode Voltage Range	V_{ICR}	-0.3 to Vcc	Vdc
Output Short Circuit Duration	t_S	Continuous	Sec
Output Sink Current	I_{SINK}	20	mA
Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C
Power Dissipation, Plastic DIP	P_D	500	mW

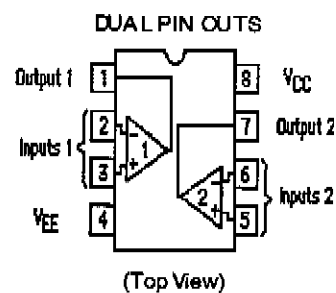| ORDERING INFORMATION		
Device	Package	Temperature Range
LMT393N LMT393D	8 Pin Plastic DIP SO-8	0°C to 70°C
LMT2903N LMT2903D	8 Pin Plastic DIP SO-8	-40°C to 105°C

LMT393, LMT2903

DUAL COMPARATORS

SILICON MONOLITHIC
INTEGRATED CIRCUIT

N SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC PACKAGE
CASE 751-02
SO-8

DUAL PINOUTS

(Top View)

CAUTION: These devices do not have internal ESD protection circuitry and are rated as CLASS 1 devices per the ESD test method in Mil-Std-833 D. They should be handled using standard ESD prevention methods to avoid damage to the device.

MacRev 3.0

ELECTRICAL CHARACTERISTICS   (V_{CC}= +5.0Vdc; *$T_{low} \leq T_A \leq T_{high}$ unless otherwise noted)

CHARACTERISTICS	SYMBOL	LMT393			LMT2903			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage (1)	V_{IO}							mV
T_A = +25°C		—	±2.0	±5.0	—	±2.0	±7.0	
$T_{low} \leq T_A \leq T_{high}$		—	—	9.0	—	—	15	
Input Offset Current	I_{IO}							nA
T_A = 25°C		—	±5.0	±50	—	±5.0	±50	
$T_{low} \leq T_A \leq T_{high}$		—	—	±150	—	±50	±200	
Input Bias Current (2)	I_{IB}							nA
T_A = 25°C		—	25	250	—	25	250	
$T_{low} \leq T_A \leq T_{high}$		—	—	400	—	200	500	
Input Common-Mode Voltage Range (2)	V_{ICR}							Volts
T_A = 25°C		0	—	[V_{CC}]-1.5	0	—	[V_{CC}]-1.5	
$T_{low} \leq T_A \leq T_{high}$		0	—	-2.0	0	—	-2.0	
Voltage Gain $R_L \geq 15$ kΩ, V_{CC} = 15 Vdc T_A = 25°C	A_{VOL}	50	200	—	25	200	—	V/mV
Large Signal Response Time V_{in} = TTL Logic Swing, V_{ref} = 1.4 Vdc V_{RL} =5.0 Vdc, R_L 5.1 kΩ, T_A = 25°C	—	—	300	—	—	300	—	ns
Response Time (3) V_{RL} = 5.0 Vdc, R_L 5.1 kΩ, T_A = 25°C	t_{TLH}	—	1.3	—	—	1.5	—	μs
Input Differencial Range (4) All $V_{in} \geq$ Gnd or V - Supply (if used)	V_{ID}	—	—	V_{CC}	—	—	V_{CC}	V
Output Sink Current $V_{in-} \geq 1.0$ Vdc, V_{in+} = 0 Vdc, $V_O \leq 1.5$ Vdc T_A = 25°C	I_{sink}	6.0	16	—	6.0	16	—	mA
Output Saturation Voltage $V_{in-} \geq 1.0$Vdc, V_{in+} = 0 , $I_{sink} \leq 4.0$ mA, T_A = 25°C	V_{OL}	—	200	400	—	200	400	mV
$T_{low} \leq T_A \leq T_{high}$		—	—	700	—	—	700	
Output Leakage Current V_{in-} = 0 V, $V_{in+} \geq 1.0$ Vdc, V_O = 5.0 Vdc, T_A = 25°C	I_{OL}	—	0.1	—	—	0.1	—	nA
V_{in-} = 0 V, $V_{in+} \geq 1.0$ Vdc, V_O = 30 Vdc, $T_{low} \leq T_A \leq T_{high}$		—	—	1000	—	—	1000	
Supply Current $R_L = \infty$ Both Comparators T_A = 25°C	I_{CC}	—	0.8	1.0	—	0.8	1.0	mA
$R_L = \infty$ Both Camparators, V_{CC} = 30 V		—	—	2.5	—	—	2.5	

* LMT393 — T_{LOW} = 0°C, T_{HIGH} = +70°C   LMT2903 — T_{LOW} = -40°C, T_{HIGH} = +105°C

NOTES:
1. At output switch point, $V_O \approx 1.4$ Vdc, R_S =0Ω with V_{CC} from 5.0 Vdc to 30 Vdc, and over the full input common-mode range (0 volts to V_{CC} = -1.5 volts)
2. Due to the PNP transistor inputs, bias current will flow out of the inputs, this current is essentially constant independant of the output state, therefore, no loading changes will exist on the input lines.
3. Response time is specified with a 100 mV step and 5.0 mV of overdrive. With larger magnitudes of overdrive faster response times are obtained.
4. The comparator will exhibit proper output state if one of the inputs become greater than V_{CC}, the outer input must remain within the common mode range. The low input state must not be less than -0.3 volts of ground or minus supply.

This data sheet contains preliminary information and design objectives. All specifications are subject to change without notice.