IS61NW6432

64K x 32 SYNCHRONOUS STATIC RAM WITH NO-WAIT STATE BUS FEATURE

ADVANCE INFORMATION
JULY 1998

FEATURES

- Fast access time:
  – 5 ns-100 MHz; 6 ns-83 MHz;
  – 7 ns-75 MHz; 8 ns-66 MHz
- No wait cycles between Read and Write
- Internal self-timed write cycle
- Individual Byte Write Control
- Clock controlled, registered address, data and control
- Pentium™ or linear burst sequence control using MODE input
- Three chip enables for simple depth expansion and address pipelining
- Common data inputs and data outputs
- JEDEC 100-pin TQFP and PQFP package
- Single +3.3V power supply
- Optional data strobe pin (#80) for latching data (See page 12 for detailed timing)

DESCRIPTION

The IS61NW6432 is a high-speed, low-power synchronous static RAM designed to provide a burstable, high-performance, 'no-wait' bus, secondary cache for the Pentium, 680X0, and Power PC microprocessors. It is organized as 65,536 words by 32 bits, fabricated with *ISSI*'s advanced CMOS technology.

Incorporating a 'no-wait' bus, wait cycles are eliminated when the bus switches from read to write, or write to read. This device integrates a 2-bit burst counter, high-speed SRAM core, and high-drive capability outputs into a single monolithic circuit.

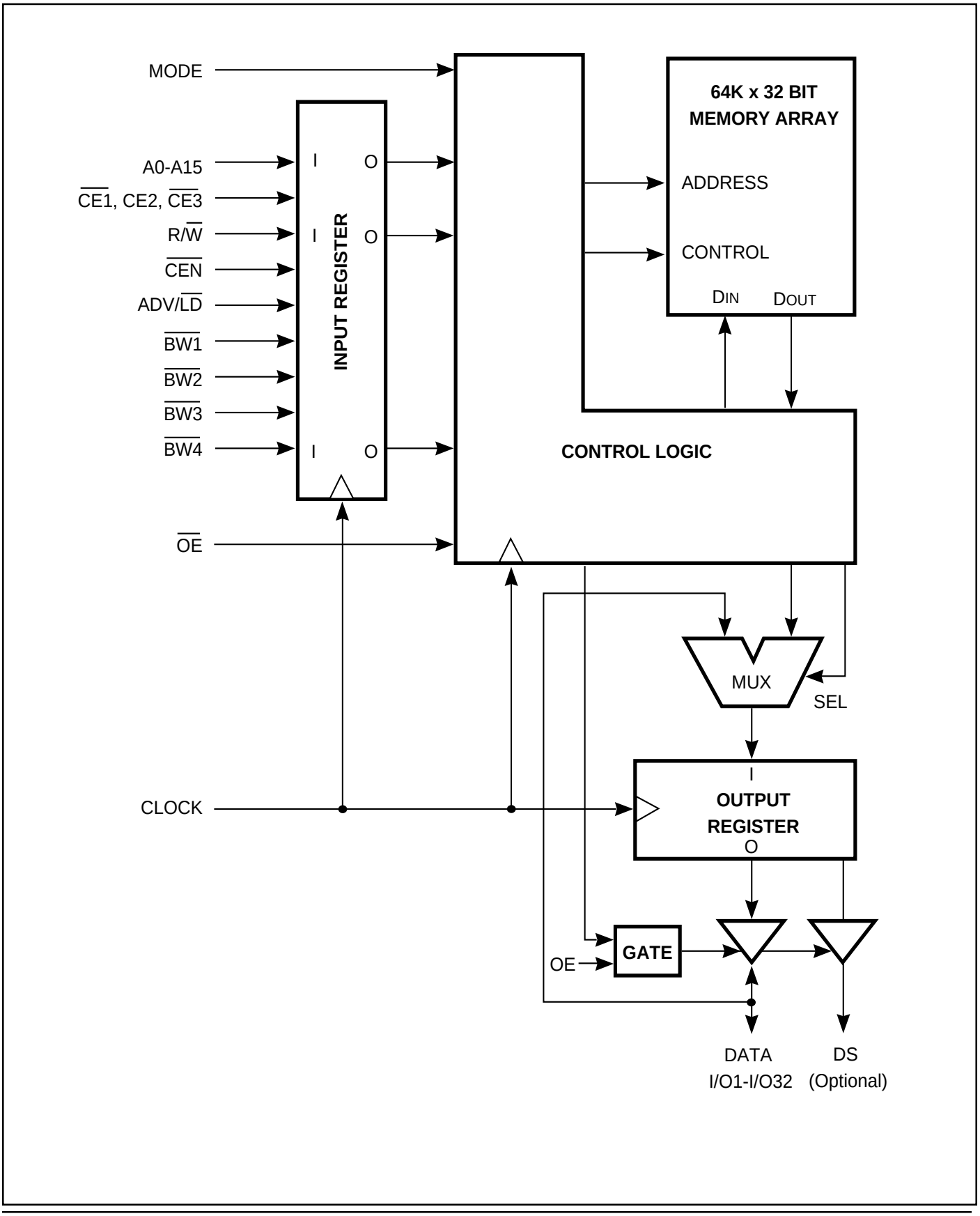
All synchronous inputs pass through registers controlled by a positive-edge-triggered clock input. Operations may be suspended and all synchronous inputs ignored when Clock Enable, $\overline{CEN}$ is HIGH. In this state the internal device will hold their previous values.

When the ADV/$\overline{LD}$ is HIGH the internal burst counter is incremented. New external addresses can be loaded when ADV/$\overline{LD}$ is LOW.

Write cycles are internally self-timed and are initiated by the rising edge of the clock inputs and when RD/$\overline{WE}$ is LOW. Separate byte enables allow individual bytes to be written. $\overline{BW1}$ controls I/O1-I/O8; $\overline{BW2}$ controls I/O9-I/O16; $\overline{BW3}$ controls I/O17-I/O24; $\overline{BW4}$ controls I/O25-I/O32. All Bytes are written when $\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, and $\overline{BW4}$ are LOW.

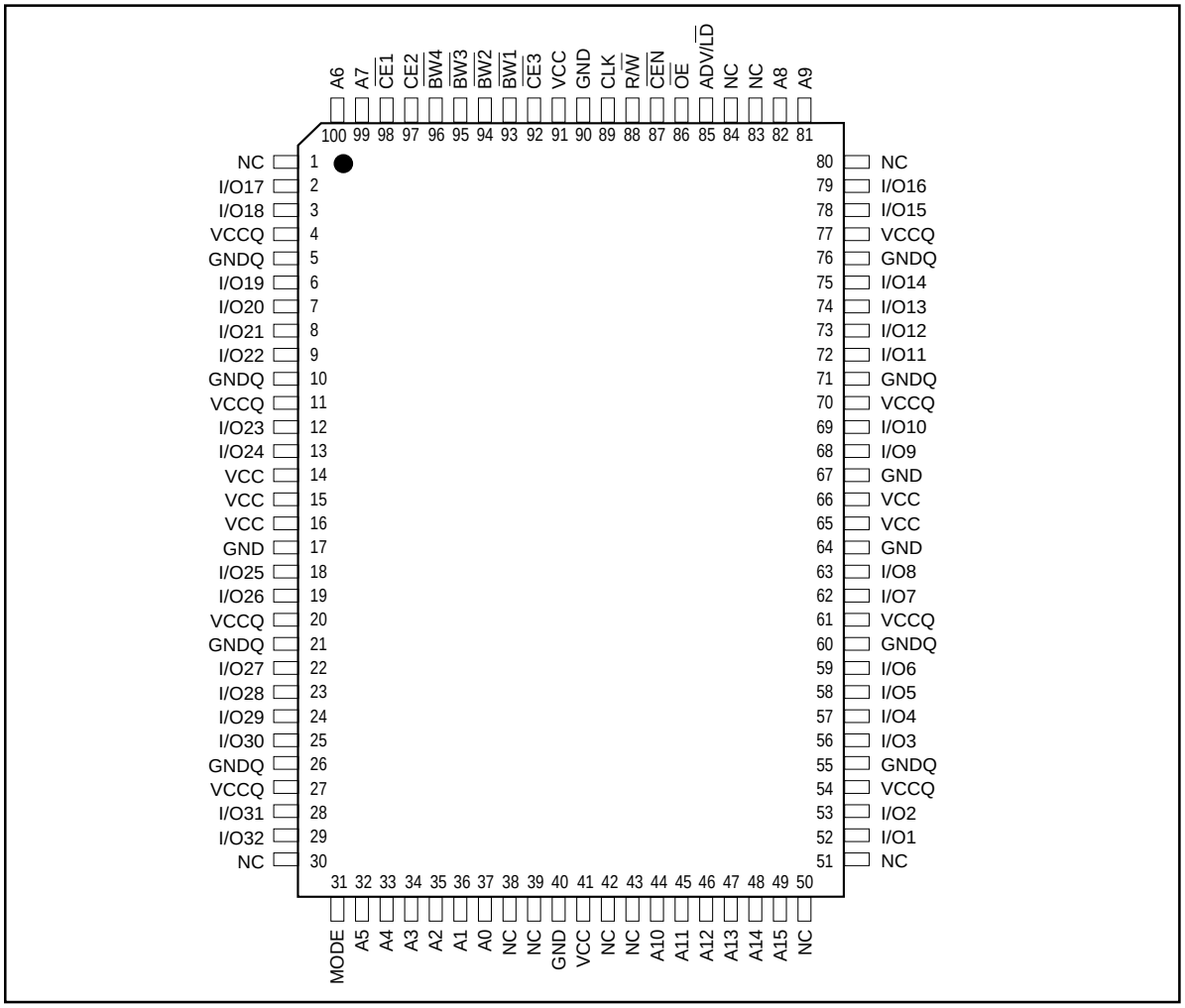
MODE pin upon power up is in interleave burst mode. It can be connected to GNDQ or VCCQ to alter power up state.

BLOCK DIAGRAM



PIN CONFIGURATION

100-Pin TQFP and PQFP (Top View)



PIN DESCRIPTIONS

A0-A15	Address Inputs
CLK	Clock
$\overline{CEN}$	Clock Enable
ADV/$\overline{CD}$	Advance Load
$\overline{BW1}$-$\overline{BW4}$	Synchronous Byte Write Enable
R/$\overline{W}$	Read/Write
$\overline{CE1}$, CE2, $\overline{CE3}$	Synchronous Chip Enable
$\overline{OE}$	Output Enable

DS(1)	Data Strobe
I/O1-I/O32	Data Input/Output
MODE	Burst Sequence Mode
V_{CC}	+3.3V Power Supply
GND	Ground
V_{CCQ}	Isolated Output Buffer Supply: +3.3V
GND_Q	Isolated Output Buffer Ground
NC	No Connect

Note:
1. Optional, NC or DS.

TRUTH TABLE[1]

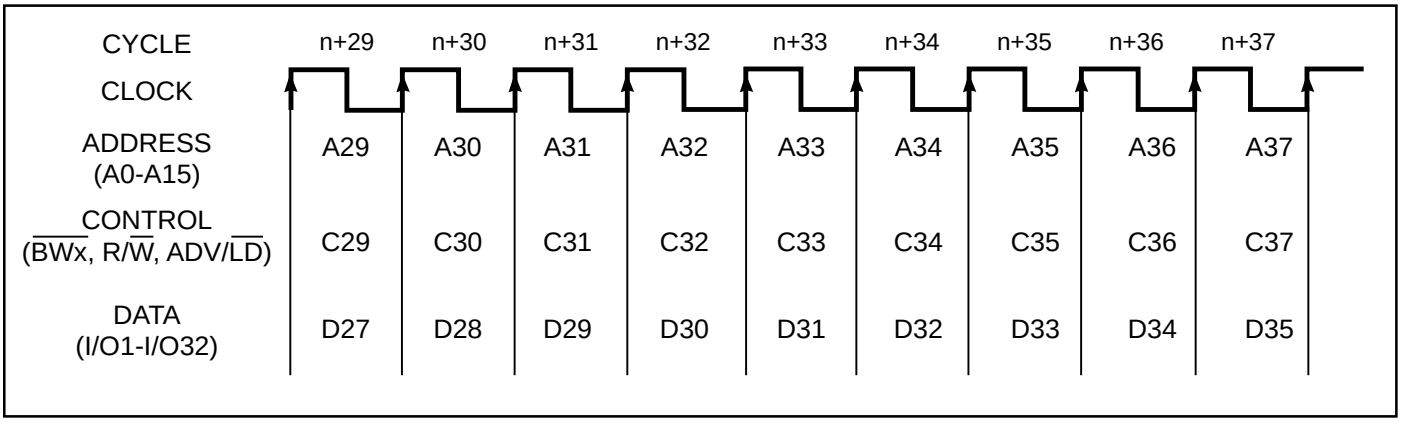
Operation	Address Used	R/$\overline{W}$	$\overline{CEx}$	ADV/$\overline{LD}$	$\overline{CEN}$	$\overline{BWx}$	CLK
Begin New Write Cycle	External	L	L	L	L	Valid	L-H
Begin New Read Cycle	External	H	L	L	L	X	L-H
Advance Burst Counter[2] (Burst Write)	Internal	X	X	H	L	Valid	L-H
Advance Burst Counter (Burst Read)	Internal	X	X	H	L	X	L-H
Deselect (2 Cycle)[3]	X	X	H	L	L	X	L-H
Hold/NOOP[4]	X	X	X	X	H	X	L-H

Notes:
1. "X" Means don't care.
2. When ADV/$\overline{LD}$ signal is sampled HIGH, the internal burst counter is incremented. The R/$\overline{W}$ signal is ignored when the counter is advanced. Therefore, the nature of the burst cycle (Read or Write) is determined by the status of the R/$\overline{W}$ signal when the first address is loaded at the beginning of the burst cycle.
3. Deselect cycle is initiated when $\overline{CEx}$ is sampled HIGH and ADV/$\overline{LD}$ sampled LOW at rising edge of clock. The data bus will tri-state two cycles after deselect is initiated.
4. When $\overline{CEN}$ is sampled high at the rising edge of clock, that clock edge is blocked from propogating through the part. The state of all the internal registers remains unchanged.

PARTIAL TRUTH TABLE (Non-burst)

Function	R/$\overline{W}$	$\overline{BW1}$	$\overline{BW2}$	$\overline{BW3}$	$\overline{BW4}$	$\overline{CEx}$	ADV/$\overline{LD}$
Read	H	X	X	X	X	L	L
Write Byte 1	L	L	H	H	H	L	L
Write Byte 2	L	H	L	H	H	L	L
Write Byte 3	L	H	H	L	H	L	L
Write Byte 4	L	H	H	H	L	L	L
Write All Bytes	L	L	L	L	L	L	L

FUNCTIONAL TIMING DIAGRAM



TYPICAL OPERATION ($\overline{CE1}$, $\overline{CE3}$ and $\overline{CEN}$ are LOW, CE2 is HIGH, Non-Burst Operation)

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CEx}$	$\overline{CEN}$	$\overline{BWx}$	$\overline{OE}$	I/O	Comments
n	A0	H	L	L	L	X	?	D–2	?
n+1	A1	L	L	L	L	L	?	D–1	?
n+2	A2	H	L	L	L	X	L	D0	Data Out
n+3	A3	L	L	L	L	L	X	D1	Data In
n+4	A4	H	L	L	L	X	L	D2	Data Out
n+5	A5	L	L	L	L	L	X	D3	Data In
n+6	A6	H	L	L	L	X	L	D4	Data Out
n+7	A7	L	L	L	L	L	X	D5	Data In
n+8	A8	H	L	L	L	X	L	D6	Data Out
n+9	A9	L	L	L	L	L	X	D7	Data In
n+10	A10	H	L	L	L	X	L	D8	Data Out
n+11	A11	H	L	L	L	X	X	D9	Data In
n+12	A12	L	L	L	L	L	L	D10	Data Out
n+13	A13	L	L	L	L	L	L	D11	Data Out
n+14	A14	H	L	L	L	X	X	D12	Data In
n+15	A15	H	L	L	L	X	X	D13	Data In
n+16	A16	H	L	L	L	X	L	D14	Data Out
n+17	A17	L	L	L	L	L	L	D15	Data Out
n+18	A18	L	L	L	L	L	L	D16	Data Out
n+19	A19	L	L	L	L	L	X	D17	Data In
n+20	A20	H	L	L	L	X	X	D18	Data In
n+21	A21	H	L	L	L	X	X	D19	Data In

Note:
1. H = High; L = Low; X = Don't Care; ? = Don't Know; Z = High Impedance

READ OPERATION

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CEx}$	$\overline{CEN}$	$\overline{BWx}$	$\overline{OE}$	I/O	Comments
n	A0	H	L	L	L	X	X	X	Address and Control meet setup
n+1	X	X	X	L	L	X	X	X	Clock Setup Valid
n+2	X	X	X	X	X	X	L	D0	Contents of Address A0 Read Out

BURST READ OPERATION

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CEx}$	$\overline{CEN}$	$\overline{BWx}$	$\overline{OE}$	I/O	Comments
n	A0	H	L	L	L	X	X	X	Address and Control meet setup
n+1	X	X	H	X	L	X	X	X	Clock Setup Valid, Advance Counter
n+2	X	X	H	X	L	X	L	D0	Address A0 Read Out, Inc. Count
n+3	X	X	H	X	L	X	L	D0+1	Address A0+1 Read Out, Inc. Count
n+4	X	X	H	X	L	X	L	D0+2	Address A0+2 Read Out, Inc. Count
n+5	A1	H	L	L	L	X	L	D0+3	Address A0+3 Read Out, Load A1
n+6	X	X	H	X	L	X	L	D0	Address A0 Read Out, Inc. Count
n+7	X	X	H	X	L	X	L	D1	Address A1 Read Out, Inc. Count
n+8	A2	H	L	L	L	X	L	D1+1	Address A1+1 Read Out, Load A2

WRITE OPERATION

Cycle	Address	R/$\overline{W}$	ADV/LD	$\overline{CEx}$	$\overline{CEN}$	$\overline{BWx}$	$\overline{OE}$	I/O	Comments
n	A0	L	L	L	L	L	X	X	Address and Control meet setup
n+1	X	X	X	L	L	X	X	X	Clock Setup Valid
n+2	X	X	X	X	L	X	X	D0	Write D0 to Address A0

BURST WRITE OPERATION

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CEx}$	$\overline{CEN}$	$\overline{BWx}$	$\overline{OE}$	I/O	Comments
n	A0	L	L	L	L	L	X	X	Address and Control meet setup
n+1	X	X	H	X	L	L	X	X	Clock Setup Valid, Inc. Count
n+2	X	X	H	X	L	L	X	D0	Address A0 Write, Inc. Count
n+3	X	H	H	L	L	X	X	D0+1	Address A0+1 Write, Inc. Count
n+4	X	X	H	X	L	L	X	D0+2	Address A0+2 Write, Inc. Count
n+5	A1	L	L	L	L	L	X	D0+3	Address A0+3 Write, Load A1
n+6	X	X	H	X	L	L	X	D0	Address A0 Write, Inc. Count
n+7	X	X	H	X	L	L	X	D1	Address A1 Write, Inc. Count
n+8	A2	L	L	L	L	L	X	D1+1	Address A1+1 Write, Load A2

Note:
1. H = High; L = Low; X = Don't Care; ? = Don't Know; Z = High Impedance

READ OPERATION WITH CLOCK ENABLE USED

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CEx}$	$\overline{CEN}$	$\overline{BWx}$	$\overline{OE}$	I/O	Comments
n	A0	H	L	L	L	X	X	X	Address and Control meet setup
n+1	X	X	X	X	H	X	X	X	Clock n+1 Ignored
n+2	A1	H	L	L	L	X	X	X	Clock Valid
n+3	X	X	X	X	H	X	L	D0	Clock Ignored. Data D0 is on the bus
n+4	X	X	X	X	H	X	L	D0	Clock Ignored. Data D0 is on the bus
n+5	A2	H	L	L	L	X	L	D0	Address A0 Read Out (bus trans.)
n+6	A3	?	L	L	L	X	L	D1	Address A1 Read Out (bus trans.)
n+7	A4	?	L	L	L	X	L	D2	Address A2 Read Out (bus trans.)

WRITE OPERATION WITH CLOCK ENABLE USED

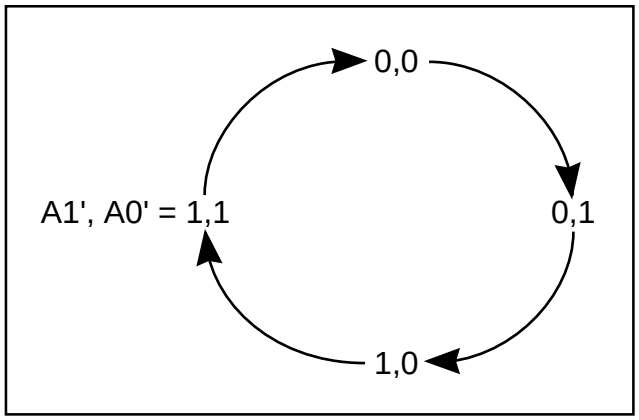
Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CEx}$	$\overline{CEN}$	$\overline{BWx}$	$\overline{OE}$	I/O	Comments
n	A0	L	L	L	L	L	X	X	Address and Control meet setup
n+1	X	X	X	X	H	X	X	X	Clock n+1 Ignored
n+2	A1	L	L	L	L	L	X	X	Clock Valid
n+3	X	X	X	X	H	X	L	di	Clock Ignored.
n+4	X	X	X	X	H	X	L	di	Clock Ignored.
n+5	A2	L	L	L	L	L	L	D0	Write data D0 (bus trans.)
n+6	A3	?	L	L	L	L	L	D1	Write data D1 (bus trans.)
n+7	A4	?	L	L	L	L	L	D2	Write data D2 (bus trans.)

Note:
1. H = High; L = Low; X = Don't Care; ? = Don't Know; Z = High Impedance; di could be D0 if desired.

INTERLEAVED BURST ADDRESS TABLE (MODE = V_{CCQ} or No Connect)

External Address A1 A0	1st Burst Address A1 A0	2nd Burst Address A1 A0	3rd Burst Address A1 A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

LINEAR BURST ADDRESS TABLE (MODE = GND_Q)



ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
T_{BIAS}	Temperature Under Bias	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +150	°C
P_D	Power Dissipation	1.8	W
I_{OUT}	Output Current (per I/O)	100	mA
V_{IN}, V_{OUT}	Voltage Relative to GND for I/O Pins	–0.5 to V_{CCQ} + 0.3	V
V_{IN}	Voltage Relative to GND for for Address and Control Inputs	–0.5 to 5.5	V

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. This device contains circuity to protect the inputs against damage due to high static voltages or electric fields; however, precautions may be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.
3. This device contains circuitry that will ensure the output devices are in High-Z at power up.

OPERATING RANGE

Range	Ambient Temperature	Vcc
Commercial	0°C to +70°C	3.3V +10%, –5%

DC ELECTRICAL CHARACTERISTICS(1) (Over Operating Range)

Symbol	Parameter	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –5.0 mA		2.4	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 5.0 mA		—	0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CCQ} + 0.3	V
V_{IL}	Input LOW Voltage			–0.3	0.8	V
I_{LI}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CCQ}(2)	Com.	–5	5	µA
I_{LO}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CCQ}, $\overline{OE}$ = V_{IH}	Com.	–5	5	µA

POWER SUPPLY CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions		-5 Min.	-5 Max.	-6 Min.	-6 Max.	-7 Min.	-7 Max.	-8 Min.	-8 Max.	Unit
I_{CC}	AC Operating Supply Current	Device Selected, All Inputs = V_{IL} or V_{IH} $\overline{OE}$ = V_{IH}, Cycle Time ≥ t_{KC} min.	Com.	—	230	—	220	—	210	—	200	mA
I_{SB}	Standby Current	Device Deselected, V_{CC} = Max., All Inputs = V_{IH} or V_{IL} CLK Cycle Time ≥ t_{KC} min., $\overline{CEN}$ = V_{IH}	Com.	—	60	—	60	—	60	—	60	mA

Notes:
1. MODE pin has an internal pull up. This pin may be a No Connect, tied to GND, or tied to V_{CCQ}.
2. MODE pin should be tied to Vcc or GND. It exhibits ±30 µA maximum leakage current when tied to ≤ GND + 0.2V or ≥ Vcc – 0.2V.

CAPACITANCE[1,2]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Input/Output Capacitance	V_{OUT} = 0V	8	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, Vcc = 3.3V.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	1.5 ns
Input and Output Timing and Reference Level	1.5V
Output Load	See Figures 1 and 2

AC TEST LOADS

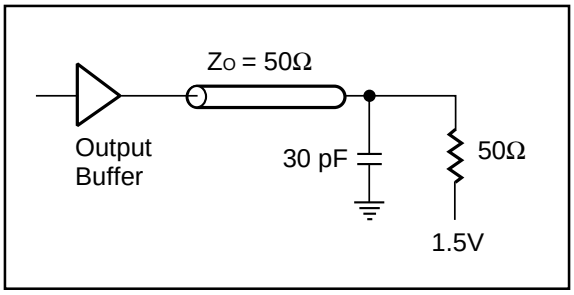


Figure 1

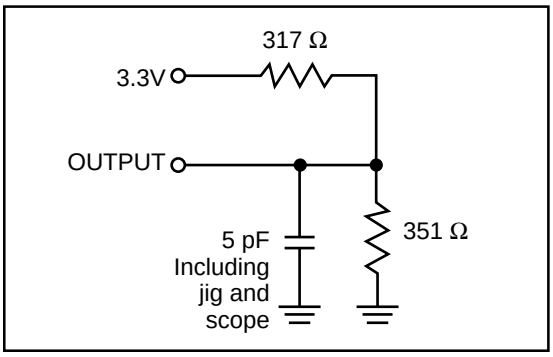


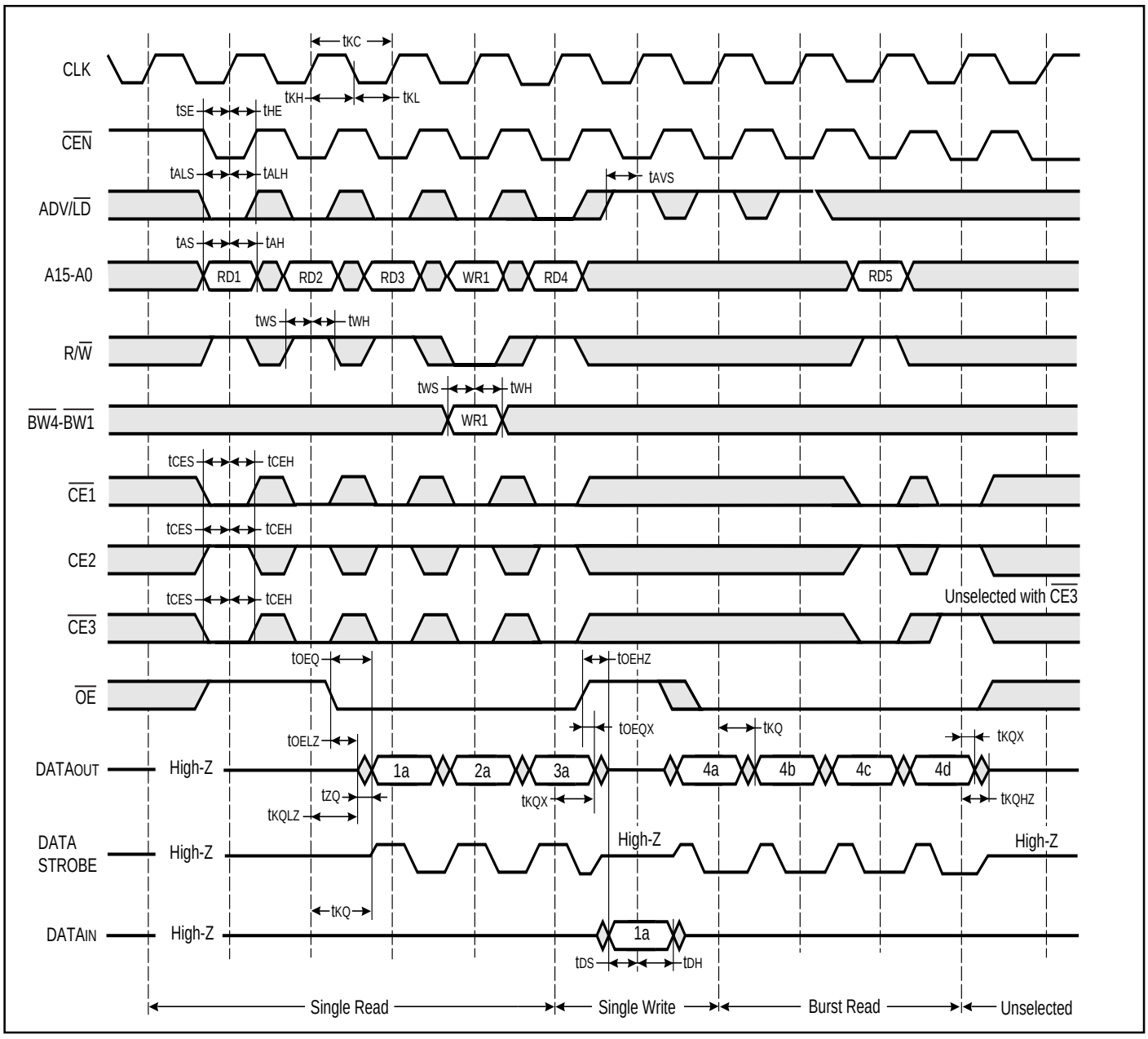
Figure 2

READ/WRITE CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	-5		-6		-7		-8		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
fmax	Clock Frequency	—	100	—	83	—	75	—	66	MHz
t_{KC}	Cycle Time	10	—	12	—	13	—	15	—	ns
t_{KH}	Clock High Time	4	—	4	—	6	—	6	—	ns
t_{KL}	Clock Low Time	4	—	4	—	6	—	6	—	ns
t_{KQ}	Clock Access Time	—	5	—	6	—	7	—	8	ns
t_{KQX}[2]	Clock High to Output Invalid	1.5	—	1.5	—	1.5	—	1.5	—	ns
t_{KQLZ}[2,3]	Clock High to Output Low-Z	2.0	—	2.0	—	2.0	—	2.0	—	ns
t_{KQHZ}[2,3]	Clock High to Output High-Z	1.5	3.5	2	3.5	2	3.5	2	3.5	ns
t_{OEQ}	Output Enable to Output Valid	—	5	—	6	—	6	—	6	ns
t_{OEQX}[2]	Output Disable to Output Invalid	0	—	0	—	0	—	0	—	ns
t_{OELZ}[2,3]	Output Enable to Output Low-Z	0	—	0	—	0	—	0	—	ns
t_{OEHZ}[2,3]	Output Disable to Output High-Z	—	3.5	—	3.5	—	3.5	—	3.5	ns
t_{AS}	Address Setup Time	2.0	—	2.0	—	2.0	—	2.0	—	ns
t_{WS}	Read/Write Setup Time	2.0	—	2.0	—	2.0	—	2.0	—	ns
t_{CES}	Chip Enable Setup Time	2.0	—	2.0	—	2.0	—	2.0	—	ns
t_{SE}	Clock Enable Setup Time	2.0	—	2.0	—	2.0	—	2.0	—	ns
t_{AVS}	Address Advance Setup Time	2.0	—	2.0	—	2.0	—	2.0	—	ns
t_{AH}	Address Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t_{HE}	Clock EnableHold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t_{WH}	Write Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t_{CEH}	Chip Enable Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t_{ALS}	Advance/Load (ADV/$\overline{LD}$) Setup Time	2.0	—	2.0	—	2.0	—	2.0	—	ns
t_{ALH}	Advance/Load (ADV/$\overline{LD}$) Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
tds	Data Setup Time	2.0	—	2.0	—	2.0	—	2.0	—	ns
tdh	Data Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
tzq	I/O From Tri-State to Valid	1.5	2.5	1.5	2.5	1.5	2.5	1.5	2.5	ns

Notes:
1. Configuration signal MODE is static and must not change during normal operation.
2. Guaranteed but not 100% tested. This parameter is periodically sampled.
3. Tested with load in Figure 2.

READ/WRITE CYCLE TIMING



ORDERING INFORMATION

Commercial Range: 0°C to +70°C

Speed (ns)	Order Part Number	Package
5	IS61NW6432-5TQ	TQFP
	IS61NW6432-5PQ	PQFP
6	IS61NW6432-6TQ	TQFP
	IS61NW6432-6PQ	PQFP
7	IS61NW6432-7TQ	TQFP
	IS61NW6432-7PQ	PQFP
8	IS61NW6432-8TQ	TQFP
	IS61NW6432-8PQ	PQFP

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