512K x 32 Module nvSRAM

3.3V High Speed SRAM with Non-Volatile Storage

FEATURES

- -55ºC to 125ºC Operation
- True non-volatile SRAM (no batteries)
- 20 ns, 25 ns, and 45 ns access times
- Automatic STORE on power down with only a small capacitor
- STORE to QuantumTrap® nonvolatile elements initiated by software, device pin, or AutoStore® on power down
- RECALL to SRAM initiated by software or power up
- Infinite Read, Write, and Recall cycles
- 200,000 STORE cycles to QuantumTrap
- 20 year data retention
- Single 3.3V +/- 0.3V operation
- Ceramic Hermetic 68 Quad Flat Pack
  -Matches compatible pinout footprint of SRAM & EEPROM Module

OPTIONS / MARKING

• 68 Ceramic Quad Flat Pack	Q
68 Ceramic Quad Flat Pack	QB
• Timing (Cycle Time)	
45ns	-45
25ns	-25
20ns	-20
• Operating Temperature Ranges	
-Industrial Temp (-40°C to 85° C)	IT
-Enhanced Temp (-40°C to 105° C)	ET
-Military Temp (-55°C to 125°C)	XT
-Military Processing (-55°C to 125°C)	MIL

FUNCTIONAL DESCRIPTION

The AS8nvLC512K32 is a fast static RAM, with a nonvolatile element in each memory cell. The memory is organized as 512K bytes of 8 bits for each of 4 die to form 512Kx32. The embedded nonvolatile elements incorporate QuantumTrap technology, producing the world's most reliable nonvolatile memory. The SRAM provides infinite read and write cycles, while independent nonvolatile data resides in the highly reliable QuantumTrap cell. Data transfers from the SRAM to the nonvolatile elements (the STORE operation) takes place automatically at power down. On power up, data is restored to the SRAM (the RECALL operation) from the nonvolatile memory. Both the STORE and RECALL operations are also available under software control.

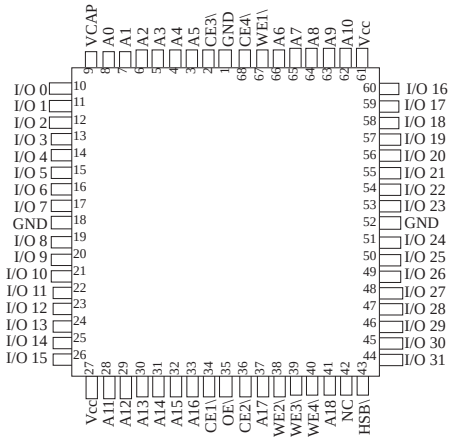
AVAILABLE AS MILITARY SPECIFICATIONS

- Military Processing (MIL-STD-883C para 1.2.2)
- Temperature Range -55C to 125C

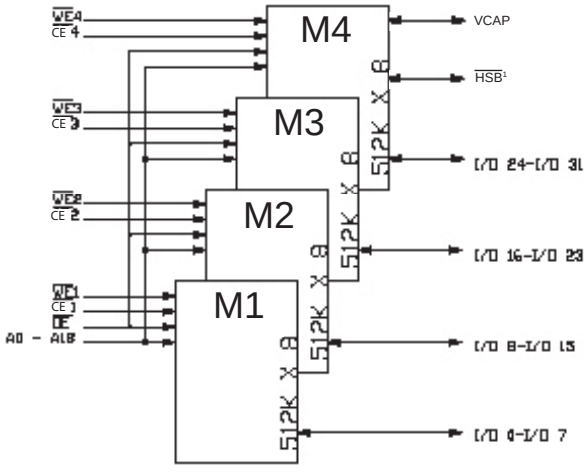
PIN ASSIGNMENT

(Top View)

68 Lead CQFP (Q)



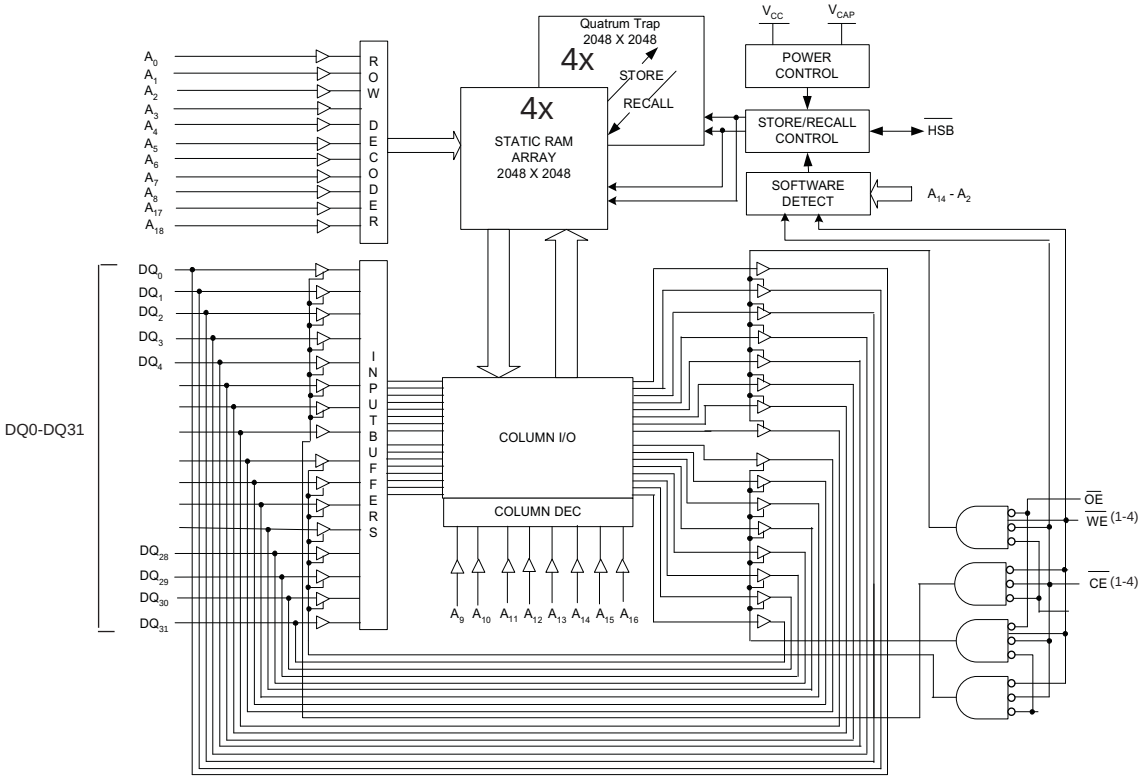
PINOUT / BLOCK DIAGRAM



Notes:
1. HSB\ signal is wired to all 4 die in module. This can be left open if not used.

Pin Name	I/O Type	Description
A0 – A18	Input	Address Inputs Used to Select one of the 524,288 32-bit words of the nvSRAM.
DQ0 – DQ7 DQ0 – DQ15 DQ16 -DQ23 DQ24 - DQ31	Input/Output	Bidirectional Data I/O Lines for die M1 (DQ0-7), M2 (DQ8-15), M3 (DQ16-23), M4 (DQ 24-31)
$WE\backslash_{1-4}$	Input	Write Enable Input, Active LOW. When selected LOW, data on the I/O pins is written to the specific address location.
$CE\backslash_{1-4}$	Input	Chip Enable Input, Active LOW. When LOW, selects the chip. When HIGH, deselects the chip.
OE\	Input	Output Enable, Active LOW. The active LOW OE input enables the data output buffers during read cycles. I/O pins are tri-stated on deasserting OE HIGH.
V_{SS}	Ground	Ground for the Device. Must be connected to the ground of the system.
V_{CC}	Power Supply	Power Supply Inputs to the Device.
HSB\	Input/Output	Hardware Store Busy (HSB\). When LOW this output indicates that a hardware store is in progress. When pulled LOW external to the chip it initiates a nonvolatile STORE operation. A weak internal pull up resistor keeps this pin HIGH if not connected (connection optional). After each store operation HSB\ is driven HIGH for short time with standard output high current.
V_{CAP}	Power Supply	AutoStore Capacitor. Supplies power to the nvSRAM during power loss to store data from SRAM to nonvolatile elements.
NC	No Connect	No Connect. This pin is not connected to the die.

LOGIC BLOCK DIAGRAM



Device Operation

The AS8nvLC512K32 nvSRAM is made up of two functional components paired in the same physical cell. They are a SRAM memory cell and a nonvolatile QuantumTrap cell. The SRAM memory cell operates as a standard fast static RAM. Data in the SRAM is transferred to the nonvolatile cell (the STORE operation), or from the nonvolatile cell to the SRAM (the RECALL operation). Using this unique architecture, all cells are stored and recalled in parallel. During the STORE and RECALL operations, SRAM read and write operations are inhibited. The AS8nvLC512K32 supports infinite reads and writes similar to a typical SRAM. In addition, it provides infinite RECALL operations from the nonvolatile cells and up to 200K STORE operations. See the Truth Table For SRAM Operations for a complete description of read and write modes.

SRAM Read

The AS8nvLC512K32 performs a read cycle when CE\ and OE\ are LOW and WE\ and HSB\ are HIGH. The address specified on pins A0-18 determines which of the 524,288 data bytes. When the read is initiated by an address transition, the outputs are valid after a delay of t_{AA} (read cycle 1). If the read is initiated by CE\ or OE\, the outputs are valid at t_{ACE} or at t_{DOE}, whichever is later (read cycle 2). The data output repeatedly responds to address changes within the t_{AA} access time without the need for transitions on any control input pins. This remains valid until another address change or until CE\ or OE\ is brought HIGH, or WE\ or HSB\ is brought LOW.

SRAM Write

A write cycle is performed when CE\ and WE\ are LOW and HSB\ is HIGH. The address inputs must be stable before entering the write cycle and must remain stable until CE\ or WE\ goes HIGH at the end of the cycle. The data on the common I/O pins DQ0–31 are written into the memory if the data is valid t_{SD} before the end of a WE\ controlled write or before the end of an CE\ controlled write. It is recommended that OE\ be kept HIGH during the entire write cycle to avoid data bus contention on common I/O lines. If OE\ is left LOW, internal circuitry turns off the output buffers tHZWE after WE\ goes LOW.

AutoStore Operation

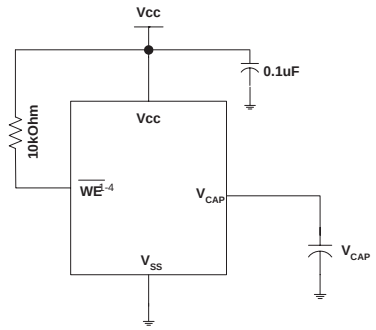
The AS8nvLC512K32 stores data to the nvSRAM using one of the following three storage operations: Hardware Store activated by HSB\; Software Store activated by an address sequence; AutoStore on device power down. The AutoStore operation is a unique feature of QuantumTrap technology and is enabled by default on the AS8nvLC512K32.

During a normal operation, the device draws current from V_{CC} to charge a capacitor connected to the V_{CAP} pin. This stored charge is used by the chip to perform a single STORE operation. If the voltage on the V_{CC} pin drops below V_{SWITCH}, the part automatically disconnects the V_{CAP} pin from V_{CC}. A STORE operation is initiated with power provided by the V_{CAP} capacitor.

Figure 2 shows the proper connection of the storage capacitor (V_{CAP}) for automatic store operation. Refer to DC Electrical Characteristics for the size of V_{CAP}. The voltage on the V_{CAP} pin is driven to V_{CC} by a regulator on the chip. A pull up should be placed on WE\ to hold it inactive during power up. This pull up is effective only if the WE\ signal is tri-state during power up. Many MPUs tri-state their controls on power up. This should be verified when using the pull up. When the nvSRAM comes out of power-on-recall, the MPU must be active or the WE\ held inactive until the MPU comes out of reset.

To reduce unnecessary nonvolatile stores, AutoStore and hardware store operations are ignored unless at least one write operation has taken place since the most recent STORE or RECALL cycle. Software initiated STORE cycles are performed regardless of whether a write operation has taken place. The HSB\ signal is monitored by the system to detect if an AutoStore cycle is in progress.

Figure 2. AutoStore Mode



Hardware STORE Operation

The AS8nvLC512K32 provides the HSB\[6] pin to control and acknowledge the STORE operations. Use the HSB\ pin to request a hardware STORE cycle. When the HSB pin is driven LOW, the AS8nvLC512K32 conditionally initiates a STORE operation after t_{DELAY}. An actual STORE cycle only begins if a write to the SRAM has taken place since the last STORE or RECALL cycle. The HSB\ pin also acts as an open drain driver that is internally driven LOW to indicate a busy condition when the STORE (initiated by any means) is in progress.

SRAM read and write operations that are in progress when HSB is driven LOW by any means are given time to complete before the STORE operation is initiated. After HSB\ goes LOW, the AS8nvLC512K32 continues SRAM operations for tDELAY. If a write is in progress when HSB\ is pulled LOW it is enabled a time, t_{DELAY} to complete. However, any SRAM write cycles requested after HSB\ goes LOW are inhibited until HSB\ returns HIGH. In case the write latch is not set, HSB\ is not driven LOW by the AS8nvLC512K32. But any SRAM read and write cycles are inhibited until HSB\ is returned HIGH by MPU or other external source.

During any STORE operation, regardless of how it is initiated, the AS8nvLC512K32 continues to drive the HSB\ pin LOW, releasing it only when the STORE is complete. When the STORE operation is completed, the AS8nvLC512K32 remains disabled until the HSB\ pin returns HIGH. Leave the HSB\ unconnected if it is not used..

Hardware RECALL (Power Up)

During power up or after any low power condition (VCC< VSWITCH), an internal RECALL request is latched. When VCC again exceeds the sense voltage of VSWITCH, a RECALL cycle is automatically initiated and takes tHRECALL to complete. During this time, HSB is driven LOW by the HSB driver.

Software STORE

Transfer data from the SRAM to the nonvolatile memory with a software address sequence. The AS8nvLC512K32 software STORE cycle is initiated by executing sequential CE controlled read cycles from six specific address locations in exact order. During the STORE cycle an erase of the previous nonvolatile data is first performed, followed by a program of the nonvolatile elements. After a STORE cycle is initiated, further input and output are disabled until the cycle is completed.

Because a sequence of READs from specific addresses is used for STORE initiation, it is important that no other read or write accesses intervene in the sequence, or the sequence is aborted and no STORE or RECALL takes place.

To initiate the software STORE cycle, the following read sequence must be performed.
1. Read Address 0x4E38 Valid READ
2. Read Address 0xB1C7 Valid READ
3. Read Address 0x83E0 Valid READ
4. Read Address 0x7C1F Valid READ
5. Read Address 0x703F Valid READ
6. Read Address 0x8FC0 Initiate STORE Cycle

The software sequence may be clocked with CE controlled reads or OE controlled reads. After the sixth address in the sequence is entered, the STORE cycle commences and the chip is disabled. HSB is driven LOW. It is important to use read cycles and not write cycles in the sequence, although it is not necessary that OE be LOW for a valid sequence. After the tSTORE cycle time is fulfilled, the SRAM is activated again for the read and write operation.

Software RECALL

Transfer the data from the nonvolatile memory to the SRAM with a software address sequence. A software RECALL cycle is initiated with a sequence of read operations in a manner similar to the software STORE initiation. To initiate the RECALL cycle, the following sequence of CE controlled read operations must be performed.
1. Read Address 0x4E38 Valid READ
2. Read Address 0xB1C7 Valid READ
3. Read Address 0x83E0 Valid READ
4. Read Address 0x7C1F Valid READ
5. Read Address 0x703F Valid READ
6. Read Address 0x4C63 Initiate RECALL Cycle

Internally, RECALL is a two step procedure. First, the SRAM data is cleared; then, the nonvolatile information is transferred into the SRAM cells. After the tRECALL cycle time, the SRAM is again ready for read and write operations. The RECALL operation does not alter the data in the nonvolatile elements.

Mode Selection

CE\$_{1-4}$	WE\$_{1-4}$	OE\ [13]	A15-A0 [7]	Mode	I/O$_{0-31}$	Power
H	X	X	X	Not Selected	Output High Z	Standby
L	H	L	X	Read SRAM	Output Data	Active
L	L	X	X	Write SRAM	Input Data	Active
L	H	L	0x4E38	Read SRAM	Output Data	Active [8]
			0xB1C7	Read SRAM	Output Data	
			0x83E0	Read SRAM	Output Data	
			0x7C1F	Read SRAM	Output Data	
			0x703F	Read SRAM	Output Data	
			0x8B45	AutoStore Disable	Output Data	

Notes
7. While there are 19 address lines on the AS8nvLC512K32, only the 13 address lines (A14 - A2) are used to control software modes. Rest of the address lines are don't care.
8. The six consecutive address locations must be in the order listed. WE must be HIGH during all six cycles to enable a nonvolatile cycle.
13.WE\ must be HIGH during SRAM read cycles.

Mode Selection (continued)

$CE\backslash_{1-4}$	$WE\backslash_{1-4}$	$OE\backslash$ [13]	A15-A0 [7]	Mode	I/O_{0-31}	Power
L	H	L	0x4E38	Read SRAM	Output Data	Active [8]
			0xB1C7	Read SRAM	Output Data	
			0x83E0	Read SRAM	Output Data	
			0x7C1F	Read SRAM	Output Data	
			0x703F	Read SRAM	Output Data	
			0x4B46	AutoStore Enable	Output Data	
L	H	L	0x4E38	Read SRAM	Output Data	Active I_{CC2} [8]
			0xB1C7	Read SRAM	Output Data	
			0x83E0	Read SRAM	Output Data	
			0x7C1F	Read SRAM	Output Data	
			0x703F	Read SRAM	Output Data	
			0x8FC0	Nonvolatile Store	Output High Z	
L	H	L	0x4E38	Read SRAM	Output Data	Active [8]
			0xB1C7	Read SRAM	Output Data	
			0x83E0	Read SRAM	Output Data	
			0x7C1F	Read SRAM	Output Data	
			0x703F	Read SRAM	Output Data	
			0x4C63	Nonvolatile Recall	Output High Z	

Preventing AutoStore

The AutoStore function is disabled by initiating an AutoStore disable sequence. A sequence of read operations is performed in a manner similar to the software STORE initiation. To initiate the AutoStore disable sequence, the following sequence of CE controlled read operations must be performed:

1. Read address 0x4E38 Valid READ
2. Read address 0xB1C7 Valid READ
3. Read address 0x83E0 Valid READ
4. Read address 0x7C1F Valid READ
5. Read address 0x703F Valid READ
6. Read address 0x8B45 AutoStore Disable

The AutoStore is re-enabled by initiating an AutoStore enable sequence. A sequence of read operations is performed in a manner similar to the software RECALL initiation. To initiate the AutoStore enable sequence, the following sequence of CE controlled read operations must be performed:

1. Read address 0x4E38 Valid READ
2. Read address 0xB1C7 Valid READ
3. Read address 0x83E0 Valid READ
4. Read address 0x7C1F Valid READ
5. Read address 0x703F Valid READ
6. Read address 0x4B46 AutoStore Enable

If the AutoStore function is disabled or re-enabled, a manual STORE operation (hardware or software) must be issued to save the AutoStore state through subsequent power down cycles. The part comes from the factory with AutoStore enabled.

Data Protection

The AS8nvLC512K32 protects data from corruption during low voltage conditions by inhibiting all externally initiated STORE and write operations. The low voltage condition is detected when VCC < VSWITCH. If the AS8nvLC512K32 is in a write mode (both CE and WE are LOW) at power up, after a RECALL or STORE, the write is inhibited until the SRAM is enabled after tLZHSB (HSB to output active). This protects against inadvertent writes during power up or brown out conditions.

Best Practices

nvSRAM products have been used effectively for over 15 years. While ease-of-use is one of the product's main system values, experience gained working with hundreds of applications has resulted in the following suggestions as best practices:

- The nonvolatile cells in this nvSRAM product are delivered from Micross Componenets with 0x00 written in all cells. Incoming inspection routines at customer or contract manufacturer's sites sometimes reprogram these values. Final NV patterns are typically repeating patterns of AA, 55, 00, FF, A5, or 5A. End product's firmware should not assume an NV array is in a set programmed state. Routines that check memory content values to determine first time system configuration, cold or warm boot status, and so on should always program a unique NV pattern (that is, complex 4-byte pattern of 46 E6 49 53 hex or more random bytes) as part of the final system manufacturing test to ensure these system routines work consistently.
- Power up boot firmware routines should rewrite the nvSRAM into the desired state (for example, autostore enabled). While the nvSRAM is shipped in a preset state, best practice is to again rewrite the nvSRAM into the desired state as a safeguard against events that might flip the bit inadvertently such as program bugs and incoming inspection routines.
- The V_{CAP} value specified in this data sheet includes a minimum and a maximum value size. Best practice is to meet this requirement and not exceed the maximum V_{CAP} value because the nvSRAM internal algorithm calculates V_{CAP} charge and discharge time based on this max V_{CAP} value. Customers that want to use a larger V_{CAP} value to make sure there is extra store charge and store time should discuss their V_{CAP} size selection with Micross Components to understand any impact on the V_{CAP} voltage level at the end of a t_{RECALL} period.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature .....–65°C to +150°C
Maximum Accumulated Storage Time
At 150°C Ambient Temperature.....1000h
At 85°C Ambient Temperature.....20 Years
Ambient Temperature with
Power Applied .....–55°C to +125°C
Supply Voltage on Vcc Relative to GND..... –0.5V to 4.1V
Voltage Applied to Outputs
in High-Z State ..... –0.5V to Vcc + 0.5V
Input Voltage ..... –0.5V to Vcc + 0.5V
Transient Voltage (<20 ns) on
Any Pin to Ground Potential.....–2.0V to Vcc + 2.0V
Package Power Dissipation
Capability (TA = 25°C) 1.0W
Surface Mount Pb Soldering
Temperature (3 Seconds).....+260°C
DC Output Current (1 output at a time, 1s duration) .....15 mA
Static Discharge Voltage ..... > 2001V
(per MIL-STD-883, Method 3015)
Latch Up Current..... > 200 mA

Operating Range

Range	Ambient Temperature	Vcc
Military	-55°C to +125°C	3.0V to 3.6V
Enhanced	-40°C to +105°C	3.0V to 3.6V
Industrial	-40°C to +85°C	3.0V to 3.6V

DC Electrical Characteristics

Over the Operating Range (V_{CC} = 3.0V to 3.6V)

Parameter	Description	Test Conditions		Min	Max	Unit
I_{CC1}	Average V_{CC} Current	tRC = 20 ns tRC = 25 ns tRC = 45 ns Values obtained without output loads (IOUT = 0 mA)	Military		320 320 260	mA mA mA
			Industrial		280 280 210	mA mA mA
I_{CC2}	Average V_{CC} Current during STORE	All Inputs Don't Care, V_{CC} = Max Average current for duration t_{STORE}			40	mA
I_{CC3} [9]	Average V_{cc} Current at t_{RC}= 200 ns, 3V, 25°C typical	All I/P cycling at CMOS levels. Values obtained without output loads (I_{OUT} = 0 mA).			140	mA
I_{CC4}	Average V_{CAP} Current during AutoStore Cycle	All Inputs Don't Care, V_{CC} = Max Average current for duration t_{STORE}			20	mA
I_{SB}	V_{CC} Standby Current	CE \≥ (V_{CC} – 0.2V). All others V_{IN} ≤ 0.2V or ≥ (V_{CC} – 0.2V). Standby current level after nonvolatile cycle is complete. Inputs are static. f = 0 MHz.			20	mA
I_{IX} [10]	Input Leakage Current (except HSB\)	V_{CC} = Max, VSS ≤ VIN ≤ VCC		-5	5	µA
	Input Leakage Current (for HSB\)	V_{CC} = Max, VSS ≤ VIN ≤ VCC		-400	10	µA
I_{OZ}	Off-State Output Leakage Current	V_{CC} = Max, V_{SS} ≤ V_{OUT} ≤ V_{CC}, CE\ or OE\ ≥ V_{IH} or WE\ ≤ V_{IL}		-10	10	µA
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage			V_{SS} - 0.3	0.8	V
V_{OH}	Output HIGH Voltage	I_{OUT} = –2 mA		2.4		V
V_{OL}	Output LOW Voltage	I_{OUT} = 4 mA			0.4	V
V_{CAP}	Storage Capacitor	Between V_{CAP} pin and V_{SS}, 6.3V Rated		80	180	µF

Notes

9. Typical conditions for the active current shown on the DC Electrical characteristics are average values at 25°C (room temperature), and VCC = 3V. Not 100% tested.
10. The HSB\ pin has IOUT = -8 uA for VOH of 2.4V when both active HIGH and LOW drivers are disabled. When they are enabled standard VOH and VOL are valid. This parameter is characterized but not tested.

Data Retention and Endurance

Parameter	Description	Min	Unit
$DATA_R$	Data Retention	20	Years
NV_C	Nonvolatile STORE Operation	200	Cycles

Capacitance

In the following table, the capacitance parameters are listed. [12]

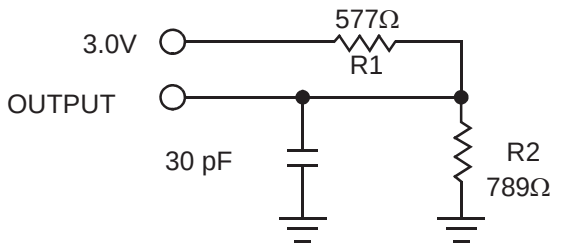
Parameter	Description	Test Conditions	Min	Unit
C_{IN}	Input Capacitance (Addr, OE\, HSB\) x 4	T_A = 25°C, f = 1 MHz, V_{CC} = 0 to 3.0V	50	pF
C_{IN}	Input Capacitance ($CE\backslash_{1-4}$, $WE\backslash_{1-4}$ x 1		20	pF
$C_{OUT(DQ)}$	I/O Capacitance x 1		25	pF

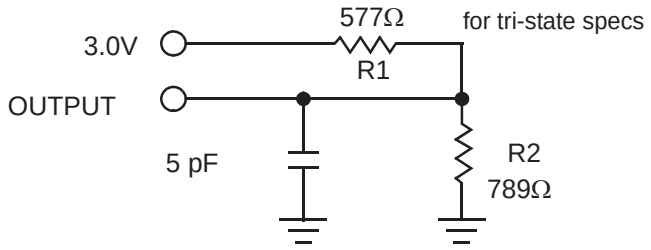
Thermal Resistance

In the following table, the thermal resistance parameters are listed. [12]

Parameter	Description	Test Conditions	68 CQFP	Unit
Θ_{JC}	Thermal Resistance (Junction to Case)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	11.3	°C/W

AC Test Loads





AC Test Conditions

Input Pulse Levels .....0V to 3V
Input Rise and Fall Times (10% - 90%)..... <3 ns
Input and Output Timing Reference Levels 1.5V

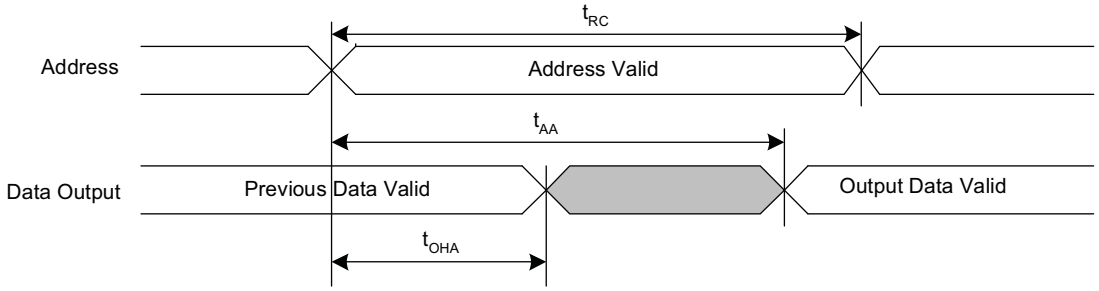
Note
12. These parameters are guaranteed by design but not tested.

AC Switching Characteristics

Parameters		Description	20 ns		25 ns		45 ns		Unit
Micross Parameters	Alt Parameters		Min	Max	Min	Max	Min	Max	
SRAM Read Cycle									
t_{ACE}	t_{ACS}	Chip Enable Access Time		20		25		45	ns
t_{RC} [13]	t_{RC}	Read Cycle Time	20		25		45		ns
t_{AA} [14]	t_{AA}	Address Access Time		20		25		45	ns
t_{DOE}	t_{OE}	Output Enable to Data Valid		10		12		20	ns
t_{OHA} [14]	t_{OH}	Output Hold After Address Change	2		2		2		ns
t_{LZCE} [12, 15]	t_{LZ}	Chip Enable to Output Active	2		2		2		ns
t_{HZCE} [12, 15]	t_{HZ}	Chip Disable to Output Active		8		10		15	ns
t_{LZOE} [12, 15]	t_{OLZ}	Output Enable to Output Active	0		0		0		ns
t_{HZOE} [12, 15]	t_{OHZ}	Output Disable to Output Inactive		8		10		15	ns
t_{PU} [12]	t_{PA}	Chip Enable to Power Active	0		0		0		ns
t_{PD} [12]	t_{PS}	Chip Disable to Power Standby		20		25		45	ns
t_{DBE}	-	Byte Enable to Data Valid		10		12		20	ns
t_{LZBE} [12]	-	Byte Enable to Output Active	0		0		0		ns
t_{HZBE} [12]	-	Byte Disable to Output Inactive		8		10		15	ns
SRAM Write Cycle									
t_{WC}	t_{WC}	Write Cycle Time	20		25		45		ns
t_{PWE}	t_{WP}	Write Pulse Width	15		20		30		ns
t_{SCE}	t_{CW}	Chip Enable to End of Write	15		20		30		ns
t_{SD}	t_{DW}	Data Setup to End of Write	8		10		15		ns
t_{HD}	t_{DH}	Data Hold After End of Write	0		0		0		ns
t_{AW}	t_{AW}	Address Setup to End of Write	15		20		30		ns
t_{SA}	t_{AS}	Address Setup to End of Write	0		0		0		ns
t_{HA}	t_{WR}	Address Hold After End of Write	0		0		0		ns
t_{HZWE} [12, 15, 16]	t_{WZ}	Write Enable to Output Disable		8		10		15	ns
t_{LZWE} [12, 15]	t_{OW}	Output Active after End of Write	2		2		2		ns
t_{BW}	-	Byte Enable to End of Write	15		20		30		ns

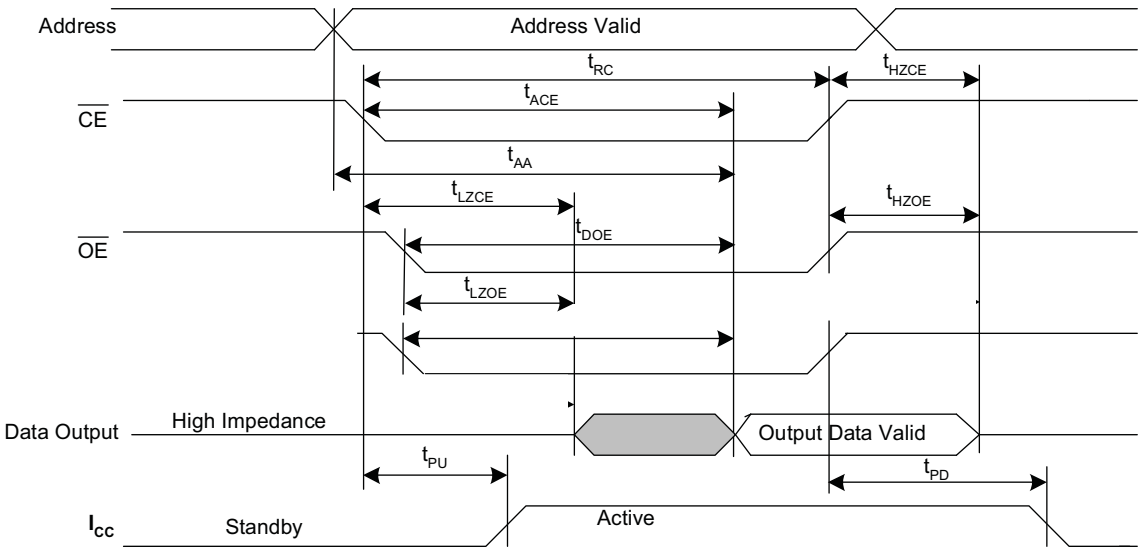
Switching Waveforms

SRAM Read Cycle #1: Address Controlled [13, 14, 17]

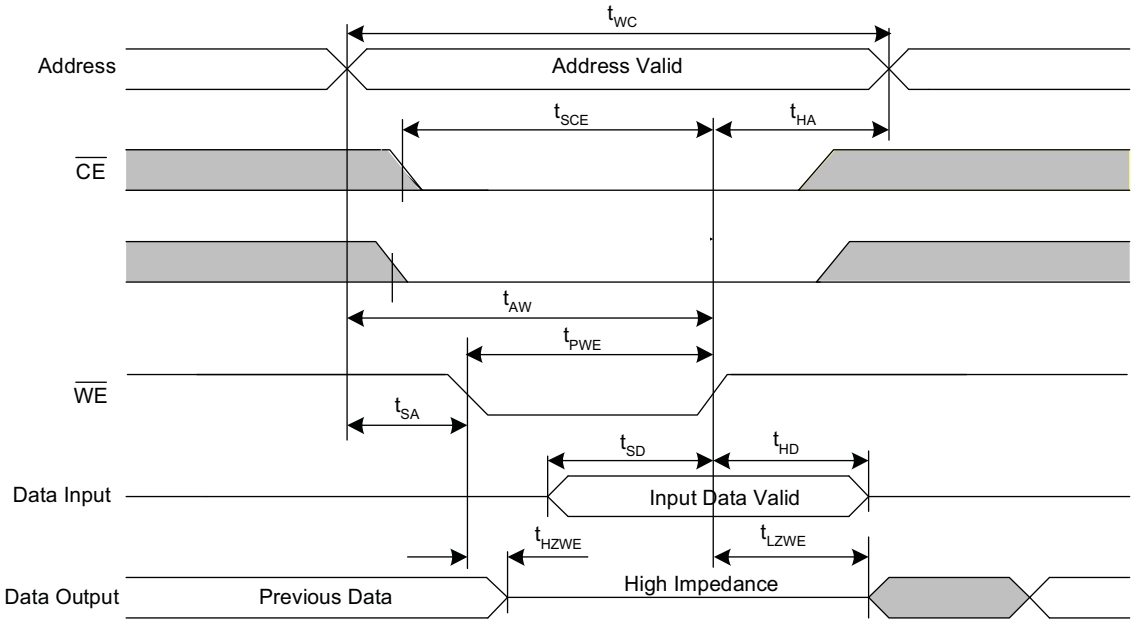


Notes
13.WE\ must be HIGH during SRAM read cycles.
14. Device is continuously selected with CE\, OE\ LOW.
15.Measured ±200 mV from steady state output voltage.
16. If WE\ is LOW when CE\ goes LOW, the outputs remain in the high impedance state.
17. HSB\ must remain HIGH during read and write cycles.

SRAM Read Cycle #2: CE\ and OE\ Controlled [3, 13, 17]

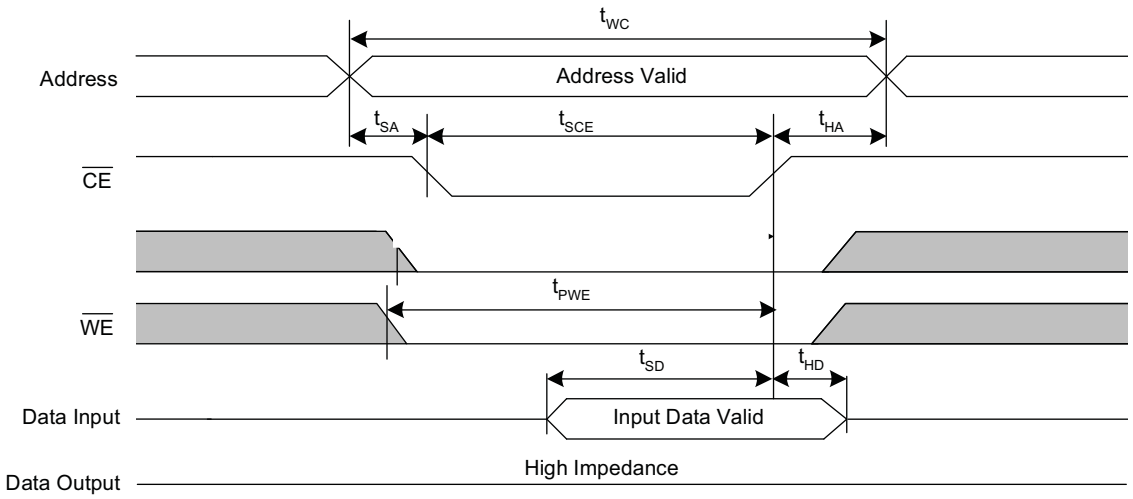


SRAM Write Cycle #1: WE\ Controlled [3, 16, 17,18]



Note
18. CE\ or WE\ must be >V_{IH} during address transitions.

SRAM Write Cycle #2: CE\ Controlled[3, 16, 17, 18]

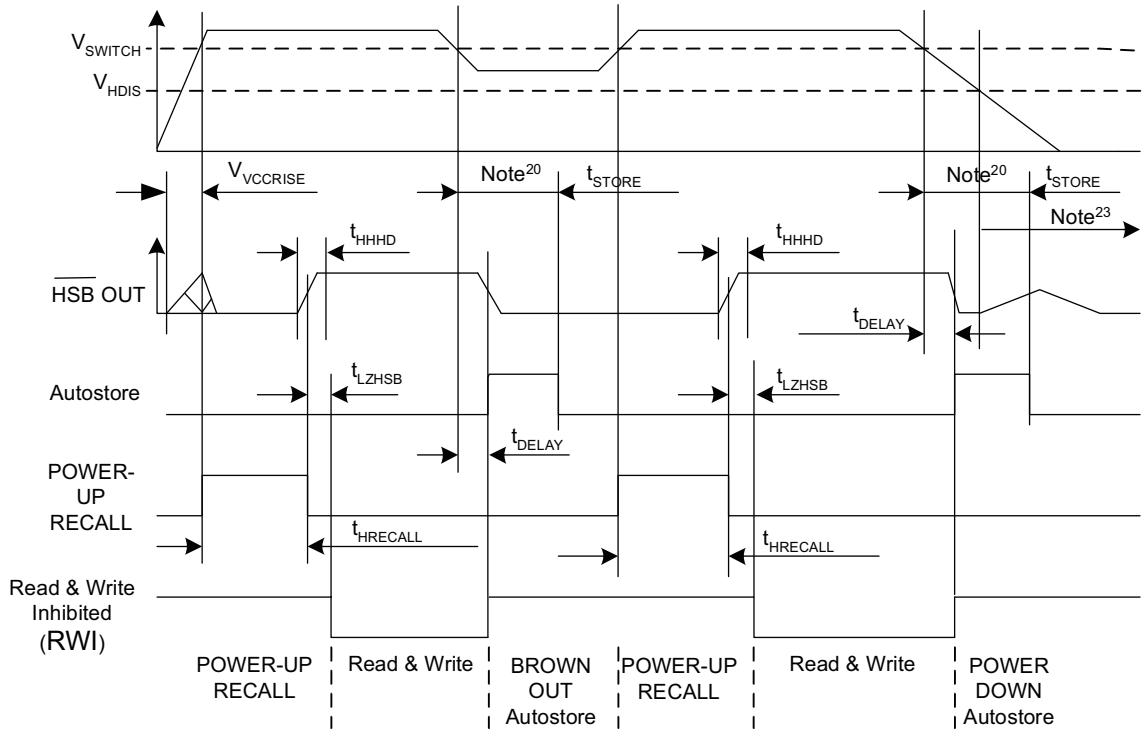


AutoStore/Power Up RECALL

Parameters	Description	20 ns		25 ns		45 ns		Unit
		Min	Max	Min	Max	Min	Max	
$t_{HRECALL}$ [19]	Power Up RECALL Duration		20		20		20	ms
t_{STORE} [20]	STORE Cycle Duration		10		10		10	ms
t_{DELAY} [21]	Time Allowed to Complete SRAM Cycle		20		25		25	ns
V_{SWITCH}	Low Voltage Trigger Level		2.65		2.65		2.65	V
$t_{VCCRISE}$ [12]	VCC Rise Time	150		150		150		µs
V_{HDIS} [12]	HSB\ Output Driver Disable Voltage		1.9		1.9		1.9	V
t_{LZHSB} [12]	HSB\ To Output Active Time		5		5		5	µs
t_{HHHD} [12]	HSB\ High Active Time		500		500		500	ns

Switching Waveforms

AutoStore or Power Up RECALL[22]



Notes
19. tHRECALL starts from the time VCC rises above VSWITCH.
20. If an SRAM write has not taken place since the last nonvolatile cycle, no AutoStore or Hardware Store takes place.
21. On a Hardware STORE, Software Store / Recall, AutoStore Enable / Disable and AutoStore initiation, SRAM operation continues to be enabled for time tDELAY.
22. Read and write cycles are ignored during STORE, RECALL, and while VCC is below VSWITCH.
23. HSB\ pin is driven HIGH to VCC only by internal 100 kOhm resistor, HSB\ driver is disabled.

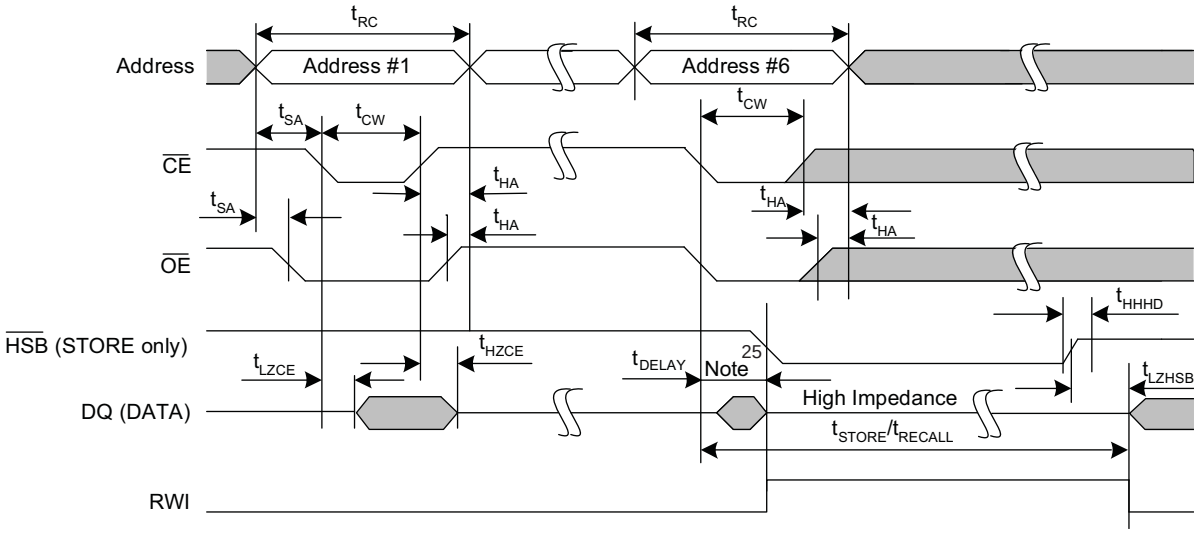
Software Controlled STORE/RECALL Cycle

In the following table, the software controlled STORE and RECALL cycle parameters are listed.[24, 25]

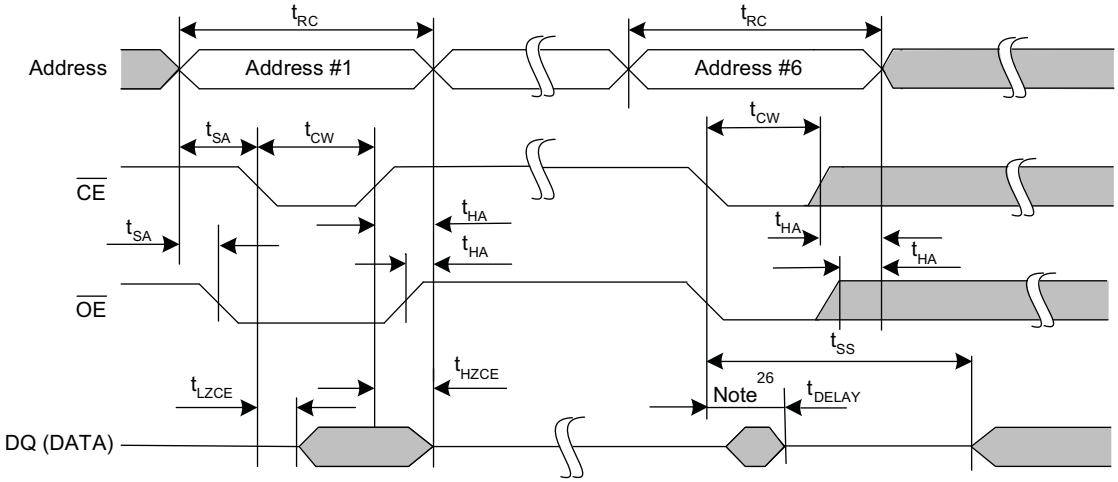
Parameters	Description	20 ns		25 ns		45 ns		Unit
		Min	Max	Min	Max	Min	Max	
t_{RC}	STORE/RECALL Initiation Cycle Time	20		25		45		ns
t_{SA}	Address Setup Time	0		0		0		ns
t_{CW}	Clock Pulse Width	15		25		30		ns
t_{HA}	Address Hold Time	0		0		0		ns
t_{RECALL}	RECALL Duration		200		200		200	µs

Switching Waveforms

CE\ and OE \Controlled Software STORE/RECALL Cycle[26]



AutoStore Enable/Disable Cycle



Notes

24. The software sequence is clocked with CE\ controlled or OE\ controlled reads.
25. The six consecutive addresses must be read in the order listed in the MODE Selection Table. WE\ must be HIGH during all six consecutive cycles.
26. DQ output data at the sixth read may be invalid since the output is disabled at t_{DELAY} time.

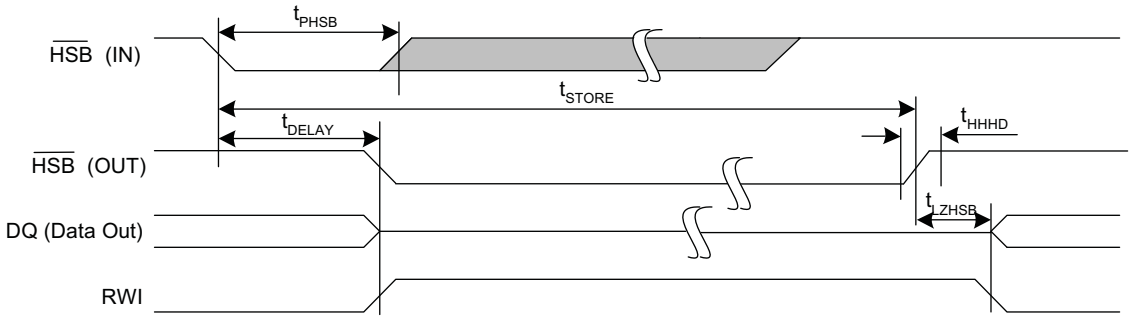
Hardware STORE Cycle

Parameters	Description	20 ns		25 ns		45 ns		Unit
		Min	Max	Min	Max	Min	Max	
t_{DHSB}	HSB\ to Output Active Time when latch not set		20		25		25	ns
t_{PHSB}	Hardware STORE Pulse Width	15		15		15		ns
t_{SS} [27, 28]	Soft Sequence Processing Time		100		100		100	µs

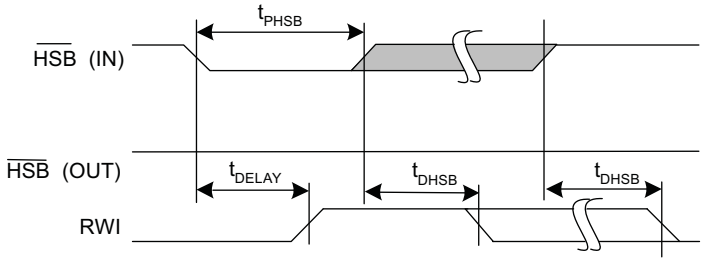
Switching Waveforms

Hardware STORE Cycle[19]

Write latch set

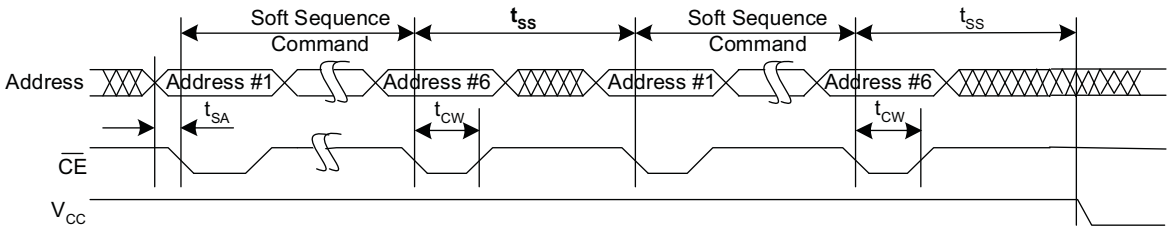


Write latch not set



HSB pin is driven high to V_{CC} only by Internal 100kOhm resistor,
HSB driver is disabled
SRAM is disabled as long as HSB (IN) is driven low.

Soft Sequence Processing[27, 28]



Notes
27. This is the amount of time it takes to take action on a soft sequence command. Vcc power must remain HIGH to effectively register command.
28. Commands such as STORE and RECALL lock out I/O until operation is complete which further increases this time. See the specific command.

Truth Table For SRAM Operations

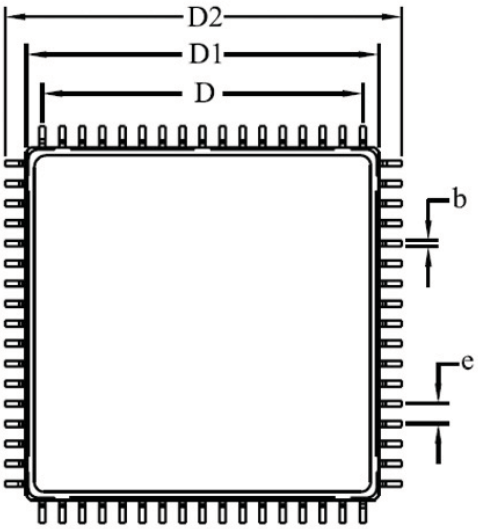
HSB\ should remain HIGH for SRAM Operations.

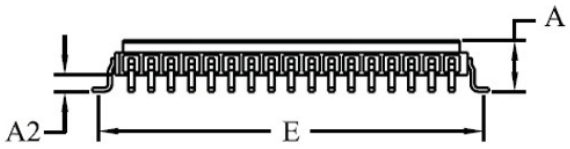
For x32 Configuration

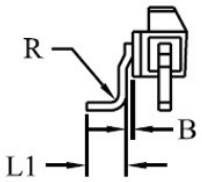
$CE\backslash_{1-4}$	$WE\backslash_{1-4}$	OE\	Inputs / Outputs	Mode	Power
H	X	X	High Z	Deselect / Power Down	Standby
L	H	L	Data Out (DQ0-DQ31)	Read	Active
L	H	H	High Z	Output Disabled	Active
L	L	X	Data In (DQ0-DQ31)	Write	Active

Ceramic 68 Quad Flat Pack

Micross Package Designator Q



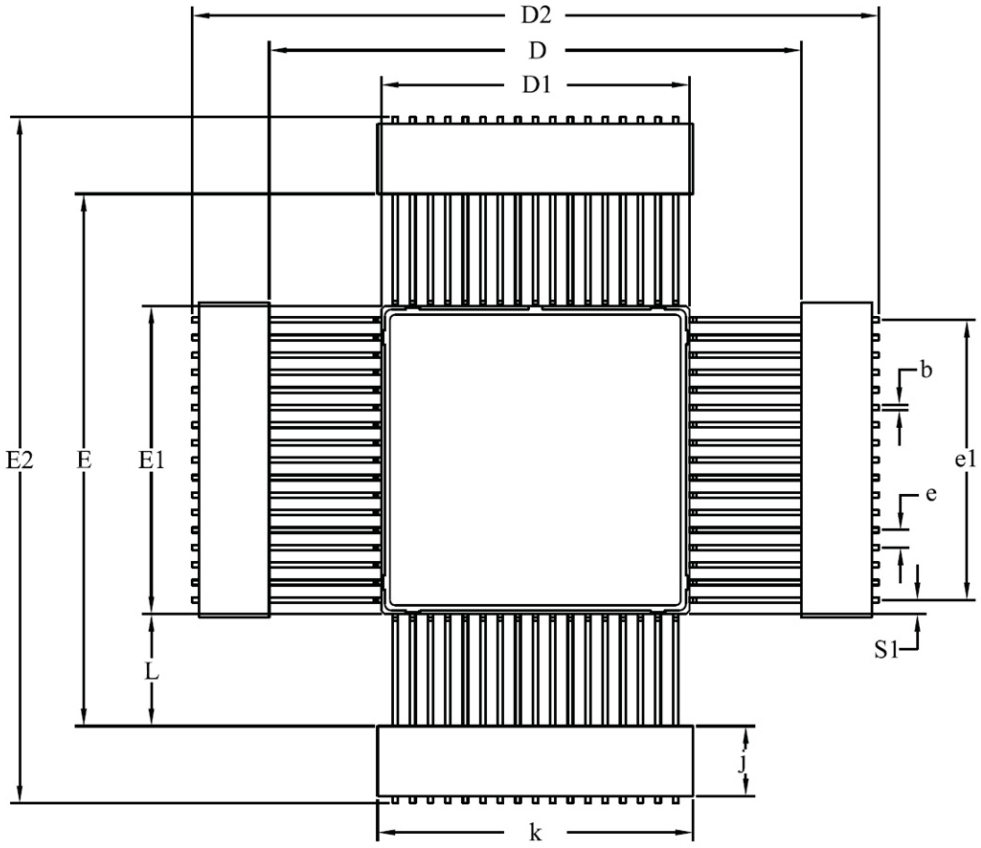




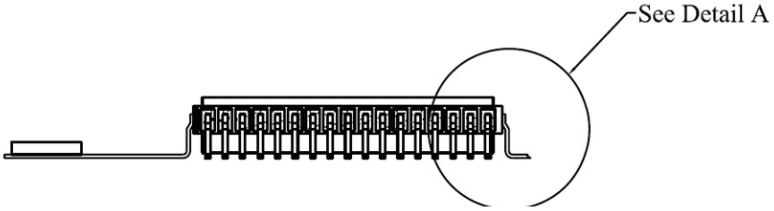
PACKAGE SPECIFICATION		
Symbol	Min	Max
A	.135	.155
A2	.005	.020
B	.010 REF	
b	.013	.017
D	.800 BSC	
D1	.870	.890
D2	.980	1.000
E	.936	.956
e	.050 BSC	
R	.010 TYP	
L1	.035	.045
Dimensions in inches		

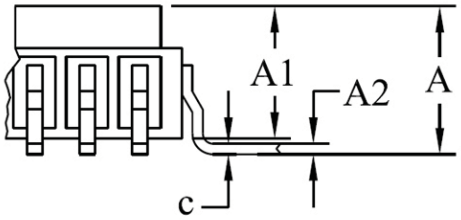
Micross Package Designator QB

Ceramic 68 Quad Flat Pack



PACKAGE SPECIFICATION		
Symbol	Min	Max
A	.135	.155
A1	.115	.135
A2	.005	.020
b	.013	.017
c	.009	.012
D/E	1.500	1.540
D1/E1	.870	.890
D2/E2	1.920	2.000
e	.050 BSC	
e1	.800 BSC	
J	.190	.210
k	.890	.910
L	.310	.330
S1	.040 BSC	
Dimensions in inches		





Detail A

Ordering Information

Micross Part Number	Configuration	Package Type	Speed (ns)	Process
AS8nvLC512K32QB-20/MIL	512K x 32	68 Quad Flat Pack w/ Tie-bar	20	MIL
AS8nvLC512K32QB-25/MIL	512K x 32	68 Quad Flat Pack w/ Tie-bar	25	MIL
AS8nvLC512K32QB-45/MIL	512K x 32	68 Quad Flat Pack w/ Tie-bar	45	MIL
AS8nvLC512K32QB-20/XT	512K x 32	68 Quad Flat Pack w/ Tie-bar	20	XT
AS8nvLC512K32QB-25/XT	512K x 32	68 Quad Flat Pack w/ Tie-bar	25	XT
AS8nvLC512K32QB-45/XT	512K x 32	68 Quad Flat Pack w/ Tie-bar	45	XT
AS8nvLC512K32QB-20/ET	512K x 32	68 Quad Flat Pack w/ Tie-bar	20	ET
AS8nvLC512K32QB-25/ET	512K x 32	68 Quad Flat Pack w/ Tie-bar	25	ET
AS8nvLC512K32QB-45/ET	512K x 32	68 Quad Flat Pack w/ Tie-bar	45	ET
AS8nvLC512K32QB-20/IT	512K x 32	68 Quad Flat Pack w/ Tie-bar	20	IT
AS8nvLC512K32QB-25/IT	512K x 32	68 Quad Flat Pack w/ Tie-bar	25	IT
AS8nvLC512K32QB-45/IT	512K x 32	68 Quad Flat Pack w/ Tie-bar	45	IT
AS8nvLC512K32Q-20/MIL	512K x 32	68 Quad Flat Pack	20	MIL
AS8nvLC512K32Q-25/MIL	512K x 32	68 Quad Flat Pack	25	MIL
AS8nvLC512K32Q-45/MIL	512K x 32	68 Quad Flat Pack	45	MIL
AS8nvLC512K32Q-20/XT	512K x 32	68 Quad Flat Pack	20	XT
AS8nvLC512K32Q-25/XT	512K x 32	68 Quad Flat Pack	25	XT
AS8nvLC512K32Q-45/XT	512K x 32	68 Quad Flat Pack	45	XT
AS8nvLC512K32Q-20/ET	512K x 32	68 Quad Flat Pack	20	ET
AS8nvLC512K32Q-25/ET	512K x 32	68 Quad Flat Pack	25	ET
AS8nvLC512K32Q-45/ET	512K x 32	68 Quad Flat Pack	45	ET
AS8nvLC512K32Q-20/IT	512K x 32	68 Quad Flat Pack	20	IT
AS8nvLC512K32Q-25/IT	512K x 32	68 Quad Flat Pack	25	IT
AS8nvLC512K32Q-45/IT	512K x 32	68 Quad Flat Pack	45	IT

*** AVAILABLE PROCESSES**	**TEMPERATURE**
IT = Industrial Temperature Range	-40^0C to $+85^0$C
ET = Enhanced Temperature Range	-40^0C to $+105^0$C
XT = Military Temperature Range	-55^0C to $+125^0$C
MIL = Military Processing	-55^0C to $+125^0$C

DOCUMENT TITLE

512K x 32 nvSRAM 3.3V High Speed SRAM with Non-Volatile Storage

REVISION HISTORY

Rev #	History	Release Date	Status
0.0	Document Creation	August 2009	Advance
0.1	Added Micross Information	January 2010	Advance
0.5	Added Q & QB Package; changes to pin description, DC Electrical, Capacitance, Thermal Resistance, AutoStore and order chart; updated diagrams on page 13, added diagrams and chart on page 14, added Enhanced temp on page 1 & 18, changed CS\ to CE\ on Pin Assignment and Pin Out on page 1, added MIL processing	April 2010	Advance