USB2412

2-Port USB 2.0 Hi-Speed Hub Controller

PRODUCT FEATURES

Datasheet

General Description

The SMSC USB2412 hub is a low-power, single transaction translator (STT) hub controller IC with two downstream ports for embedded USB applications. The SMSC hub controller supports low-speed, full-speed, and hi-speed (if operating as a hi-speed hub) downstream devices on all of the enabled downstream ports.

Features

- Fully integrated USB termination and pull-up/pull-down resistors
- Supports a single external 3.3 V supply source; internal regulators provide 1.2 V internal core voltage
- On-chip 24 MHz crystal and ceramic resonator driver or external 24 MHz clock input
- ESD protection up to 4 kilovolts on all USB pins
- Supports self-powered operation
- Contains a built-in default configuration; no external configuration options or components are required
- Downstream ports as optional non-removable ports
- Supports compound devices on a port-by-port basis
- 28-pin QFN (5 x 5 mm) lead-free RoHS compliant package
- Supports the commercial temperature range: 0ºC to +70ºC

Highlights

- High performance, low-power, small footprint hub controller IC with two downstream ports
- Fully compliant with the USB 2.0 specification
- 28QFN low pin count package
- Optimized for minimal bill-of-materials and low cost designs

Applications

- Automobile/home audio systems
- Cable/DSL modems
- Embedded systems
- Gaming consoles
- HDD enclosures
- IP telephony
- KVM switches
- LCD monitors and TVs
- Multi-function USB peripherals
- Mobile PC docking
- PC motherboards
- PC media drive bay
- Portable hub boxes
- Point-of-Sale (POS) systems
- Printers and scanners
- Server front panels
- Set-top boxes, DVD players, DVR/PVR
- Thin client terminals

ORDER NUMBERS:

ORDER NUMBERS	PACKAGE TYPE	PACKAGE SIZE	REEL SIZE
USB2412-DZK	28-Pin QFN Lead-Free, RoHS Compliant Package (includes tape and reel option)	5 x 5 x 0.5 mm	-
USB2412-DZK-TR			

Product meets the Halogen Maximum Concentration Values per IEC61249-2-21

For RoHS compliance and environmental information, please visit www.smsc.com/rohs.

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Chapter 1 Acronyms

OCS: Over-Current Sense

PCB: Printed Circuit Board

PHY: Physical Layer

PLL: Phase-Locked Loop

QFN: Quad Flat No Leads

RoHS: Restriction of Hazardous Substances Directive

SIE: Serial Interface Engine

TT: Transaction Translator

Chapter 2 Block Diagram

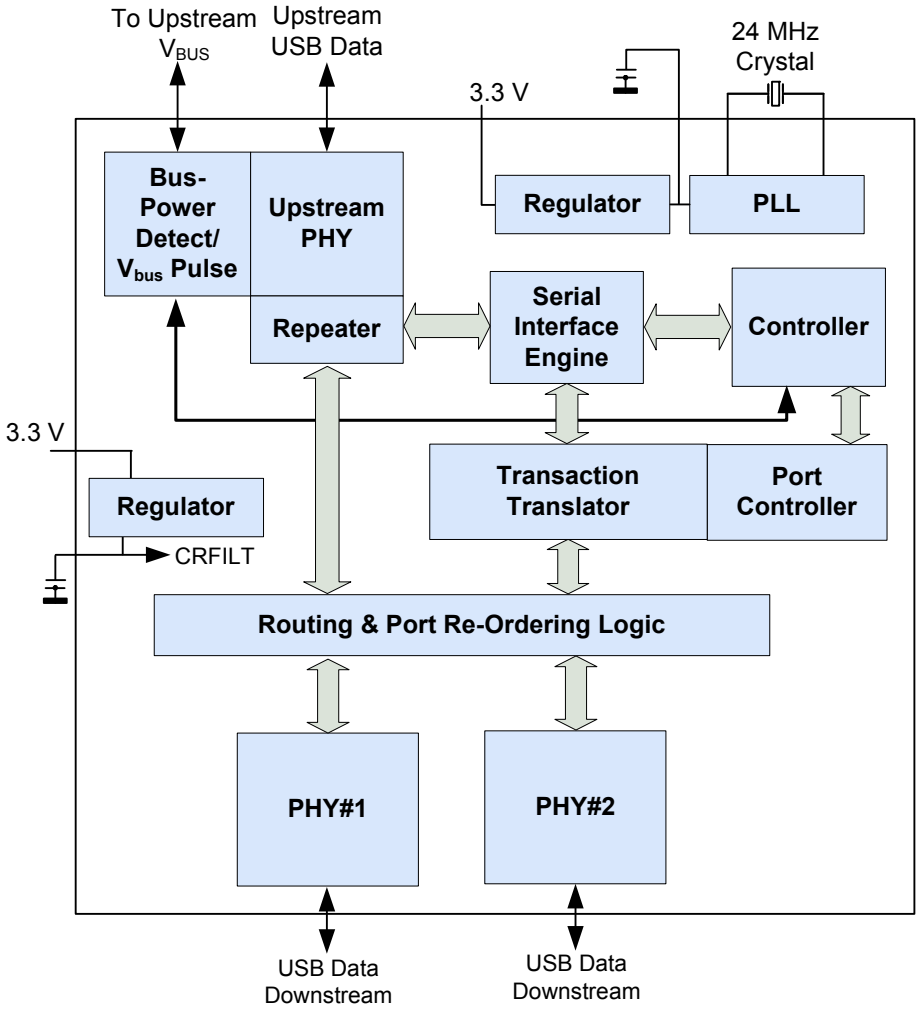


Figure 2.1 USB2412 Block Diagram

Chapter 3 Pin Descriptions

This chapter is organized by a set of pin configurations followed by a corresponding pin list organized by function according to their associated interface. A detailed description list of each signal (named in the pin list) is organized by function in Table 3.2, “USB2412 Pin Descriptions,” on page 10. Please refer to Table 3.3, “Buffer Type Descriptions,” on page 12 for a list of buffer types.

The “N” symbol in the signal name indicates that the active, or asserted, state occurs when the signal is at a low voltage level. When “N” is not present after the signal name, the signal is asserted when it is at the high voltage level.

The terms assertion and negation are used exclusively. This is done to avoid confusion when working with a mixture of “active low” and “active high” signals. The term assert, or assertion, indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term negate, or negation, indicates that a signal is inactive.

3.1 Pin Configuration

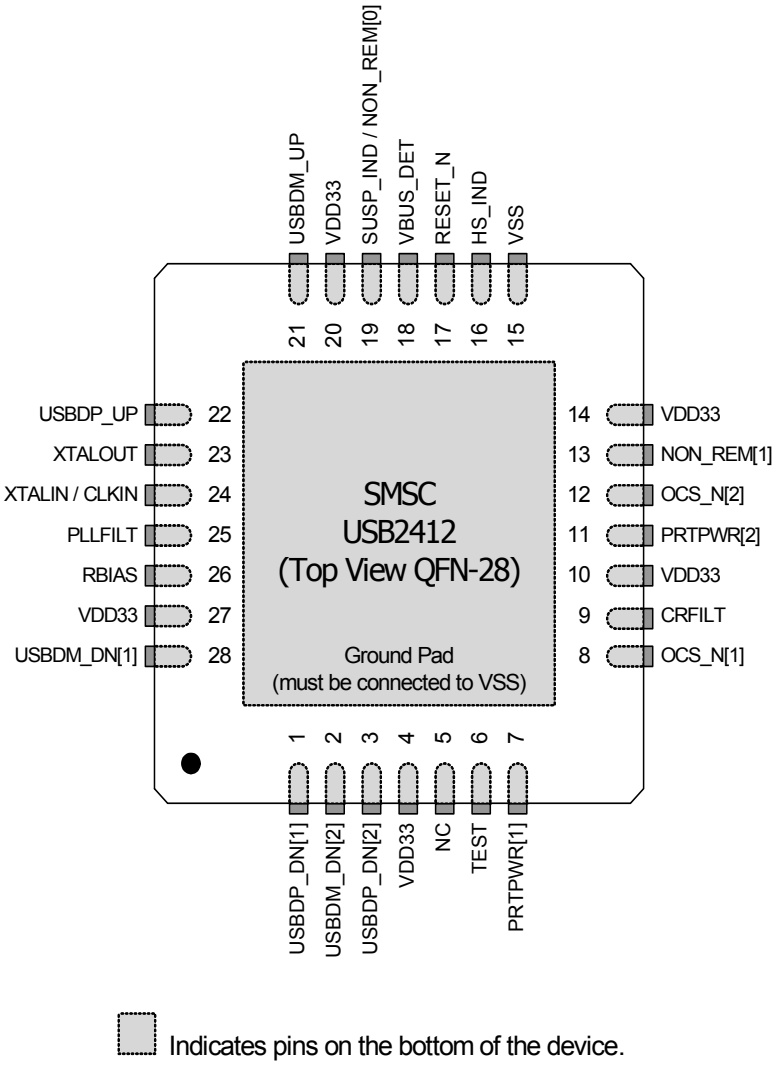


Figure 3.1 2-Port 28-Pin QFN

3.2 28-Pin Table

Table 3.1 USB2412 28-Pin Table

UPSTREAM USB 2.0 INTERFACES (3 PINS)			
USBDP_UP	USBDM_UP	VBUS_DET	
DOWNSTREAM 2-PORT USB 2.0 INTERFACES (9 PINS)			
USBDP_DN[1]	USBDM_DN[1]	USBDP_DN[2]	USBDM_DN[2]
PRT_PWR[1]	PRT_PWR[2]	OCS_N[1]	OCS_N[2]
RBIAS			
MISC (7 PINS)			
RESET_N	TEST	XTALIN / CLKIN	XTALOUT
NON_REM[1]	SUSP_IND / NON_REM[0]	HS_IND	
POWER, GROUND, AND NO CONNECTS (9 PINS)			
(5) VDD33	CRFILT	PLLFILT	VSS
NC			
TOTAL 28			

3.3 Pin Descriptions (Grouped by Function)

Table 3.2 USB2412 Pin Descriptions

PIN #	SYMBOL	BUFFER TYPE	DESCRIPTION
UPSTREAM USB 2.0 INTERFACES			
21 22	USBDM_UP USBDP_UP	IO-U	USB Bus Data These pins connect to the upstream USB bus data signals (host, port, or upstream hub).
18	VBUS_DET	I/O12	Detect Upstream VBUS Power Detects the state of Upstream VBUS power. The SMSC hub monitors VBUS_DET to determine when to assert the internal D+ pull-up resistor which signals a connect event. When designing a detachable hub, this pin should be connected to VBUS on the upstream port via a 2 to 1 voltage divider. For self-powered applications with a permanently attached host, this pin must be connected to 3.3 V. According to Section 7.2.1 of the USB 2.0 specification, a downstream port can never provide power to its D+ or D- pull-up resistors unless the upstream port's VBUS is in the asserted (powered) state. The VBUS_DET pin on the hub monitors the state of the upstream VBUS signal and will not pull-up the D+ resistor if VBUS is not active. If VBUS goes from an active to an inactive state (Not Powered), the hub will remove power from the D+ pull-up resistor within 10 seconds.
DOWNSTREAM USB 2.0 INTERFACES			
1 3 28 2	USBDP_DN[1] USBDP_DN[2] USBDM_DN[1] USBDM_DN[2]	IO-U	Hi-Speed USB Data These pins connect to the downstream USB peripheral devices attached to the hub's ports.
7 11	PRTPWR[1] PRTPWR[2]	IPD	USB Power Enable Enables power to USB peripheral devices that are downstream. The hub supports active high power controllers only.
8 12	OCS_N[1] OCS_N[2]	IPU	Over-Current Sense Input from external current monitor indicating an over-current condition. This pin contains an internal pull-up to the 3.3 V supply.
26	RBIAS	I-R	USB Transceiver Bias A 12.0 kΩ (+/- 1%) resistor is attached from ground to this pin to set the transceiver's internal bias settings.

Table 3.2 USB2412 Pin Descriptions (continued)

PIN #	SYMBOL	BUFFER TYPE	DESCRIPTION
			MISC
13	NON_REM[1]	I/O	Non-removable Port Strap Option This pin will be sampled (in conjunction with SUSP_IND / NON_REM[0]) at RESET_N negation to determine if ports [2:1] contain permanently attached (non-removable) devices: NON_REM[1:0] = '00', all ports are removable. NON_REM[1:0] = '01', port 1 is non-removable. NON_REM[1:0] = '1x, ports 1 and 2 are non-removable. Please see Section 3.5, "Non-Removable Strap Option" for a complete description.
19	SUSP_IND /	I/O	Active/Suspend Status LED Suspend Indicator: Indicates USB hub state. Please see Section 3.6, "LED Strap Option" for a complete description. NON_REM[0] = '0', SUSP_IND is active high. NON_REM[0] = '1', SUSP_IND is active low. 'negated' = Unconfigured, or configured and in USB Suspend 'asserted' = The hub is configured and is active (i.e., not in suspend)
	NON_REM[0]		Non-removable Port Strap Option This pin will be sampled (in conjunction with NON_REM[1]) at RESET_N negation to determine if ports [2:1] contain permanently attached (non-removable) devices: NON_REM[1:0] = '00', all ports are removable. NON_REM[1:0] = '01', port 1 is non-removable. NON_REM[1:0] = '1x', ports 1 and 2 are non-removable. Please see Section 3.5, "Non-Removable Strap Option" for a complete description.
16	HS_IND	I/O12	Hi-Speed Upstream Port Indicator HS_IND: Hi-speed Indicator for upstream port connection speed. **Note:** An LED can be attached for visual indication. Please see Section 3.6, "LED Strap Option" for a complete description. When an LED is not used, this pin requires a 50 kΩ or higher resistor to ground. 'Asserted' = the hub is connected at HS 'Negated' = the hub is connected at FS
24	XTALIN	ICLKx	24 MHz Crystal Input This pin connects to either one terminal of the crystal or to an external 24 MHz clock when a crystal is not used.
	CLKIN		External Clock Input This pin connects to either one terminal of the crystal or to an external 24 MHz clock when a crystal is not used.

Table 3.2 USB2412 Pin Descriptions (continued)

PIN #	SYMBOL	BUFFER TYPE	DESCRIPTION
23	XTALOUT	OCLKx	24 MHz Crystal Output This is the other terminal of the crystal, or a no connect pin, when an external clock source is used to drive XTALIN/CLKIN.
6	TEST	IPD	TEST pin User must treat as a no connect pin or connect to ground. No trace or signal should be routed or attached to this pin.
17	RESET_N	IS	RESET Input The system can reset the chip by driving this input low. The minimum active low pulse is 1 µs.
POWER, GROUND, and NO CONNECTS			
9	CRFILT		VDD Core Regulator Filter Capacitor This pin must have a 1.0 µF (or greater) ±20% (ESR <0.1 Ω) capacitor to VSS.
4 10 14 20 27	VDD33		3.3 V Power
25	PLLFILT		PLL Regulator Filter Capacitor This pin must have a 1.0 µF (or greater) ±20% (ESR <0.1 Ω) capacitor to VSS.
15	VSS		Ground Pad / ePad The package slug is the only VSS for the device and must be tied to ground with multiple vias.
5	NC		No Connect No signal or trace should be routed or attached to these pins.

3.4 Buffer Type Descriptions

Table 3.3 Buffer Type Descriptions

BUFFER	DESCRIPTION
I/O	Input/Output.
IPD	Input with internal weak pull-down resistor.
IPU	Input with internal weak pull-up resistor.

Table 3.3 Buffer Type Descriptions (continued)

BUFFER	DESCRIPTION
IS	Input with Schmitt trigger.
I/O12	Input/Output buffer with 12 mA sink and 12 mA source.
ICLKx	XTAL clock input.
OCLKx	XTAL clock output.
I-R	RBIAS.
I/O-U	Analog Input/Output defined in USB specification.

3.5 Non-Removable Strap Option

The strap function of pins 13 and 19 are enabled thru the internal default configuration. The driver type of each strap pin is I/O (no internal pull-up or pull-down for the input function). Use this type of strap option for NON_REM[1:0]. Figure 3.2 shows an example of Strap High and Strap Low. Use the Strap High configuration to set the strap option value to a '1'. Use the Strap Low configuration to set the strap option value to '0'.

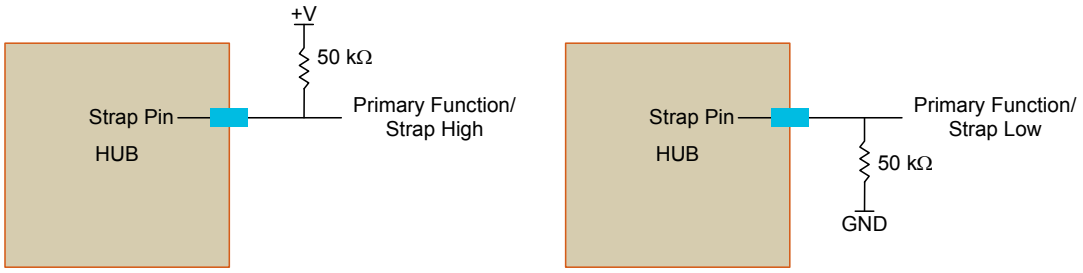


Figure 3.2 Non-Removable Pin Strap Example

3.6 LED Strap Option

The strap function of pins 13 and 19 are enabled thru the internal default configuration. The driver type of each strap pin is I/O (no internal pull-up or pull-down for the input function). When the strap pin shares functionality with an LED, use this type of strap option.

The internal logic will drive the LED appropriately (active high or low) depending on the sampled strap option. Figure 3.3 shows an example of Strap High and Strap Low. Use the Strap High configuration to set the strap option value to a '1'. Use the Strap Low configuration to set the strap option value to '0'.

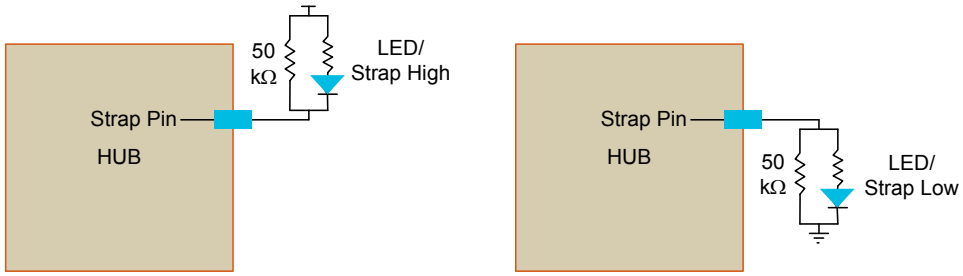


Figure 3.3 LED Pin Strap Example

Chapter 4 Internal Default Configuration

4.1 Hub

SMSC's USB 2.0 hub is fully specification compliant to the Universal Serial Bus specification, version 2.0, April 27, 2000 (12/7/2000 and 5/28/2002 Errata). Please reference Chapter 10 (Hub specification) for general details regarding hub operation and functionality.

The hub provides 1 Transaction Translator (TT) that is shared by both downstream ports (defined as Single-TT configuration). The TT contains 4 non-periodic buffers.

4.1.1 Hub Configuration

The USB2412 only supports internal defaults with the exception of the non-removable strap option (NON_REM[1:0]). The hub internal default settings are as follows:

- Internal Default Configuration without any over-rides
- Strap options enabled
- Self-powered operation enabled
- Individual power switching
- Individual over-current sensing

4.2 Reset

There are two different resets that the hub experiences. One is a hardware reset via the RESET_N pin and the second is a USB Bus Reset.

4.2.1 External Hardware RESET_N

A valid hardware reset is defined as assertion of RESET_N for a minimum of 1 µs after all power supplies are within operating range. While reset is asserted, the hub (and its associated external circuitry) consumes less than 500 µA of current from the upstream USB power source.

Assertion of RESET_N (external pin) causes the following:

1. All downstream ports are disabled, and PRTPWR power to downstream devices is removed.
2. The PHYs are disabled, and the differential pairs will be in a high-impedance state.
3. All transactions immediately terminate; no states are saved.
4. All internal registers return to the default state (in most cases, 00(h)).
5. The external crystal oscillator is halted.
6. The PLL is halted.
7. The hub is "operational" 500 µs after RESET_N is negated.

4.2.1.1 RESET_N

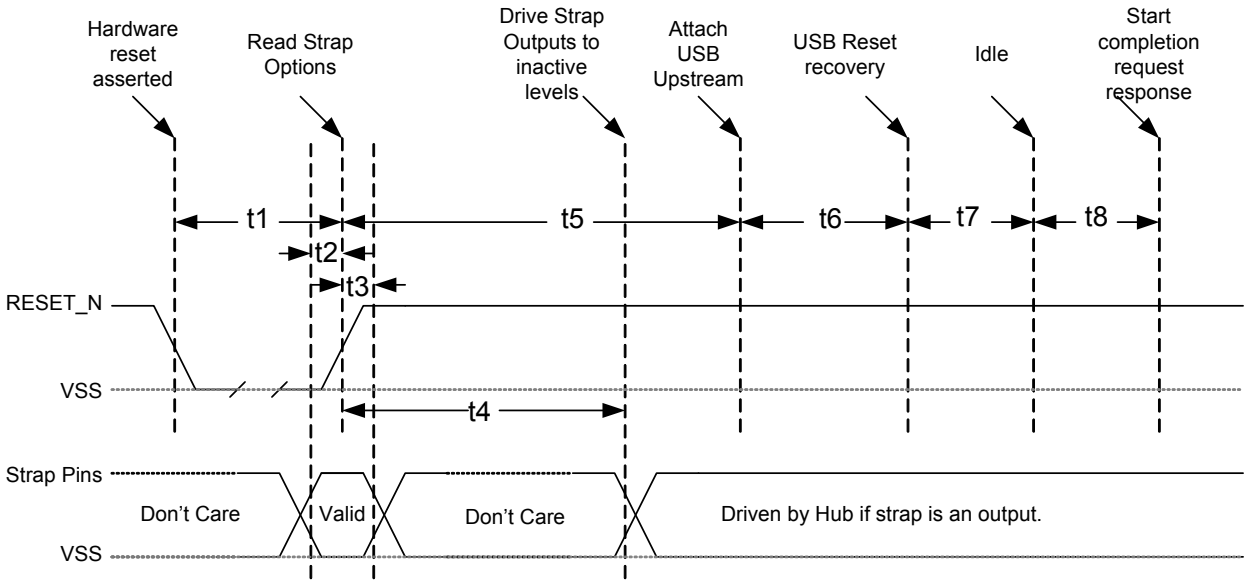


Figure 4.1 Reset_N Timing

Table 4.1 Reset_N Timing

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	RESET_N Asserted.	1			µsec
t2	Strap Setup Time	16.7			nsec
t3	Strap Hold Time.	16.7		1400	nsec
t4	hub outputs driven to inactive logic states		1.5	2	µsec
t5	USB Attach (See Note).			100	msec
t6	Host acknowledges attach and signals USB Reset.	100			msec
t7	USB Idle.		undefined		msec
t8	Completion time for requests (with or without data stage).			5	msec

Note: All power supplies must have reached the operating levels mandated in Chapter 5, DC Parameters, prior to (or coincident with) the assertion of RESET_N.

4.2.2 USB Bus Reset

In response to the upstream port signaling a reset to the hub, the hub does the following:

Note: The hub does not propagate the upstream USB reset to downstream devices.

1. Sets default address to '0'.
2. Sets configuration to: Unconfigured.
3. Negates PRTPWR[2:1] to all downstream ports.
4. Clears all TT buffers.

5. Moves device from suspended to active (if suspended).
6. Complies with Section 11.10 of the USB 2.0 specification for behavior after completion of the reset sequence. The host then configures the hub and the hub's downstream port devices in accordance with the USB specification.

Note: The hub does not propagate the upstream USB reset to downstream devices.

Chapter 5 DC Parameters

5.1 Maximum Guaranteed Ratings

PARAMETER	SYMBOL	MIN	MAX	UNITS
Storage Temperature	T_{STOR}	-55	150	°C
Lead Temperature				°C
3.3 V supply voltage	VDD33 PLLFILT CRFILT		4.6	V
Voltage on any I/O pin		-0.5	5.5	V
Voltage on XTALIN		-0.5	4.0	V
Voltage on XTALOUT		-0.5	2.5	V

Note 5.1 Please refer to JEDEC Specification J-STD-020D.

Note 5.2 Stresses above the specified parameters could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any condition above those indicated in the operation sections of this specification is not implied.

Note 5.3 When powering this device from laboratory or system power supplies, it is important that the absolute maximum ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. When this possibility exists, it is suggested that a clamp circuit be used.

5.2 Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS	COMMENTS
Operating Temperature	T_A	0	70	°C	Ambient temperature in still air.
3.3 V supply voltage	VDD33	3.0	3.6	V	
3.3 V supply rise time	t_{RT}	0	400	µs	See Figure 5.1
Voltage on any I/O pin		-0.3	5.5	V	If any 3.3 V supply voltage drops below 3.0 V, then the MAX becomes: (3.3 V supply voltage) + 0.5
Voltage on XTALIN		-0.3	VDD33	V	

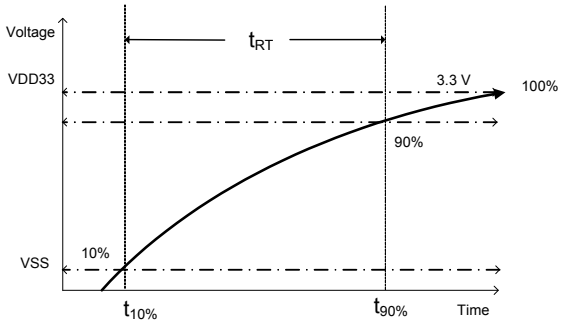


Figure 5.1 Supply Rise Time Model

Table 5.1 DC Electrical Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
I, IS Type Input Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0			V	
Input Leakage	I_{IL}	-10		+10	µA	V_{IN} = 0 to VDD33
Hysteresis ('IS' Only)	V_{HYSI}	250		350	mV	
Input Buffer with Pull-Up (IPU)						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0			V	
Low Input Leakage	I_{ILL}	+35		+90	µA	V_{IN} = 0
High Input Leakage	I_{IHL}	-10		+10	µA	V_{IN} = VDD33
Input Buffer with Pull-Down (IPD)						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0			V	
Low Input Leakage	I_{ILL}	+10		-10	µA	V_{IN} = 0
High Input Leakage	I_{IHL}	-35		-90	µA	V_{IN} = VDD33
ICLK Input Buffer						
Low Input Level	V_{ILCK}			0.5	V	
High Input Level	V_{IHCK}	1.4			V	
Input Leakage	I_{IL}	-10		+10	µA	V_{IN} = 0 to VDD33

Table 5.1 DC Electrical Characteristics (continued)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
O12, I/O12 &I/OSD12 Type Buffer Low Output Level High Output Level Output Leakage Hysteresis ('SD' pad only)	 V_{OL} V_{OH} I_{OL} V_{HYSC}	 2.4 -10 250		 0.4 +10 350	 V V µA mV	 I_{OL} = 12 mA @ VDD33 = 3.3 V I_{OH} = -12 mA @ VDD33 = 3.3 V V_{IN} = 0 to VDD33 (Note 5.1)
Supply Current Unconfigured **Hi-Speed Host**	$I_{CCINTHS}$		40	45	mA	
Supply Current Unconfigured **Full-Speed Host**	$I_{CCINTFS}$		35	40	mA	
Supply Current Configured **Hi-Speed Host, 1 downstream port**	I_{HCH1}		60	65	mA	
Supply Current Configured **Hi-Speed Host, each additional downstream port**			**1 port base + 25 mA**	**1 port base + 25 mA**	mA	
Supply Current Configured **Full-Speed Host, 1 downstream port**	I_{FCC1}		45	50	mA	There is no additional current for additional ports.
Supply Current Configured **Full-Speed Host, each additional downstream port**			**1 port base + 8 mA**	**1 port base + 8 mA**	mA	
Supply Current Suspend	I_{CSBY}		475	1000	µA	All supplies combined
Supply Current Reset	I_{CRST}		550	1100	µA	All supplies combined

Note 5.4 Output leakage is measured with the current pins in high impedance.

Note 5.5 See USB 2.0 specification for USB DC electrical characteristics.

5.2.1 Pin Capacitance

Table 5.2 Pin Capacitance

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITION
		MIN	TYP	MAX		
Clock Input Capacitance	C_{XTAL}			6	pF	All pins except USB pins and the pins under the test tied to AC ground.
Input Capacitance	C_{IN}			6	pF	Capacitance T_A = 25°C fc = 1 MHz VDD33 = 3.3 V
Output Capacitance	C_{OUT}			6	pF	The maximum capacitance values include the full length of the pin pad. Please see the Y dimension in Figure 7.2.

5.2.2 Package Thermal Specifications

Thermal parameters are measured or estimated for devices with the exposed pad soldered to thermal vias in a multilayer 2S2P PCB per JESD51. Thermal resistance is measured from the die to the ambient air.

Table 5.3 36-Pin QFN Package Thermal Parameters

PARAMETER	VELOCITY (meters/sec)	SYMBOL	VALUE	UNIT
Thermal Resistance	0	Θ_{JA}	40.3	°C/W
	1		35.2	
Junction-to-Top-of-Package	0	Ψ_{JT}	0.5	°C/W
	1		0.6	

Chapter 6 AC Specifications

6.1 Oscillator/Crystal

Parallel Resonant, Fundamental Mode, 24 MHz ±350 ppm.

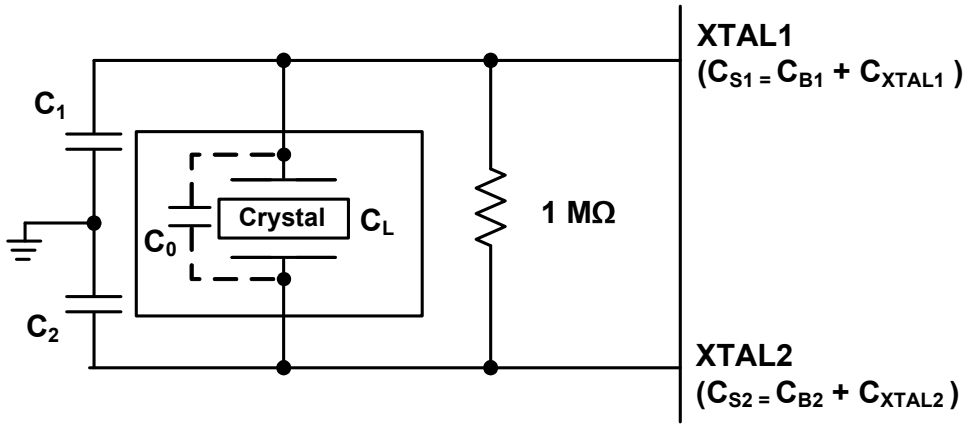


Figure 6.1 Typical Crystal Circuit

Table 6.1 Crystal Circuit Legend

SYMBOL	DESCRIPTION	IN ACCORDANCE WITH
C_0	Crystal shunt capacitance	Crystal manufacturer's specification (See Note 6.1)
C_L	Crystal load capacitance	
C_B	Total board or trace capacitance	OEM board design
C_S	Stray capacitance	SMSC IC and OEM board design
C_{XTAL}	XTAL pin input capacitance	SMSC IC
C_1	Load capacitors installed on OEM board	Calculated values based on Figure 6.2, "Formula to Find the Value of C1 and C2" (See Note 6.2)
C_2		

$$C_1 = 2 \times (C_L - C_0) - C_{S1}$$

$$C_2 = 2 \times (C_L - C_0) - C_{S2}$$

Figure 6.2 Formula to Find the Value of C_1 and C_2

Note 6.1 C_0 is usually included (subtracted by the crystal manufacturer) in the specification for C_L and should be set to '0' for use in the calculation of the capacitance formulas in Figure 6.2, "Formula to Find the Value of C1 and C2". However, the OEM PCB itself may present a parasitic capacitance between XTALIN and XTALOUT. For an accurate calculation of C_1 and C_2, take the parasitic capacitance between traces XTALIN and XTALOUT into account.

Note 6.2 Each of these capacitance values is typically approximately 18 pF.

6.2 Ceramic Resonator

24 MHz ± 350 ppm

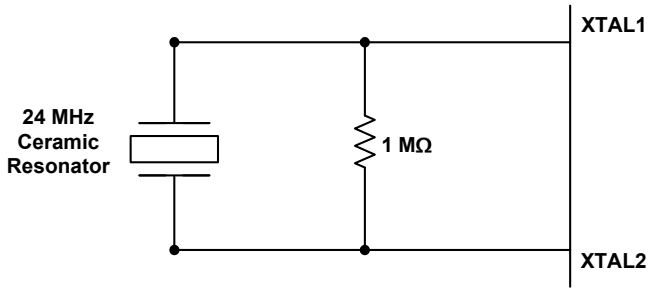


Figure 6.3 Ceramic Resonator Usage with SMSC IC

6.3 External Clock

50% Duty cycle ± 10%, 24 MHz ± 350 ppm, Jitter < 100 ps rms.

The external clock is recommended to conform to the signaling level designated in the JESD76-2 specification on 1.8 V CMOS Logic. XTALOUT should be treated as a no connect.

6.3.1 USB 2.0

The SMSC Hub conforms to all voltage, power, and timing characteristics and specifications as set forth in the USB 2.0 specification. Please refer to the USB 2.0 specification for more information.

Chapter 7 Package Outline

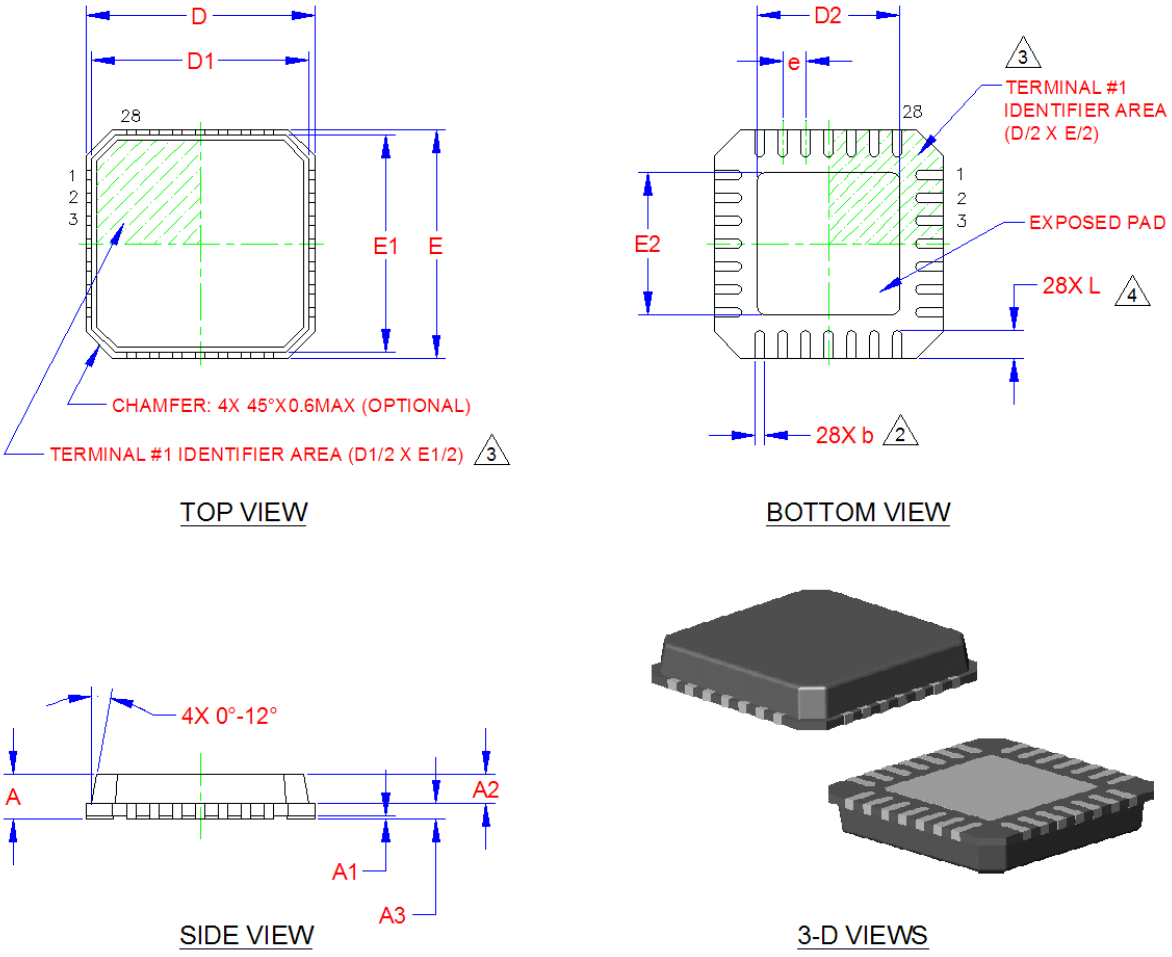


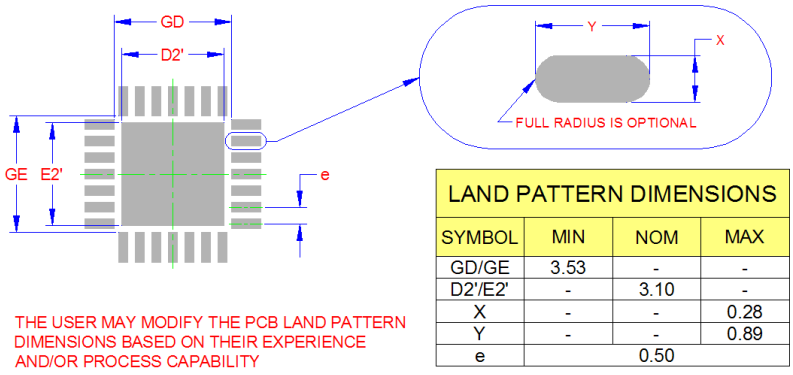
Figure 7.1 USB2412 28-Pin QFN Package Outline (5x5 mm Body, 0.5 Pitch, 3.1 ePad)

Table 7.1 Package Parameters

	MIN	NOMINAL	MAX	NOTE	REMARKS
A	0.80	0.85	1.00	-	Overall Package Height
A1	0	0.02	0.05	-	Standoff
A2	0.60	-	0.80	-	Mold Cap Thickness
D/E	4.90	5.00	5.10	-	X/Y Overall Body Size
D1/E1	4.55	4.75	4.95	-	X/Y Mold Cap Size
D2/E2	3.00	3.10	3.20	-	X/Y Exposed Pad Size
L	0.30	0.40	0.50	-	Terminal Length
b	0.18	0.25	0.30	2	Terminal Width
K	0.45	0.55	-	-	Terminal to ePad Clearance
e	0.50 BSC			-	Terminal Pitch

Notes:

1. All dimensions are in millimeters.
2. Position tolerance of each terminal and exposed pad is ±0.05 mm at maximum material condition. Instances of dimension “b” apply to plated terminals and is measured between 0.15 and 0.33 mm from the terminal tip.
3. Details of terminal #1 identifier are optional. However, they must be located within the area indicated.
4. Coplanarity zone applies to exposed pad and terminals.



LAND PATTERN DIMENSIONS			
SYMBOL	MIN	NOM	MAX
GD/GE	3.53	-	-
D2'/E2'	-	3.10	-
X	-	-	0.28
Y	-	-	0.89
e		0.50	

Figure 7.2 Recommended Printed Circuit Board (PCB) Land Pattern

7.1 Tape and Reel Specification

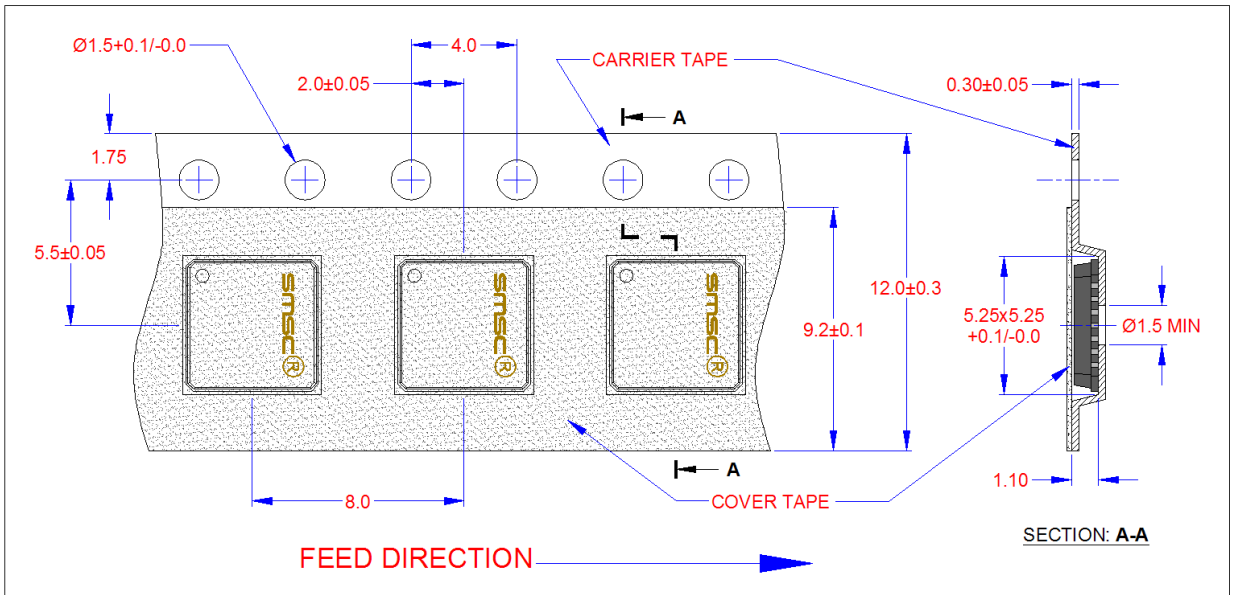
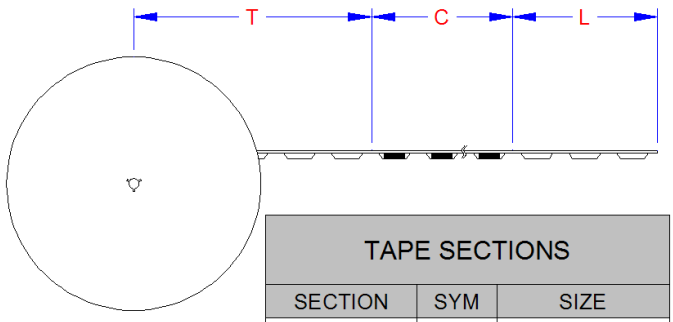
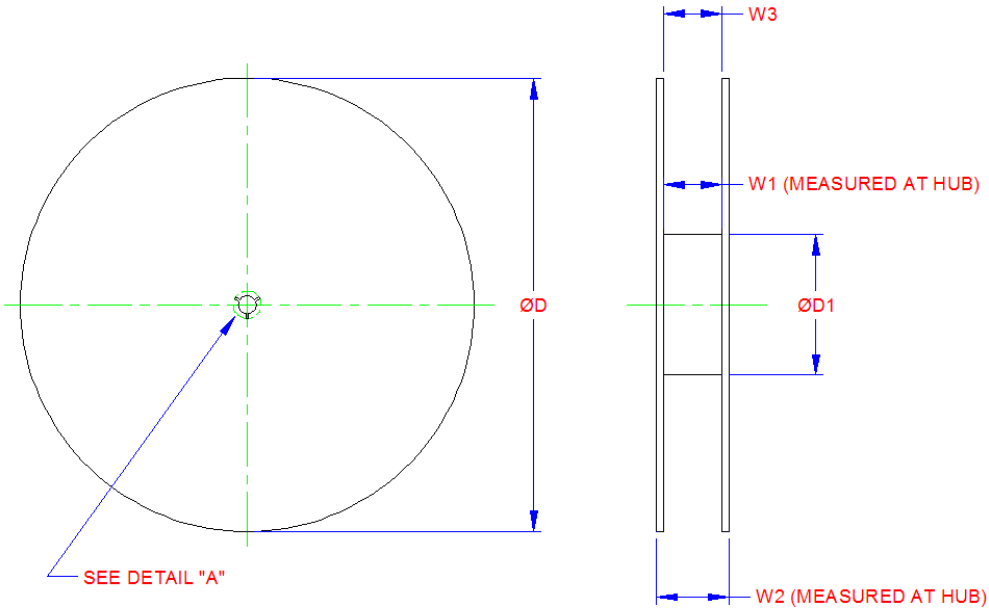


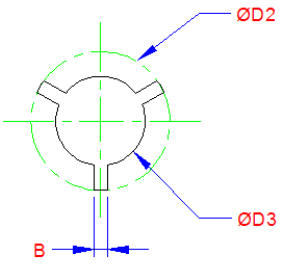
Figure 7.3 28-Pin Package Tape Dimensions and Part Orientation (mm)



TAPE SECTIONS		
SECTION	SYM	SIZE
TRAILER	T	20 pockets (MIN)
COMPONENT	C	4000 components
LEADER	L	50 pockets (MIN)

Figure 7.4 28-Pin Package Tape Length and Part Quantity





DETAIL "A"

REEL DIMs for 12mm CARRIER TAPE			
PART	FEATURE	SYM	SIZE (mm)
FLANGE	DIAMETER	D	330 (+0.25/-4.00)
	SPACE between FLANGES	W1	12.4 (+2.0/-0.0)
	OVERALL WITH	W2	18.4 (MAX)
	MIN SPACE "W1" AT FLANGE EDGE	W3	12.3 (MIN)
HUB	OUTER DIAMETER	D1	102 REF
	KEY SLIT DIAMETER	D2	20.2 (MIN)
	ARBOR HOLE DIAMETER	D3	13.0 (+0.5/-0.2)
	KEY SLIT WIDTH	B	2.0 (±0.5)

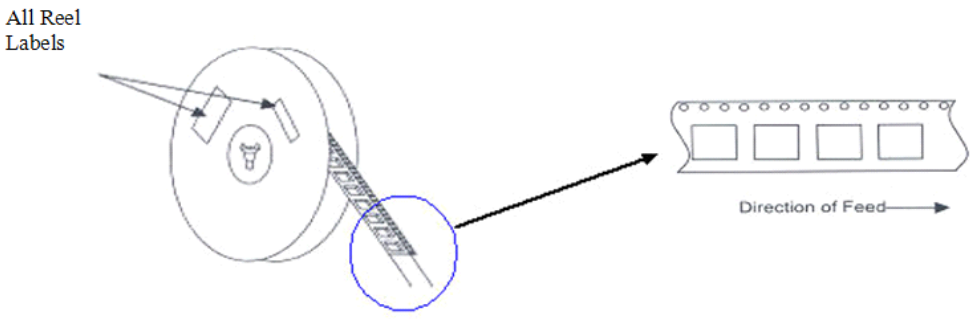


Figure 7.5 Package Reel Specifications