NEC

MOS FIELD EFFECT TRANSISTOR

NP110N055PUG

SWITCHING
N-CHANNEL POWER MOS FET

DESCRIPTION

The NP110N055PUG is N-channel MOS Field Effect Transistor designed for high current switching applications.

ORDERING INFORMATION

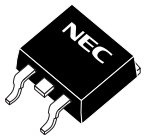
PART NUMBER	PACKAGE
NP110N055PUG	TO-263 (MP-25ZP)

FEATURES

- Channel temperature 175 degree rating
- Super low on-state resistance

  $R_{DS(on)}$ = 2.8 mΩ MAX. (V_{GS} = 10 V, I_D = 55 A)
- Low C_{iss}: C_{iss} = 16300 pF TYP.

(TO-263)



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	55	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±20	V
Drain Current (DC) (T_C = 25°C)	$I_{D(DC)}$	±110	A
Drain Current (Pulse) Note1	$I_{D(pulse)}$	±440	A
Total Power Dissipation (T_A = 25°C)	P_{T1}	1.8	W
Total Power Dissipation (T_C = 25°C)	P_{T2}	288	W
Channel Temperature	T_{ch}	175	°C
Storage Temperature	T_{stg}	–55 to +175	°C
Repetitive Avalanche Current Note2	I_{AR}	T.B.D.	A
Repetitive Avalanche Energy Note2	E_{AR}	T.B.D.	MJ

Notes 1. PW ≤ 10 μs, Duty cycle ≤ 1%

2. Starting T_{ch} = 25°C, V_{DD} = 28 V, R_G = 25 Ω , V_{GS} = 20 → 0 V

THERMAL RESISTANCE

Channel to Case Thermal Resistance	$R_{th(ch-C)}$	0.52	°C/W
Channel to Ambient Thermal Resistance	$R_{th(ch-A)}$	83.3	°C/W

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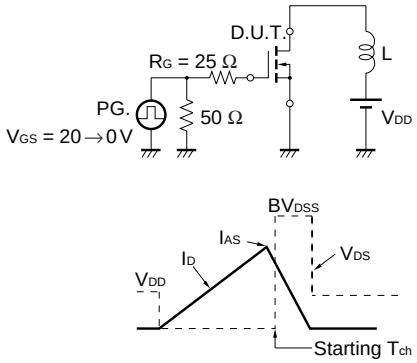
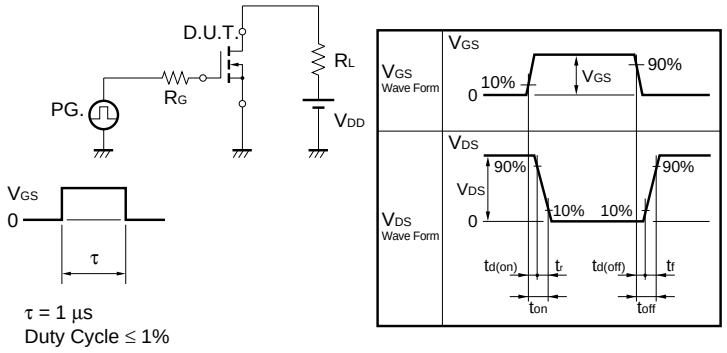
ELECTRICAL CHARACTERISTICS (T_A = 25°C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 55 V, V_{GS} = 0 V			10	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
Gate to Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	2.0	3.0	4.0	V
Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS} = 10 V, I_D = 55 A	T.B.D.			S
Drain to Source On-state Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 55 A		2.0	2.8	mΩ
Input Capacitance	C_{iss}	V_{DS} = 25 V		16300		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		1400		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		800		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 28 V		T.B.D.		ns
Rise Time	t_r	I_D = 55 A		T.B.D.		ns
Turn-off Delay Time	$t_{d(off)}$	V_{GS} = 10 V		T.B.D.		ns
Fall Time	t_f	R_G = 0 Ω		T.B.D.		ns
Total Gate Charge	Q_G	V_{DD} = 44V		T.B.D.		nC
Gate to Source Charge	Q_{GS}	V_{GS} = 10 V		T.B.D.		nC
Gate to Drain Charge	Q_{GD}	I_D = 110 A		T.B.D.		nC
Body Diode Forward Voltage	$V_{F(S-D)}$	I_F = 110 A, V_{GS} = 0 V		1.0	1.5	V
Reverse Recovery Time	t_{rr}	I_F = 110 A, V_{GS} = 0 V		T.B.D.		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/μs		T.B.D.		nC

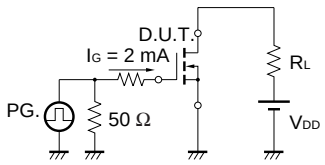
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME



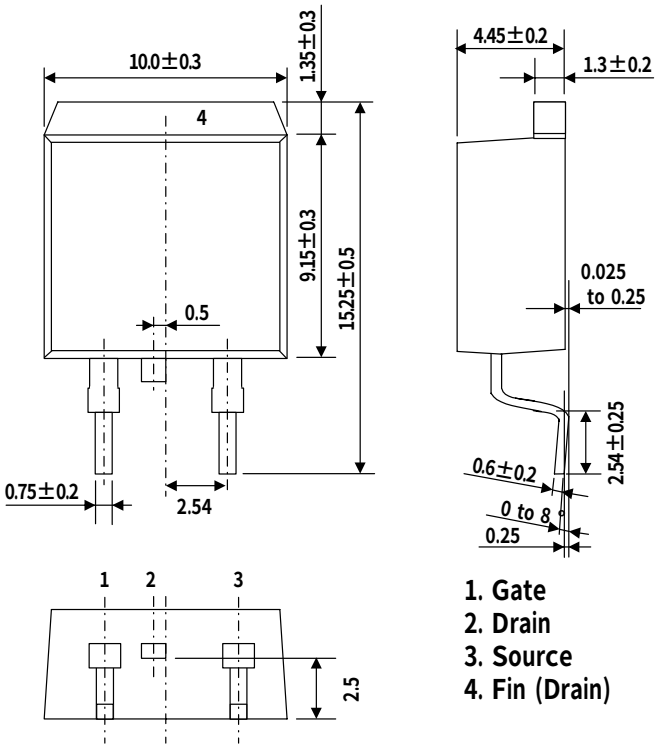
TEST CIRCUIT 3 GATE CHARGE



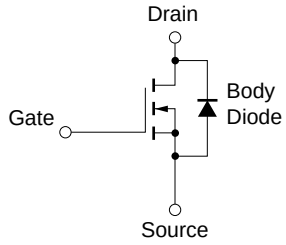
PACKAGE DRAWING (Unit: mm)

TO-263 (MP-25ZP)

Note; This drawing is tentative version



EQUIVALENT CIRCUIT



Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

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