

Features

- 10-Bit Resolution.
- 5MHz Sampling Rate.
- Internal S/H Function.
- Signal 5V Power Supply.
- V_{IN} Input Range : 0V to AV_{DD} .
- V_{REF} DC Range : 1V to AV_{DD} .
- Low Power : 175mW.
- Three – State Digital Outputs.
- Latch – Up Free

Applications

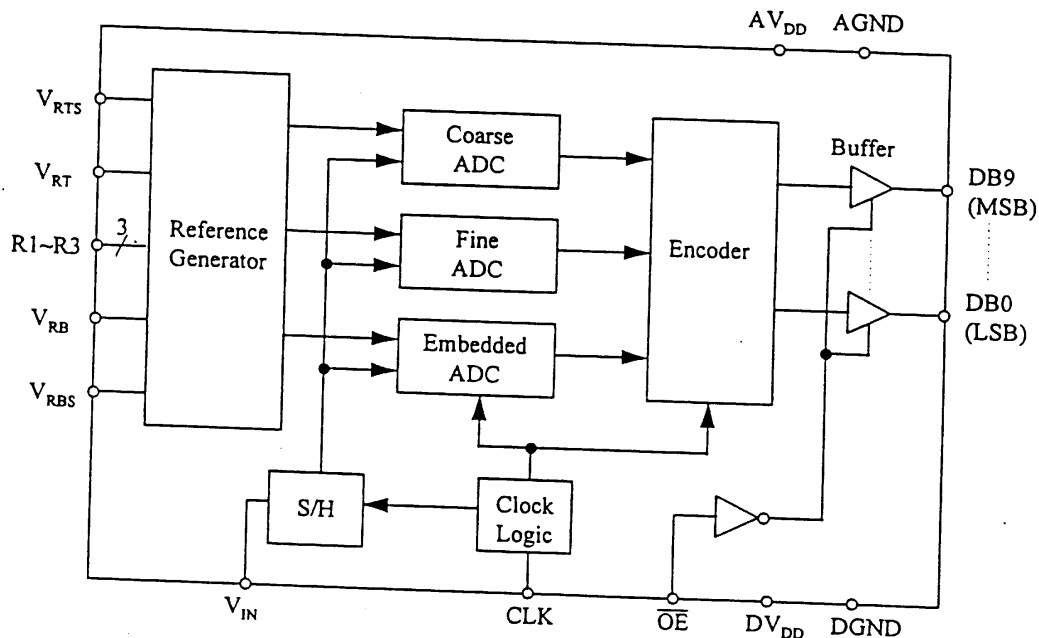
- Scanner

DESCRIPTION

The ES52099 is a 10 bit , 5MSPS, Analog to Digital Converter for applications that require high speed and high accuracy. Designed with advanced 5V CMOS process, this device offers excellent performance. Low power consumption and latch-up free operation.

The ES 52099 maintains low power consumption at high conversion rates with subranging architecture, and the comparator design achieves a low analog input capacitance. The input circuitry of the input circuitry of the ES52099 includes an on-chip S/H function that allows this part to digitize analog input signals between AGND and AV_{DD} .

Block Diagram



The ES52099 has been patented at R.O.C. and the patent number is 076864.

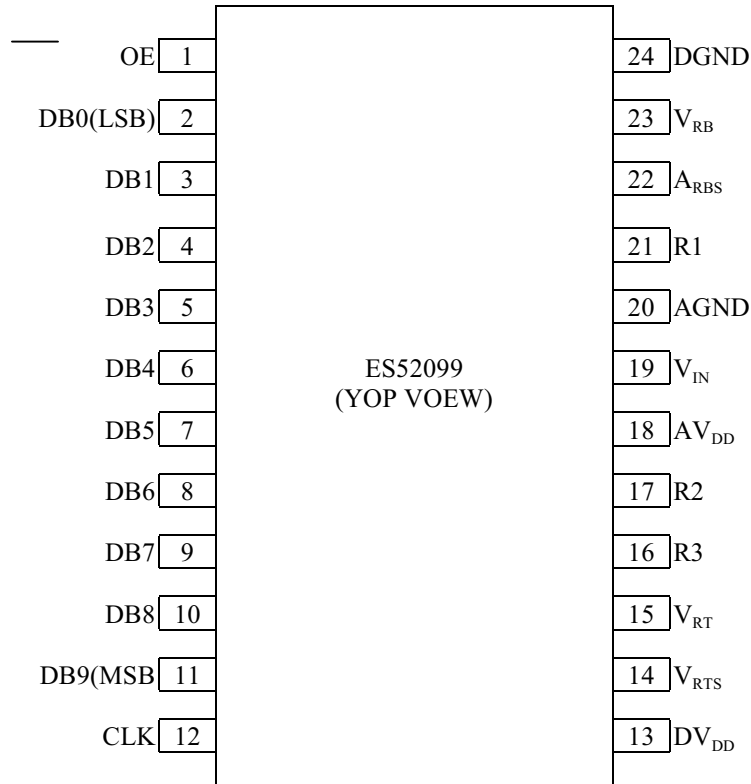
Absolute Maximum Rating ($T_A = 25^{\circ}\text{C}$ unless otherwise noted)

Supply voltage(V_{DD})-----	7V
Reference voltage(V_{RT}, V_{RB}) -----	$V_{DD}+0.5\sim\text{GND}-0.5\text{V}$
Analog input voltage(V_{IN}) -----	$V_{DD}+0.5\sim\text{GND}-0.5\text{V}$
All input voltage(CLK) -----	$V_{DD}+0.5\sim\text{GND}-0.5\text{V}$
All output voltage(V_{OH}, V_{OL})-----	$V_{DD}+0.5\sim\text{GND}-0.5\text{V}$
Storage temperature(T_{STG}) -----	$-65\sim+150^{\circ}\text{C}$
Lead Temperature(Soldering 10 Seconds) -----	300°C

Recommended Operating Conditions

Supply voltage	AV_{DD}, AV_{SS}	4.75 to 5.25	V
	DV_{DD}, AV_{SS}	4.75 to 5.25	V
	DGND-AGND	0 to 100	mV
Reference input voltage	V_{RB}	0 and above	V
	V_{RT}	AV_{DD} and below	V
	$V_{RT} - V_{RB}$	1.0 to V_{DD}	V
Analog input voltage	V_{IN}	V_{RB} to V_{RT}	V

PIN Assignment



Pin Description

Pin NO.	Symbol	Description	Pin NO.	Symbol	Description
1	OE	Output Enable	13	DV _{DD}	Digital Power Supply
2	DB0	Data Ouptput Bit 0 (LSB)	14	V _{RTS}	Top Internal Reference
3	DB1	Data Ouptut Bit 1	15	V _{RT}	Top Internal Reference
4	DB2	Data Ouptut Bit 2	16	R3	3/4 Reference Tap Point
5	DB3	Data Ouptut Bit 3	17	R2	1/2 Reference Tap Point
6	DB4	Data Ouptut Bit 4	18	AV _{DD}	Analog Power Supply
7	DB5	Data Ouptut Bit 5	19	V _{IN}	Analog Input Voltage
8	DB6	Data Ouptut Bit 6	20	AGND	Analog Ground
9	DB7	Data Ouptut Bit 7	21	R1	1/4 Reference Tap Point
10	DB8	Data Ouptut Bit 8	22	V _{RBS}	Bottom Internal Reference
11	DB9	Data Ouptut Bit 9(MSB)	23	V _{RB}	Bottom of Reference
12	CLK	Clock Input	24	DGND	Digital Ground

Electrical Characteristics

Unless Otherwise Specified :

$$AV_{DD} = DV_{DD} = 5^{\circ}\text{C} \text{ , } F_s = 5\text{MSPS}(50\% \text{ Duty Cycle}) \text{ , } V_{RT} = 4.0\text{V} \text{ , } V_{RB} = 1.0\text{V} \text{ , } T_A = 25^{\circ}\text{C}$$

Characteristic	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Key Features						
Resolution			10			Bits
Sampling Rate	Fs				5	MHz
Digital Outputs						
Logical"1"Current	I _{OH}	V _{OH} = 4.5V	3.5			mA
Logical"0"Current	I _{OL}	V _{OH} = 0.5V	3.5			mA
Tristate Leakage	I _{OZ}	V _{OUT} = DGND to DV _{DD}		10		μ A
Data Valid Delay	T _{OL}			40		ns
Data Enalb Delay	t _{OL}			25		ns
Data Tristate Delay	T _{DHZ}			25		ns
Digital Inputs						
Logical"1"Voltage	V _{IH}		4			V
Logical"0"Voltage	V _{IL}				1	V
DC Leakage Current	I _{IN}	V _{IN} = DGND to DV _{DD}				
CLK				5		μ A
$\overline{\text{OE}}$				15		μ A
Input Capacitance				5		pF
Clock Timing						
Clock Period	1/Fs		200			ns
Rise & Fall Time	tR,tF			5		ns
“High”Pulse Width	t _{PWH}			100		ns
“LOW”Pulse Width	t _{PWH}			100		ns
Duty Cycle				50		%

Electrical Characteristics

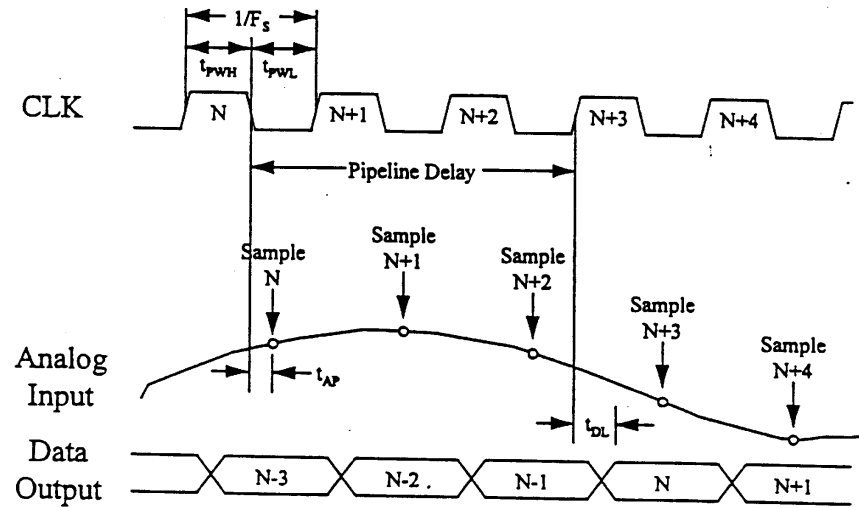
Unless Otherwise Specified:

$AV_{DD} = DV_{DD} = 5V$, $FS = 5MHz(50\% \text{ Duty Cycle})$, $V_{RT} = 4.0V$, $V_{RB} = 1.0V$, $T_A = 25^{\circ}C$

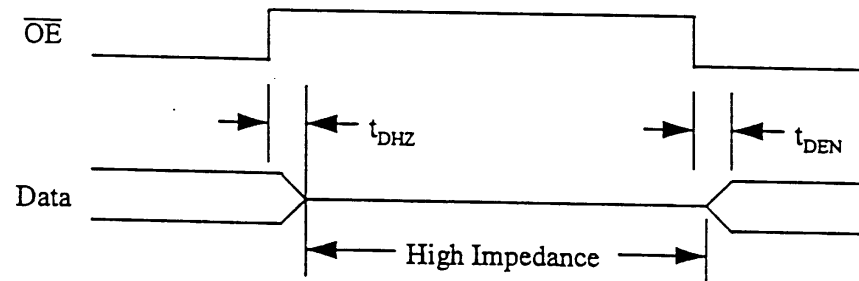
Characteristic	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Reference Voltage						
Positive Ref. Voltage	V _{RT}				AV _{DD}	V
Negative Ref. Voltage	V _{RB}		AGND			V
DifferentialRef. Voltage	V _{REF}	V _{REF} = V _{RT} -V _{RB}	1.0		AV _{DD}	V
Ladder Resistance	R _L				375	Ω
Ladder Temp. Coefficient	R _{TCO}				2000	Ppm/°C
Top Internal Reference	V _{RTS}	V _{RTS} Connected to V _{RTS}		4		V
Bottom Internal Refence	V _{RBS}	V _{RB} Connected to V _{RTS}		1		V
Accuracy						
Differential Non-linearity	DNL				±0.8	LSB
Integral Non-linearity	INL		-1		+4	LSB
Zero Scale Offset Error	E _{OB}			-20		mV
Full Scale Offset Error	E _{OT}			-40		mV
Power Supplies						
Operating Voltage (AV _{DD} , DV _{DD})	V _{DD}				5	V
Current(AV _{DD} , DV _{DD})	I _{DD}			35	40	mA
Analog Input						
Input Voltage Range	V _{IN}		V _{RB}		V _{RT}	V
Input Capacitance Sample	C _{IN}			25		pF
Input Capacitance Convert				5		pF
Aperture Delay	t _{AP}			25		ns
Aperture Uncertainty(jitter)	T _{AJ}			50		ps



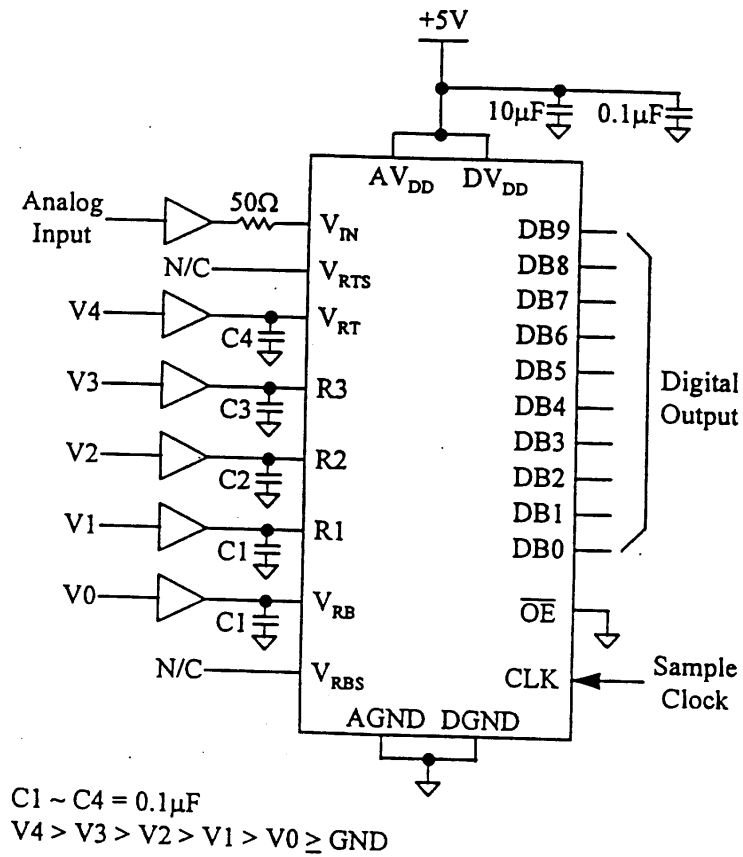
Timing Diagram



Tri-State Timing Diagram



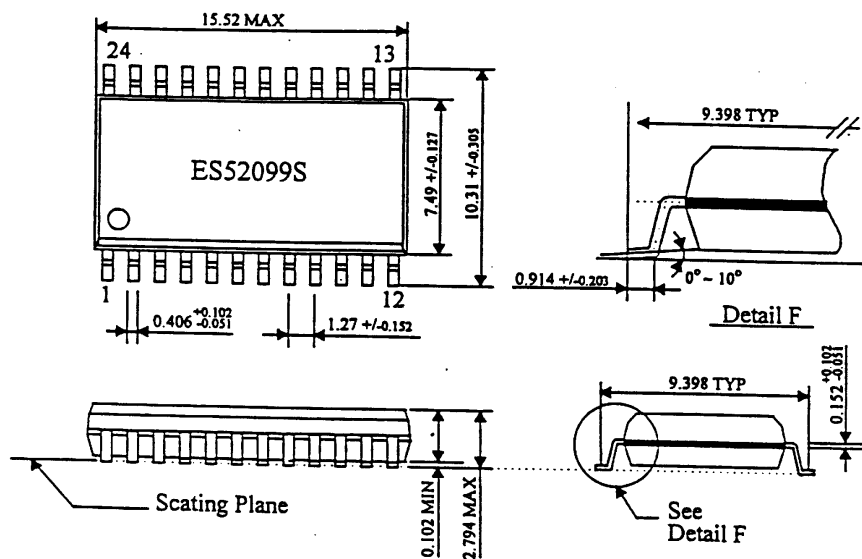
Application Circuit





Package Outline Unit: mm

ES52099S 24-pin SOP N.B. (Plastic)



ES52099E 24-pin SKINNY DIP (Plastic)

