CY2SSTV857-32

Differential Clock Buffer/Driver DDR400/PC3200-Compliant

Features

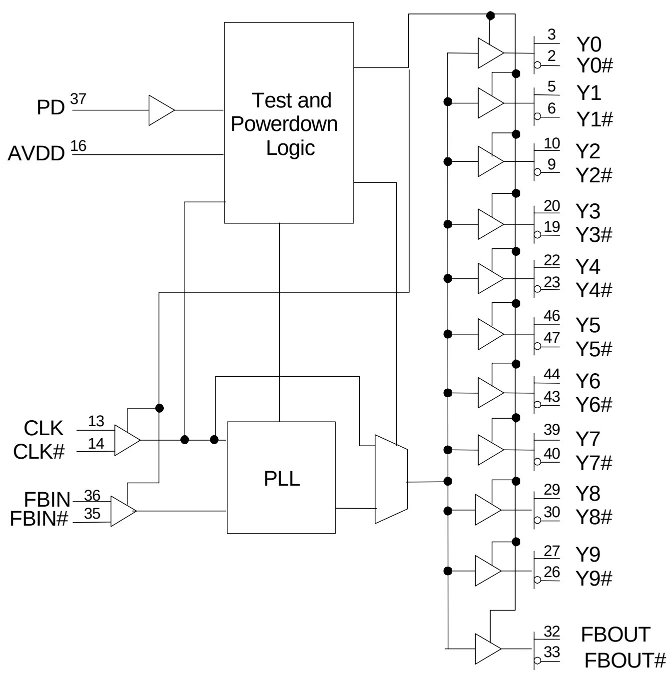
- **Operating frequency: 60 MHz to 230 MHz**
- **Supports 400 MHz DDR SDRAM**
- **10 differential outputs from one differential input**
- **Spread-Spectrum-compatible**
- **Low jitter (cycle-to-cycle): < 75**
- **Very low skew: < 100 ps**
- **Power management control input**
- **High-impedance outputs when input clock < 20 MHz**
- **2.6V operation**
- **Pin-compatible with CDC857-2 and -3**
- **48-pin TSSOP and 40 QFN package**
- **Industrial temperature of –40°C to 85°C**
- **Conforms to JEDEC DDR specification**

Description

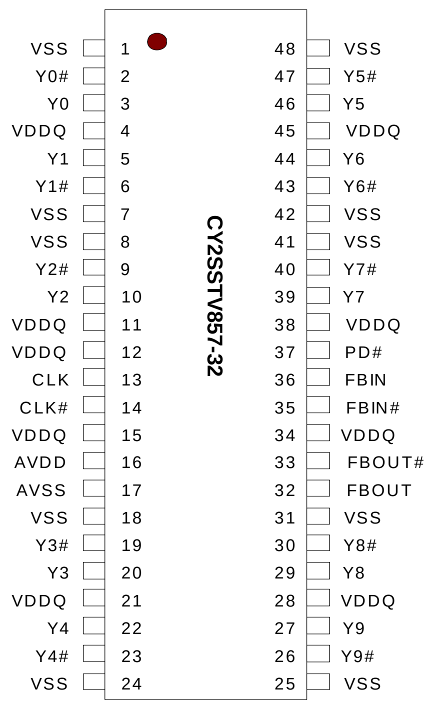
The CY2SSTV857-32 is a high-performance, low-skew, low-jitter zero-delay buffer designed to distribute differential clocks in high-speed applications. The CY2SSTV857-32 generates ten differential pair clock outputs from one differential pair clock input. In addition, the CY2SSTV857-32 features differential feedback clock outpts and inputs. This allows the CY2SSTV857-32 to be used as a zero delay buffer.

When used as a zero delay buffer in nested clock trees, the CY2SSTV857-32 locks onto the input reference and translates with near-zero delay to low-skew outputs.

Block Diagram



Pin Configuration



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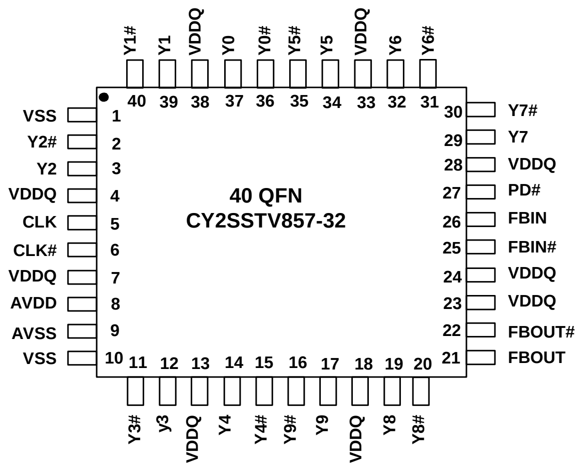
40 QFN Package



Pin Description

Pin # 48 TSSOP	Pin # 40 QFN	Pin Name	I/O[1]	Pin Description	Electrical Characteristics
13, 14	5,6	CLK, CLK#	I	**Differential Clock Input**.	LV Differential Input
35	25	FBIN#	I	**Feedback Clock Input**. Connect to FBOUT# for accessing the PLL.	Differential Input
36	26	FBIN	I	**Feedback Clock Input**. Connect to FBOUT for accessing the PLL.	
3, 5, 10, 20, 22	37,39,3,12,14	Y(0:4)	O	**Clock Outputs**.	Differential Outputs
2, 6, 9, 19, 23	36,40,2,11,15	Y#(0:4)	O	**Clock Outputs**.	
27, 29, 39, 44, 46	17,19,29,32,34	Y(9:5)	O	**Clock Outputs**.	Differential Outputs
26, 30, 40, 43, 47	16,20,30,31,35	Y#(9:5)	O	**Clock Outputs**.	
32	21	FBOUT	O	**Feedback Clock Output**. Connect to FBIN for normal operation. A bypass delay capacitor at this output will control Input Reference/Output Clocks phase relationships.	Differential Outputs
33	22	FBOUT#	O	**Feedback Clock Output**. Connect to FBIN# for normal operation. A bypass delay capacitor at this output will control Input Reference/Output Clocks phase relationships.	
37	27	PD#	I	**Power Down Input**. When PD# is set HIGH, all Q and Q# outputs are enabled and switch at the same frequency as CLK. When set LOW, all Q and Q# outputs are disabled Hi-Z and the PLL is powered down.	
4, 11,12,15, 21, 28, 34, 38, 45	4,7,13,18,23,24, 28,33,38	VDDQ		**2.6V Power Supply for Output Clock Buffers**.	2.6V Nominal
16	8	AVDD		**2.6V Power Supply for PLL**. When VDDA is at GND, PLL is bypassed and CLK is buffered directly to the device outputs. During disable (PD# = 0), the PLL is powered down.	2.6V Nominal
1, 7, 8, 18, 24, 25, 31, 41, 42, 48	1,10	VSS		**Common Ground**.	0.0V Ground
17	9	AVSS		**Analog Ground**.	0.0V Analog Ground

Note:
1. A bypass capacitor (0.1µF) should be placed as close as possible to each positive power pin (<0.2"). If these bypass capacitors are not close to the pins, their high-frequency filtering characteristic will be cancelled by the lead inductance of the traces.

Zero Delay Buffer

When used as a zero delay buffer the CY2SSTV857-32 will likely be in a nested clock tree application. For these applications, the CY2SSTV857-32 offers a differential clock input pair as a PLL reference. The CY2SSTV857-32 then can lock onto the reference and translate with near zero delay to low-skew outputs. For normal operation, the external feedback input, FBIN, is connected to the feedback output, FBOUT. By connecting the feedback output to the feedback input the propagation delay through the device is eliminated. The PLL works to align the output edge with the input reference edge thus producing a near zero delay. The reference frequency affects the static phase offset of the PLL and thus the relative delay between the inputs and outputs.

When VDDA is strapped LOW, the PLL is turned off and bypassed for test purposes.

Power Management

Output enable/disable control of the CY2SSTV857-32 allows the user to implement power management schemes into the design. Outputs are three-stated/disabled when PD# is asserted LOW (see *Table 1*).

Table 1. Function Table

Inputs				Outputs				PLL
AVDD	**PD#**	**CLK**	**CLK#**	**Y**	**Y#**	**FBOUT**	**FBOUT#**	
GND	H	L	H	L	H	L	H	BYPASSED/OFF
GND	H	H	L	H	L	H	L	BYPASSED/OFF
X	L	L	H	Z	Z	Z	Z	Off
X	L	H	L	Z	Z	Z	Z	OFF
2.6V	H	L	H	L	H	L	H	On
2.6V	H	H	L	H	L	H	L	On
2.6V	H	< 20 MHz	< 20 MHz	Hi-Z	Hi-Z	Hi-Z	HI-Z	Off

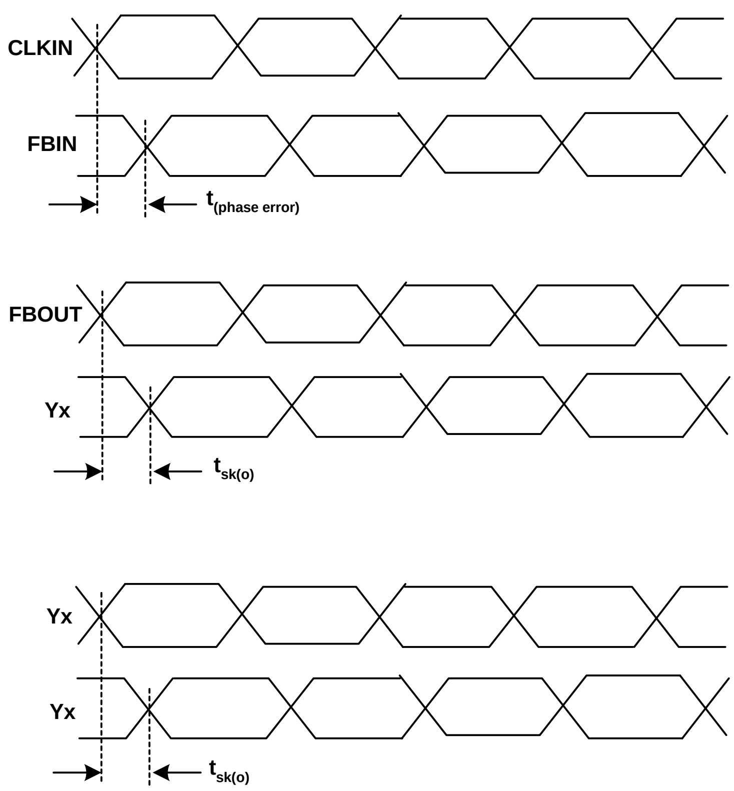


Figure 1. Phase Error and Skew Waveforms

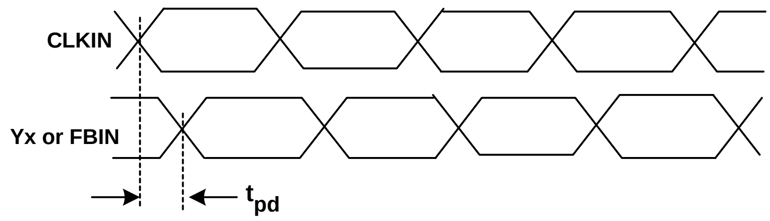


Figure 2. Propagation Delay Time t_{PLH}, t_{PHL}

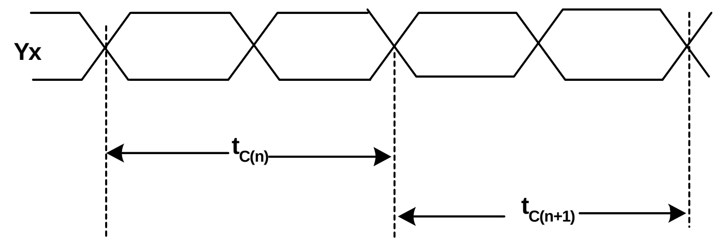
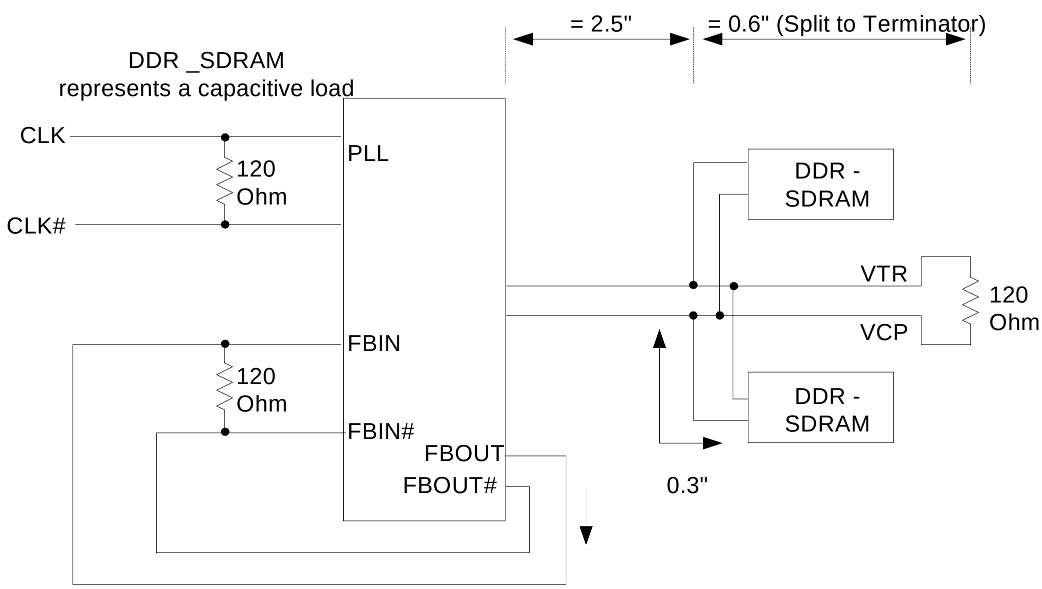
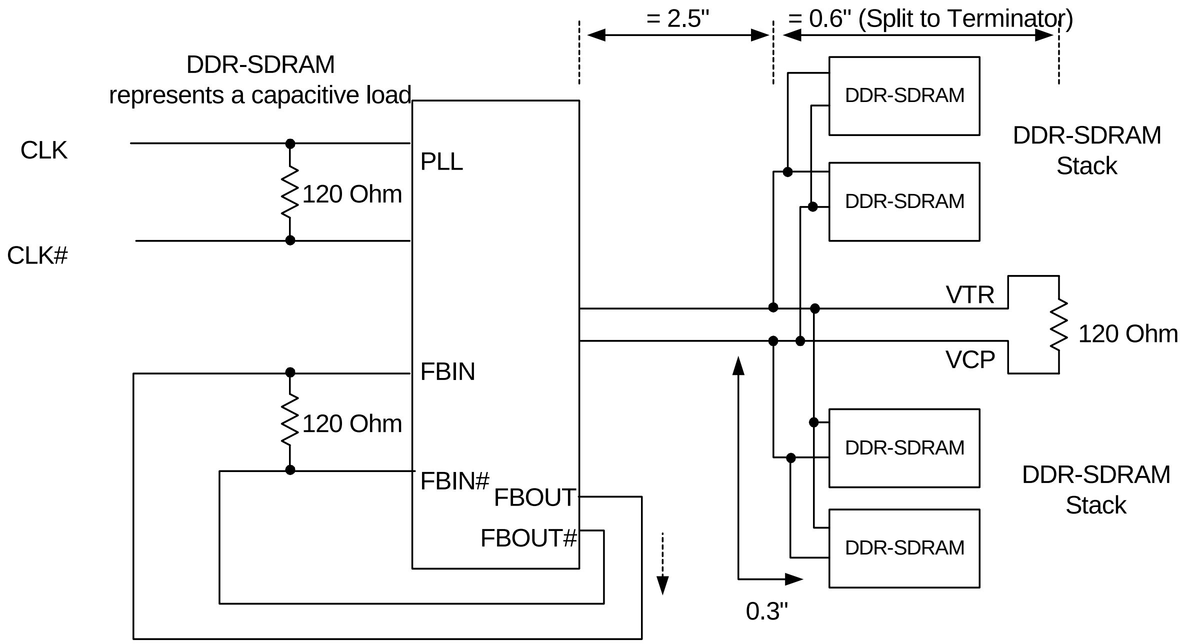


Figure 3. Cycle-to-cycle Jitter



Output load capacitance for 2 DDR-SDRAM Loads: 5 pF< CL< 8 pF

Figure 4. Clock Structure # 1



Output load capacitancce for 4 DDR-SDRAM Loads: 10 pF < CL < 16 pF

Figure 5. Clock Structure # 1

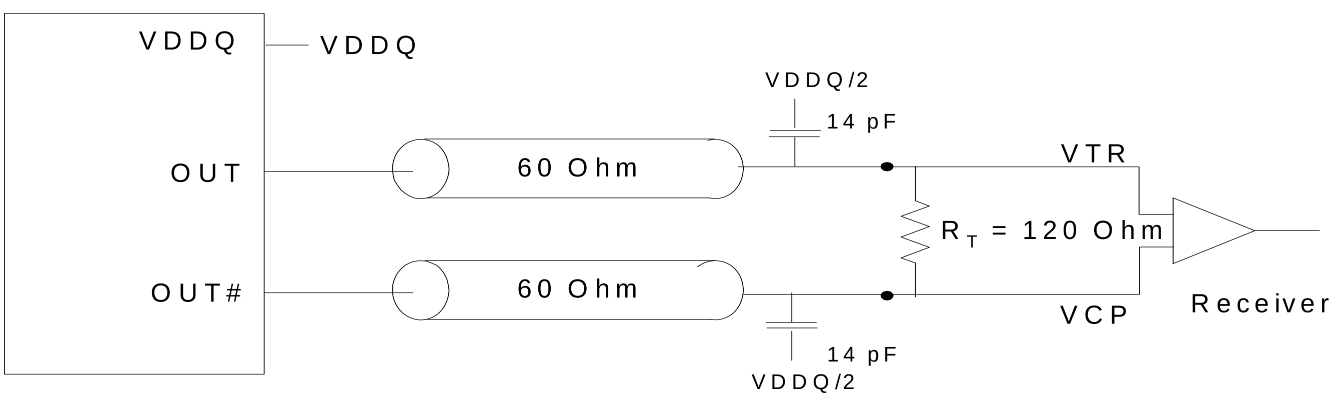


Figure 6. Differential Signal Using Direct Termination Resistor

Absolute Maximum Conditions[2]

Input Voltage Relative to V_{SS}: .... V_{SS} – 0.3V

Input Voltage Relative to V_{DDQ} or AV_{DD}: .... V_{DDQ} + 0.3V

Storage Temperature: .... –65°C to + 150°C

Operating Temperature: .... –40°C to +85°C

Maximum Power Supply: 3.5V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, V_{in} and V_{out} should be constrained to the range:

$V_{SS} < (V_{in}$ or $V_{out}) < V_{DDQ}$.

Unused inputs must always be tied to an appropriate logic voltage level (either V_{SS} or V_{DDQ}).

DC Electrical Specifications[3]

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
V_{DDQ}	Supply Voltage	Operating	2.375	–	2.625	V
V_{IL}	Input Low Voltage	PD#	–	–	0.3 × V_{DDQ}	V
V_{IH}	Input High Voltage		0.7 × V_{DDQ}	–	–	V
V_{ID}	Differential Input Voltage[4]	CLK, FBIN	0.36	–	V_{DDQ} + 0.6	V
V_{IX}	Differential Input Crossing Voltage[5]	CLK, FBIN	$(V_{DDQ}/2)$ – 0.2	$V_{DDQ}/2$	$(V_{DDQ}/2)$ + 0.2	V
I_{IN}	Input Current [CLK, FBIN, PD#]	V_{IN} = 0V or $V_{IN} = V_{DDQ}$	–10	–	10	µA
I_{OL}	Output Low Current	V_{DDQ} = 2.375V, V_{OUT} = 1.2V	26	35	–	mA
I_{OH}	Output High Current	V_{DDQ} = 2.375V, V_{OUT} = 1V	28	–32	–	mA
V_{OL}	Output Low Voltage	V_{DDQ}= 2.375V, I_{OL} = 12 mA	–	–	0.6	V
V_{OH}	Output High Voltage	V_{DDQ} = 2.375V, I_{OH} = –12 mA	1.7	–	–	V
V_{OUT}	Output Voltage Swing[6]		1.1	–	V_{DDQ} – 0.4	V
V_{OC}	Output Crossing Voltage[7]		$(V_{DDQ}/2)$ – 0.2	$V_{DDQ}/2$	$(V_{DDQ}/2)$ + 0.2	V
I_{OZ}	High-Impedance Output Current	V_O = GND or $V_O = V_{DDQ}$	–10	–	10	µA
I_{DDQ}	Dynamic Supply Current[8]	All V_{DDQ}, F_O = 200 MHz	–	235	300	mA
I_{DD}	PLL Supply Current	V_{DDA} only	–	9	12	mA
I_{DDS}	Standby Supply Current	PD# = 0 and CLK/CLK# = 0 MHz	–	–	100	µA
Cin	Input Pin Capacitance		2	–	3.5	pF

AC Electrical Specifications [9, 10]

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
f_{CLK}	Operating Clock Frequency	AV_{DD}, V_{DDQ} = 2.6V ± 0.1V	60	–	230	MHz
t_{DC}	Input Clock Duty Cycle		40	–	60	%
t_{LOCK}	Maximum PLL Lock Time		–	–	100	µs
D_{TYC}	Duty Cycle[11]	60 MHz to 100 MHz	49	50	51	%
		101 MHz to 170 MHz	48	–	52	%
tsl(o)	Output Clocks Slew Rate	20%–80% of VOD	1		2	V/ns
t_{PZL}, t_{PZH}	Output Enable Time[12] (all outputs)		–	3	25	ns
t_{PLZ}, t_{PHZ}	Output Disable Time[12] (all outputs)		–	3	8	ns

Notes:

2. Multiple Supplies: The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.
3. Unused inputs must be held HIGH or LOW to prevent them from floating.
4. Differential input signal voltage specifies the differential voltage VTR–VCPI required for switching, where VTR is the true input level and VCP is the complementary input level. See *Figure 6*.
5. Differential cross-point input voltage is expected to track V_{DDQ} and is the voltage at which the differential signal must be crossing.
6. For load conditions see *Figure 6*.
7. The value of VOC is expected to be (VTR + VCP)/2. In case of each clock directly terminated by a 120Ω resistor. See *Figure 6*.
8. All outputs switching load with 14 pF in 60Ω environment. See *Figure 6*.
9. Parameters are guaranteed by design and characterization. Not 100% tested in production.
10. PLL is capable of meeting the specified parameters while supporting SSC synthesizers with modulation frequency between 30 kHz and 50 kHz with a down spread or –0.5%.
11. While the pulse skew is almost constant over frequency, the duty cycle error increases at higher frequencies. This is due to the formula: duty cycle = t_{WHC}/t_C, where the cycle time(tC) decreases as the frequency goes up.
12. Refers to transition of non-inverting output.

AC Electrical Specifications (continued)[9, 10]

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
t_{CCJ}	Cycle to Cycle Jitter [10]	f > 66 MHz	–75	–	75	ps
tjit(h-per)	Half-period jitter[10, 13]	f > 66 MHz	–100	–	100	ps
t_{PLH}(t_{PD})	Low-to-High Propagation Delay, CLK to Y	Test Mode only	1.5	3.5	7.5	ns
t_{PHL}(t_{PD})	High-to-Low Propagation Delay, CLK to Y		1.5	3.5	7.5	ns
$t_{SK(O)}$	Any Output to Any Output Skew[14]		–	–	100	ps
t_{PHASE}	Phase Error[14]		–50	–	50	ps

Ordering Information

Part Number	Package Type	Product Flow
CY2SSTV857ZC–32	48-pin TSSOP	Commercial, 0° to 70°C
CY2SSTV857ZC–32T	48-pin TSSOP–Tape and Reel	Commercial, 0° to 70°C
CY2SSTV857LFC–32[15]	40-pin QFN	Commercial, 0° to 70°C
CY2SSTV857LFC–32T[15]	40-pin QFN–Tape and Reel	Commercial, 0° to 70°C
CY2SSTV857ZI–32	48-pin TSSOP	Industrial, –40° to 85°C
CY2SSTV857ZI–32T	48-pin TSSOP–Tape and Reel	Industrial, –40° to 85°C
CY2SSTV857LFI–32[15]	40-pin QFN	Industrial, –40° to 85°C
CY2SSTV857LFI–32T[15]	40-pin QFN–Tape and Reel	Industrial, –40° to 85°C
Lead-Free		
CY2SSTV857ZXC–32	48-pin TSSOP	Commercial, 0° to 70°C
CY2SSTV857ZXC–32T	48-pin TSSOP–Tape and Reel	Commercial, 0° to 70°C
CY2SSTV857LFXC–32[15]	40-pin QFN	Commercial, 0° to 70°C
CY2SSTV857LFXC–32T[15]	40-pin QFN–Tape and Reel	Commercial, 0° to 70°C
CY2SSTV857ZXI–32	48-pin TSSOP	Industrial, –40° to 85°C
CY2SSTV857ZXI–32T	48-pin TSSOP–Tape and Reel	Industrial, –40° to 85°C

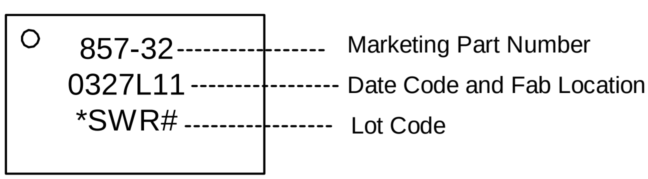
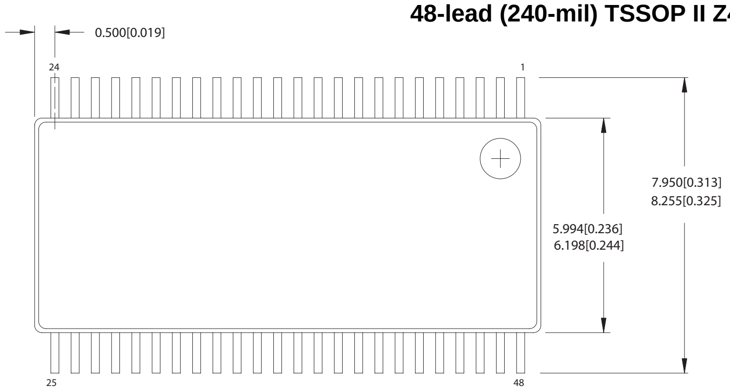


Figure 7. Actual Marking on the Device

Notes:
13. Period jitter and half-period jitter specifications are separate specifications that must be met independently of each other.
14. All differential input and output terminals are terminated with 120Ω/16 pF, as shown in *Figure 5*.
15. The ordering part number differs from the marking on the actual device. See *Figure 7* for the actual marking on the device.

Package Drawing and Dimension

48-lead (240-mil) TSSOP II Z4824

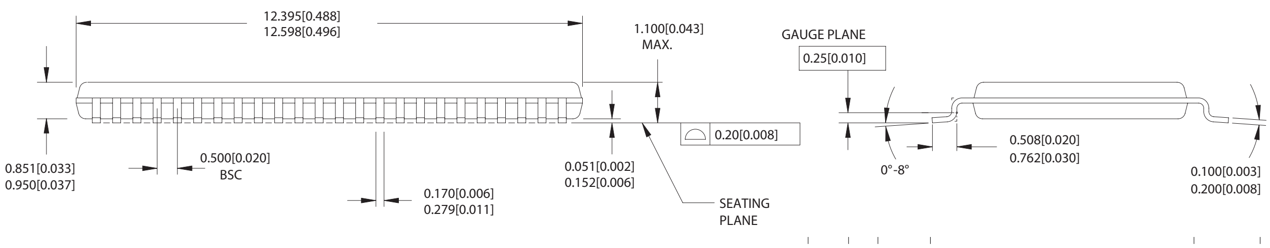


DIMENSIONS IN MM[INCHES] MIN.
MAX.

REFERENCE JEDEC MO-153

PACKAGE WEIGHT 0.33gms

PART #
Z4824 STANDARD PKG.
ZZ4824 LEAD FREE PKG.



DIMENSIONS IN MM[INCHES] MIN.
MAX.

REFERENCE JEDEC MO-220

40-lead QFN 6 x 6 MM LF40A