AKD4420-SC

AK4420 Evaluation Board Rev.2

General Description

AKD4420-SC is an evaluation board for AK4420 (192kHz sampling 24Bit Stereo ΔΣ DAC with 2Vrms Output). AKD4420-SC has a digital audio interface (AK4115) of Optical input and can easily achieve the interface with digital audio system. Therefore, it is easy to evaluate the sound quality of AK4420.

■ Ordering Guide

AKD4420-SC ---- AK4420 Evaluation Board

Function

☐ **On-board digital audio interface. (AK4115)**

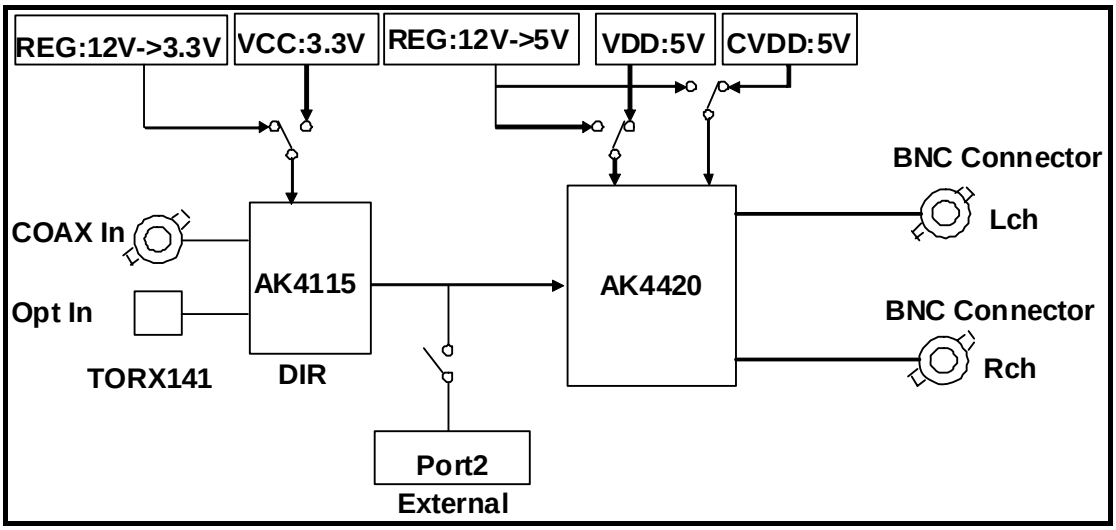


Figure 1. AKD4420-SC Block diagram
(* Circuit diagram are attached at the end of this manual.)

Board Outline Chart

■ Outline Chart

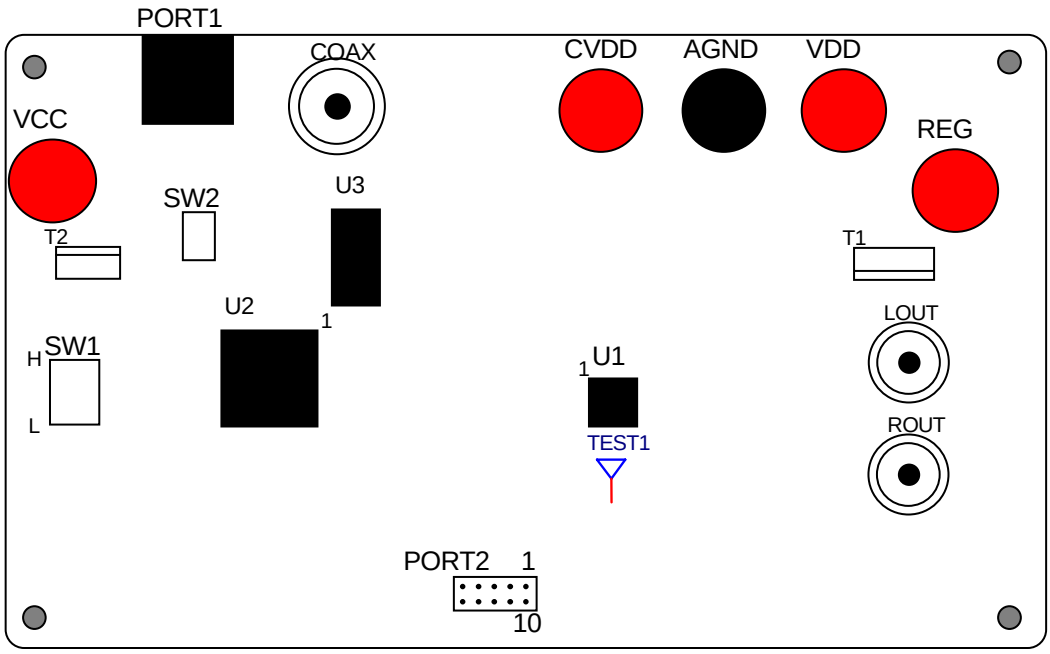


Figure 2. AKD4420-SC Outline Chart

■ Comment

(1) LOUT, ROUT (BNC-JACK)
It is analog signal output Jack. The signal is output from LOUT/ROUT pins.

(2) COAX, PORT1, PORT2 (Digital signal connector)
COAX (BNC-JACK): Digital signal (SPDIF, Fs: 24～48kHz) is input to the AK4115. (Default)
PORT1 (Optical Connecter): Optical digital signal (SPDIF, Fs: 32～48kHz) is input to the AK4115.
PORT2 (10 pin header): The clock and data can be input and output with this connector.

(3) REG, VDD, AGND, CVDD, VCC
These are the power supply connectors. Connect power supply with these pins.
As for the detail comments, refer to the setup of power supply in P3.

(4) SW1, SW2 (Switch)
SW1: Setting of frequency of MCKO that is output from AK4115.
SW2: Reset of AK4115. Keep “H” during normal operation.

■ Operation sequence

1) Set up the power supply lines.
Each supply line should be distributed from the power supply unit.

Name of jack	Color of jack	Typ Voltage	Voltage Range	Using	Default Setting
VCC1 (Note 1)	Red	+12V	+7~+15V	AVDD, DVDD, TVDD, OVDD of AK4115 and VCC of Logic circuit (Regulator:T2)	Connected to +12V
VDD1	Red	+5V	+4.5~+5.5V	VDD of AK4420	Connected to +5V
CVDD1	Red	+5V	+4.5~+5.5V	CVDD of AK4420	Connected to +5V
AGND2	Black	0V	0V	Ground	Connected to GND (Should be connected)
REG (Note 2)	Red	+12V	+7V~+15V	VDD, CVDD of AK4420 (Regulator:T1)	Open

Table 1.Set up of power supply lines

Note 1) In case of using +3.3V power supply to connect VCC1, It is possible to supply the voltage to AK4115 and the Logic circuit without using Regulator.
In this case, change to R36: Open→ Short (0Ω); R34,R35: Short (0Ω) → Open

Note 2) In case of using +12V power supply to connect REG, Use regulator: T1 can supply AK4420 with clean voltage.
In this case, change to R25,R44: Short (0Ω)→ Open; R37,R43:Open→ Short (0Ω); VDD, CVDD should be open.

2) DIP Switch setting:
Refer to Table 2 and Table 3

3) Power Down:
The AK4115 should be reset once by bringing SW2 (AK4115 PDN) “L” upon power-up.

■ Evaluation mode

1. Using DIR (Optical Link)
The DIR generates MCLK, BICK, LRCK and SDATA from the received data through optical connector (PORT1: TORX141). It is possible to evaluate the AK4420 by using CD disk.
Setting: R19: Open →470Ω; R33: short (0Ω)→Open

2. Using DIR (COAX) (Default)
The DIR generates MCLK, BICK, LRCK and SDATA from the received data through BNC connector (J3). It is possible to evaluate the AK4420 by using CD disk.
Setting: R19: Open; R33: short (0Ω); (Default)
＊ COAX is recommended for an evaluation of the Sound quality.

3. Supply all interface signals that includ master clock via PORT2 from external equipments..
Setting: R11: 5.1Ω→Open
R12, R13, R14: 51Ω→Open
R15, R16, R17, R18: Open→51Ω or short (0Ω)

Note) The above work of removing (open) or shorting resistors need to modify the connection by soldering.

■ Setting of DIP switch

[SW1]: AK4115 setting

No.	Pin	OFF ("L")	ON ("H")	Default の状態
1	OCKS0	AK4115's Master Clock setting Look Table 3		OFF
2	OCKS1			ON

Table 2. SW1 setting

OCKS1	OCKS0	MCLK Frequency	
0	0/1	256fs @ fs=96kHz	
1	0	512fs @ fs=48kHz	Default
1	1	128fs @ fs=192kHz	

Table 3. MCLK clock setting

■ Setting of SW2 switch

[SW2](PDN): Reset of AK4115. Keep "H" during normal operation.

Measurement Results

[Measurement condition]

- Measurement unit : Audio Precision System two Cascade (AP2)
- MCLK : 512fs, 256fs, 128fs
- BICK : 64fs
- fs : 44.1kHz, 96kHz, 192kHz
- Bit : 24bit
- Power Supply : VDD=CVDD=5V
- Interface : DIR
- Temperature : Room

Table Data

fs=44.1kHz

Parameter	Input signal	Measurement filter	Lch	Rch
S/(N+D)	1kHz, 0dB	20kLPF	92.3	92.3
DR	1kHz, -60dB	20kLPF, A-weighted	105.1	105.1
S/N	"0" data	20kLPF, A-weighted	106.0	105.7

fs=96kHz

Parameter	Input signal	Measurement filter	Lch	Rch
S/(N+D)	1kHz, 0dB	40kLPF	92.2	92.2
DR	1kHz, -60dB	40kLPF, A-weighted	105.7	105.3
S/N	"0" data	40kLPF, A-weighted	105.9	105.7

fs=192kHz

Parameter	Input signal	Measurement filter	Lch	Rch
S/(N+D)	1kHz, 0dB	40kLPF	93.0	92.8
DR	1kHz, -60dB	40kLPF, A-weighted	105.2	105.1
S/N	"0" data	40kLPF, A-weighted	105.4	105.3

Plot Data

(fs=44.1kHz)

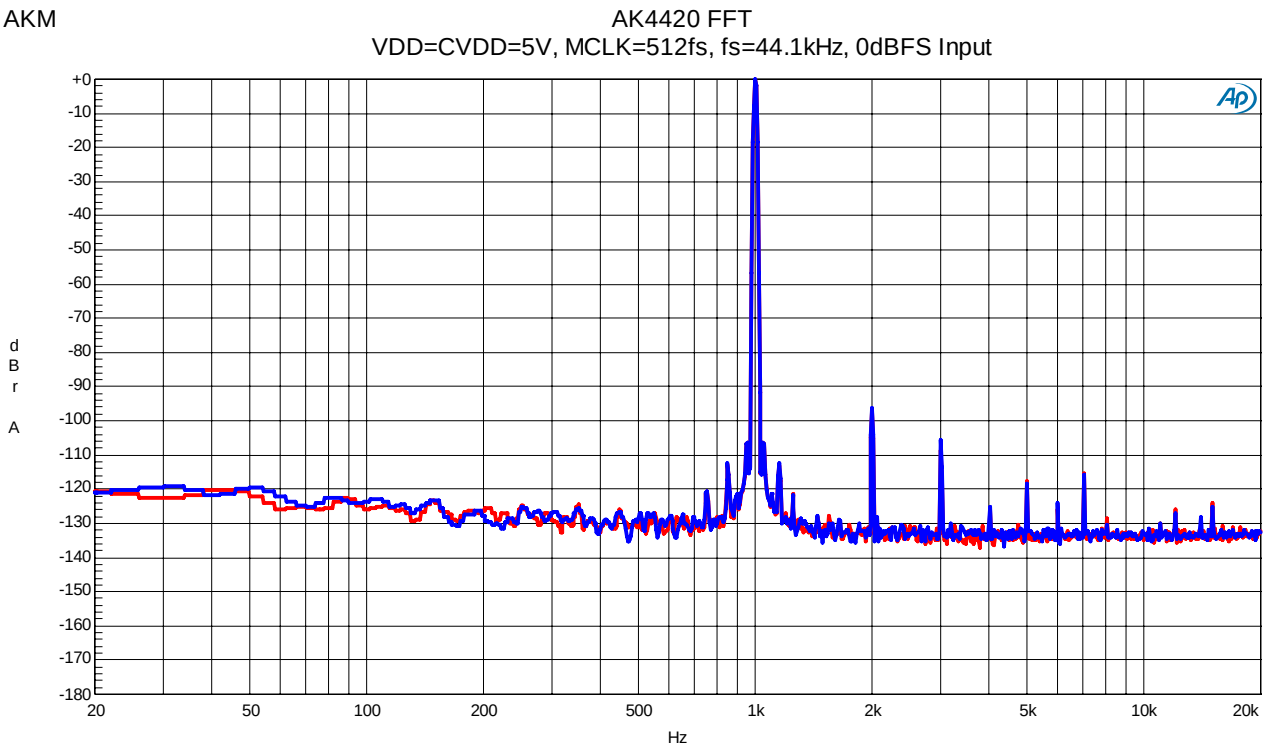


Figure 2. FFT (0dB)

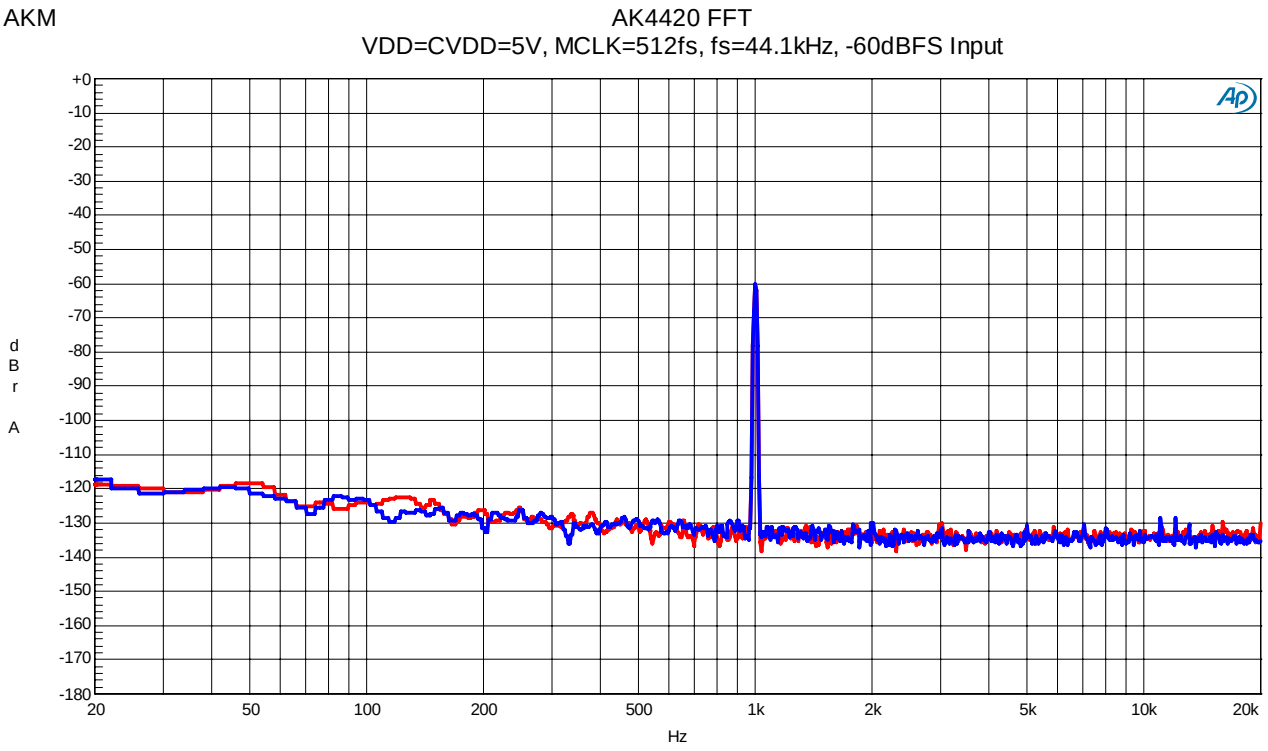


Figure 3. FFT (-60dB)

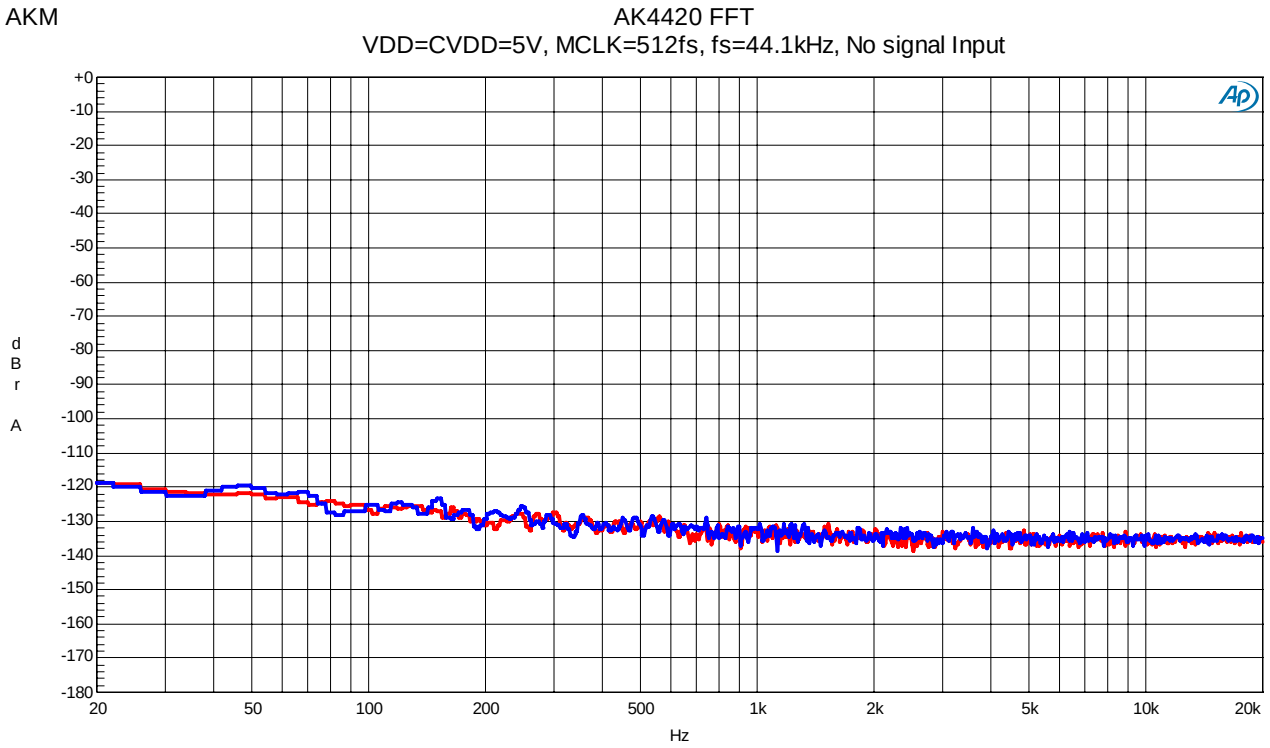


Figure 4. FFT (No Signal)

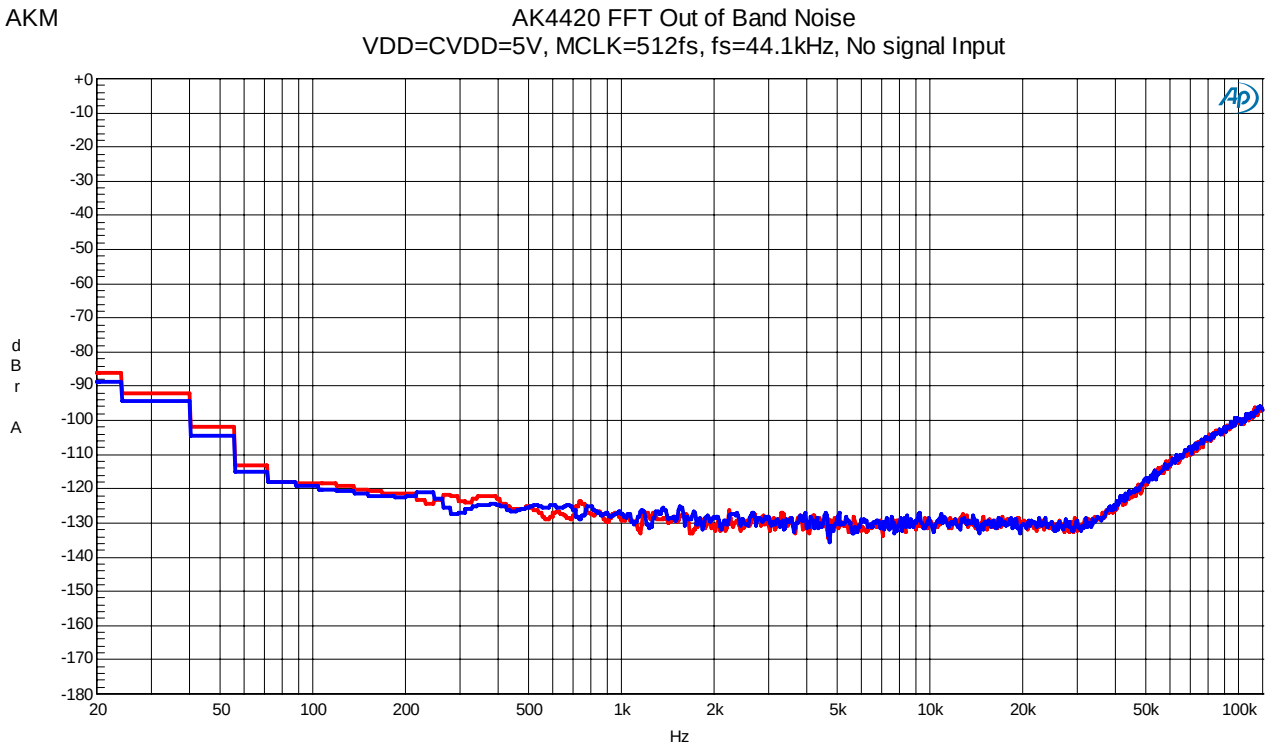


Figure 5. FFT (Out of Band Noise)

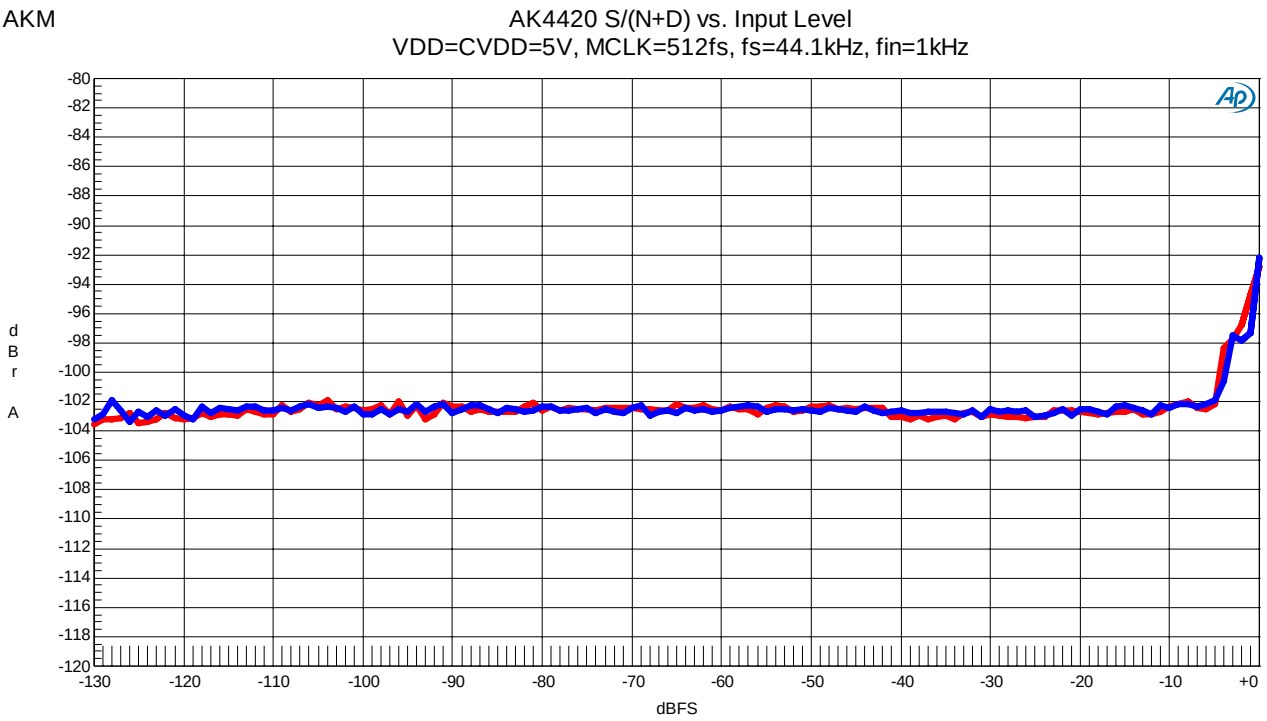


Figure 6. S/(N+D) vs. Input Level

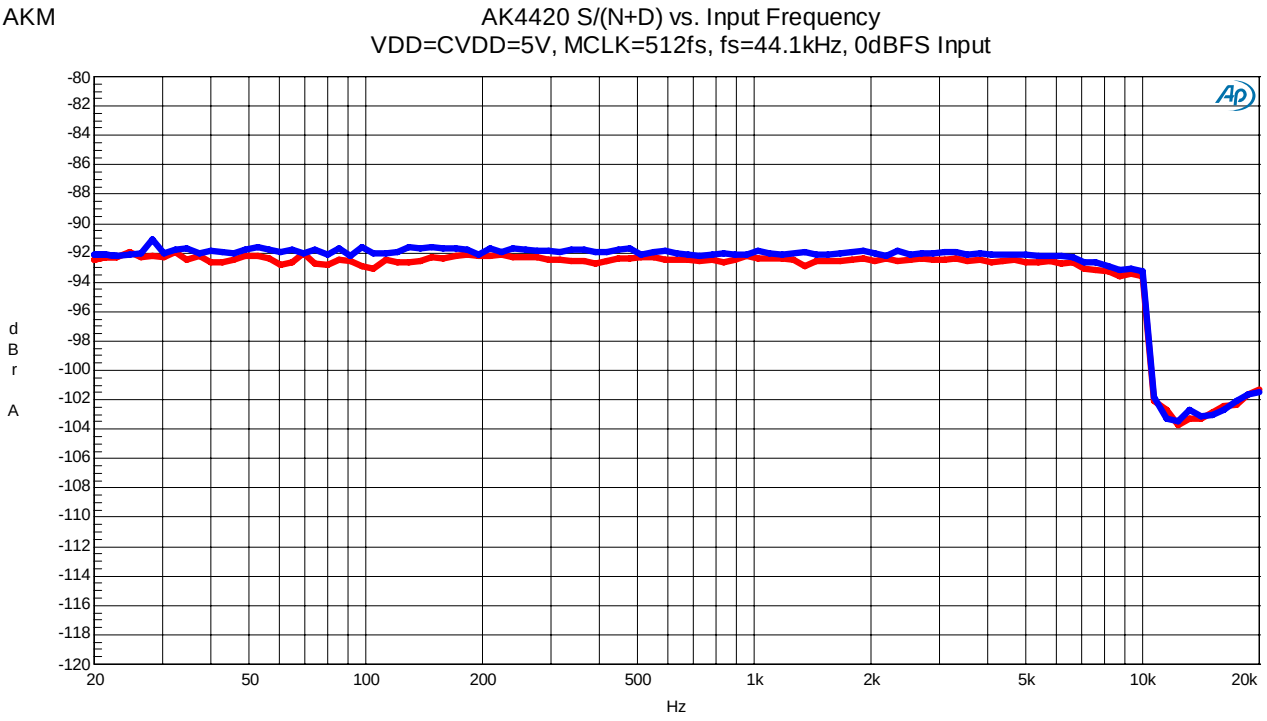


Figure 7. S/(N+D) vs. Input Frequency

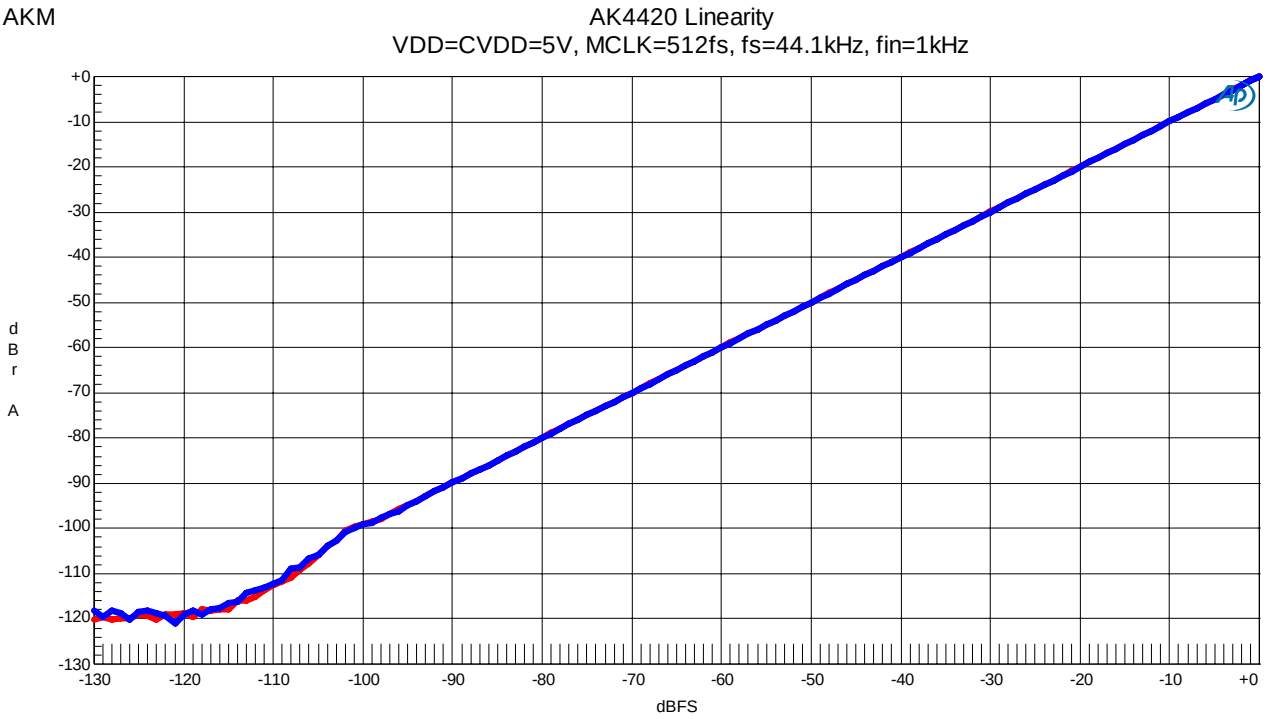


Figure 8. Linearity

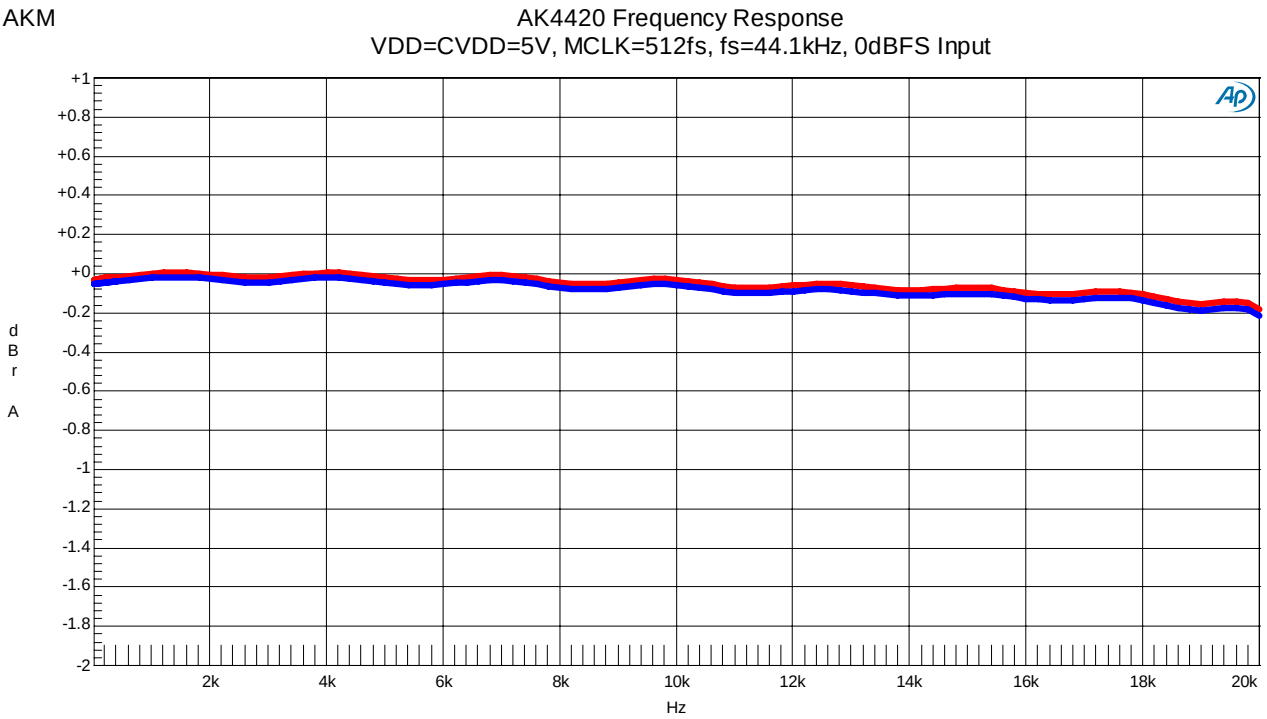


Figure 9. Frequency Response

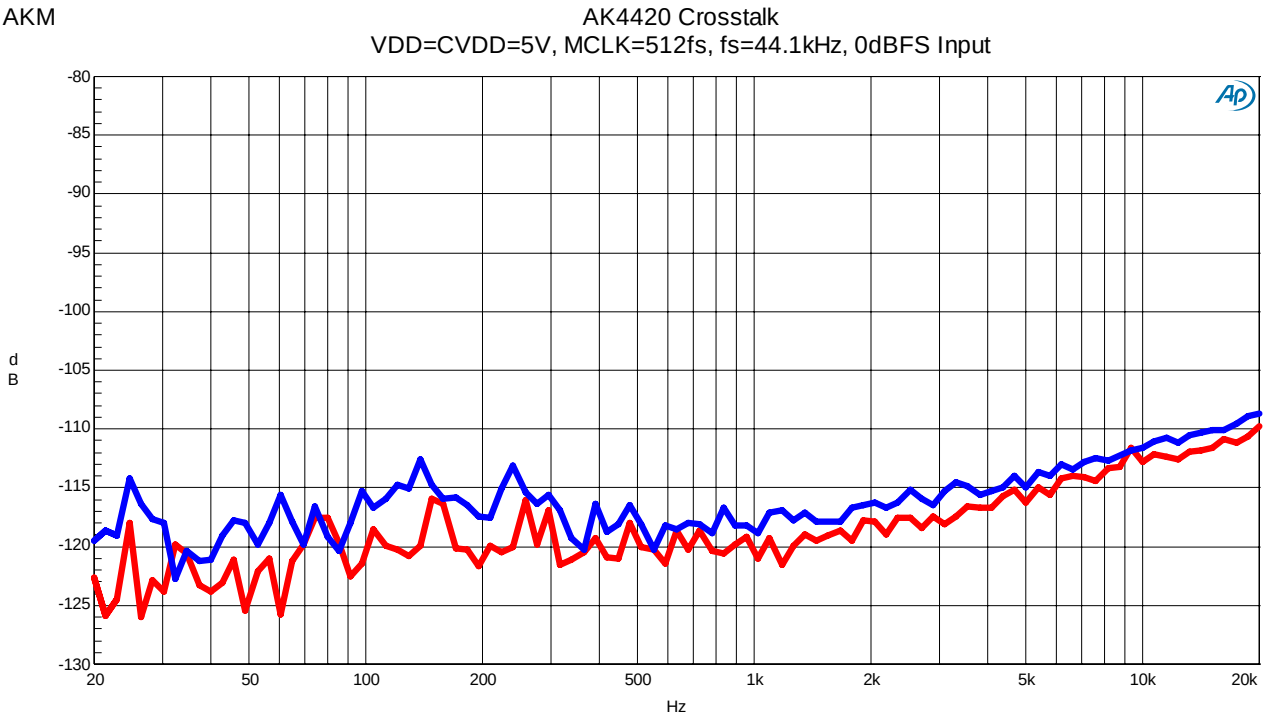


Figure 10. Crosstalk

(fs=96kHz)

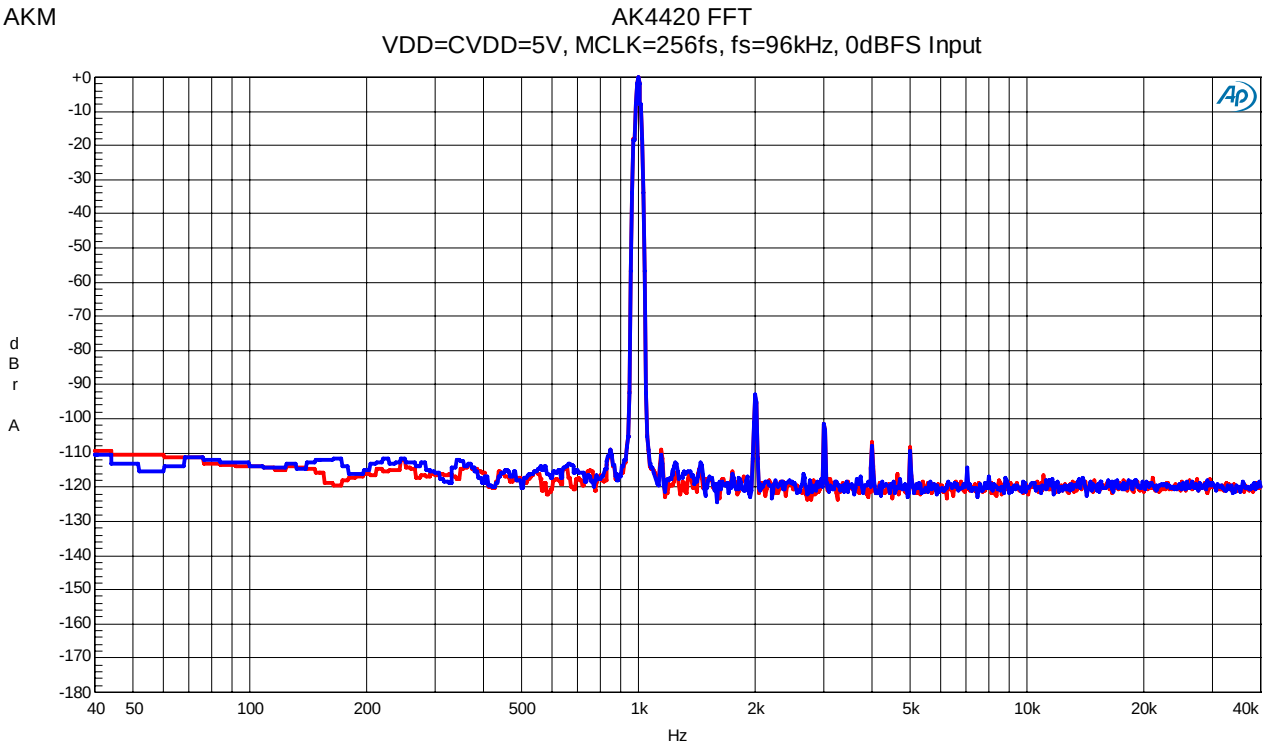


Figure 11. FFT (0dB)

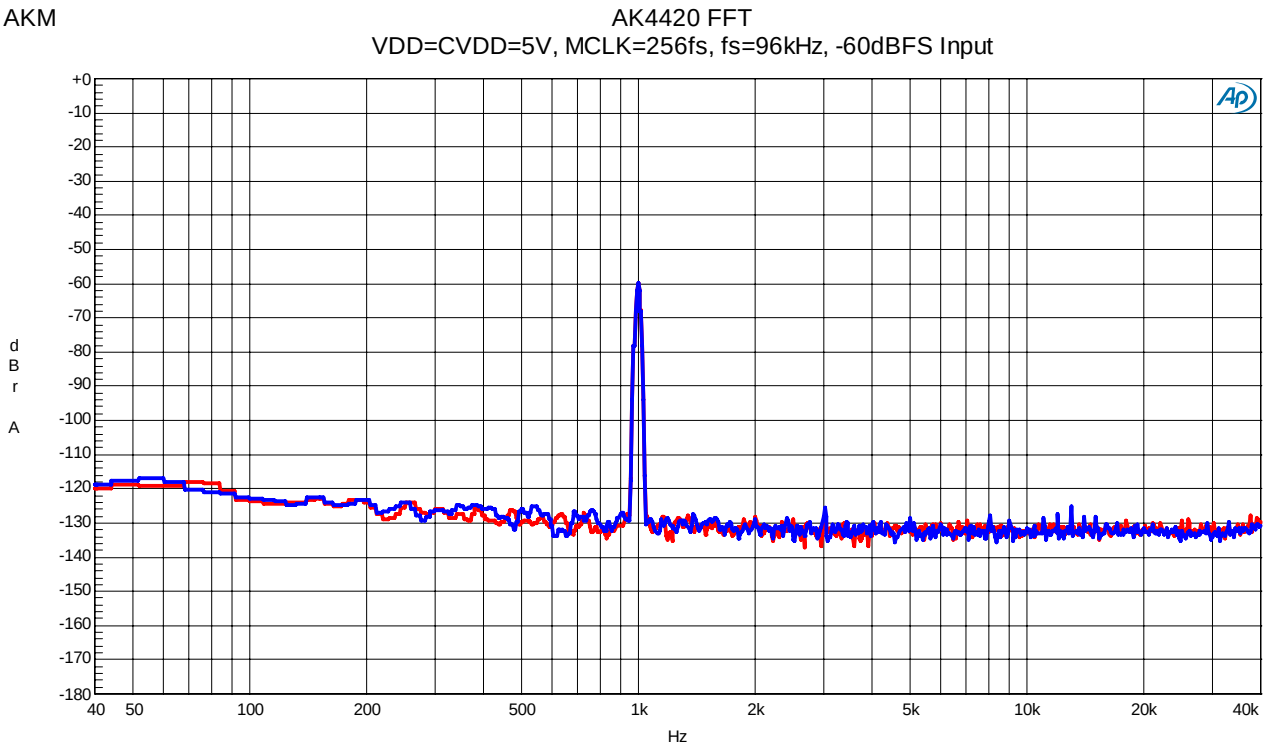


Figure 12. FFT (-60dB)

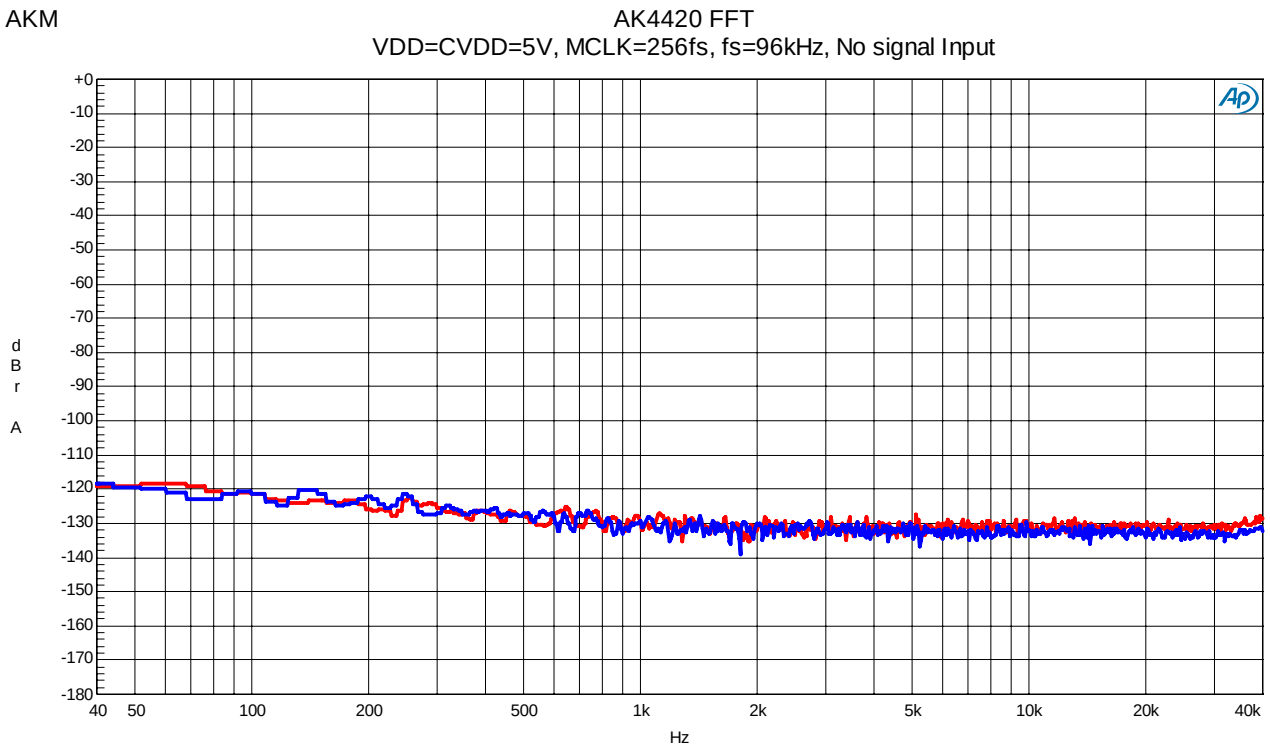


Figure 13. FFT (No Signal)

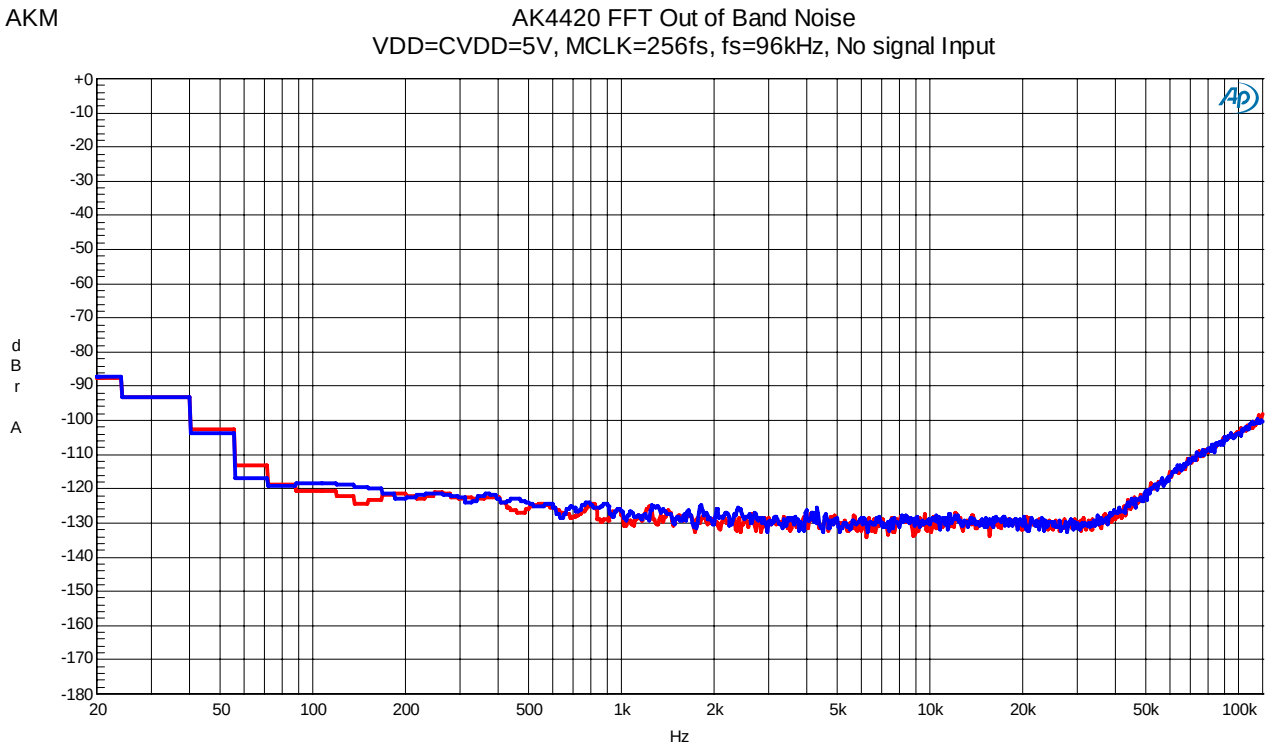


Figure 14. FFT (Out of Band Noise)

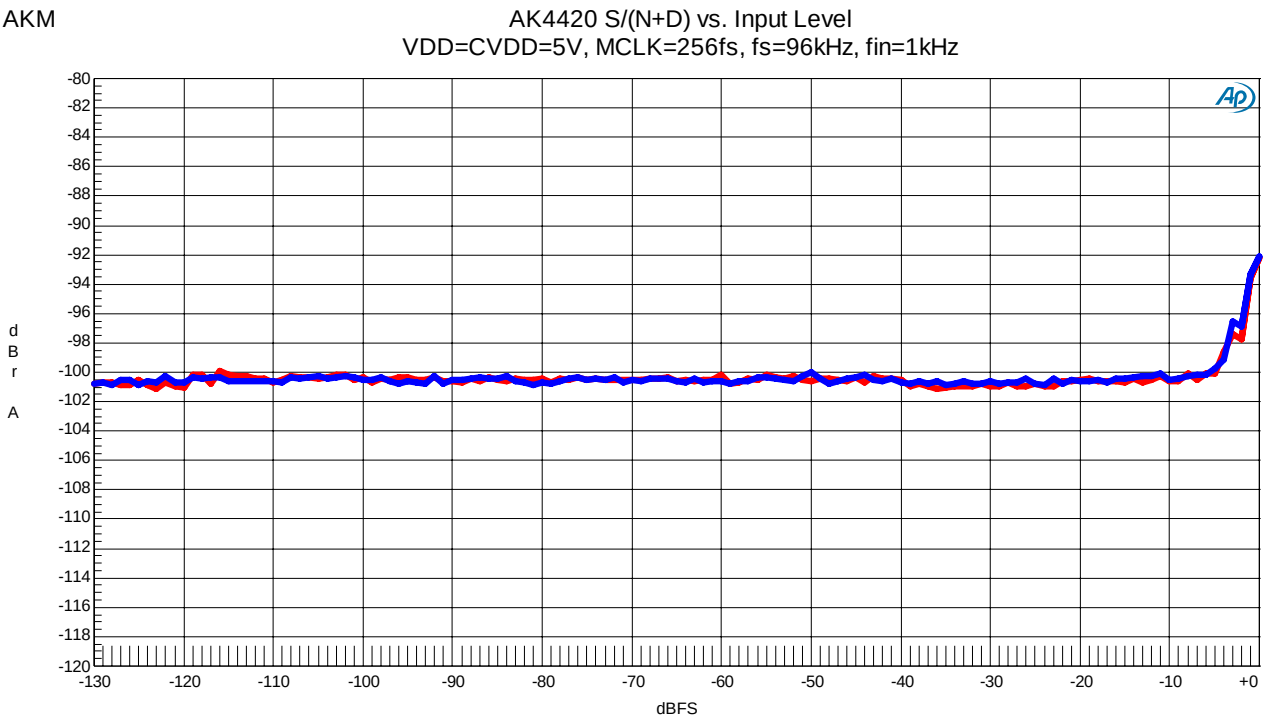


Figure 15. S/(N+D) vs. Input Level

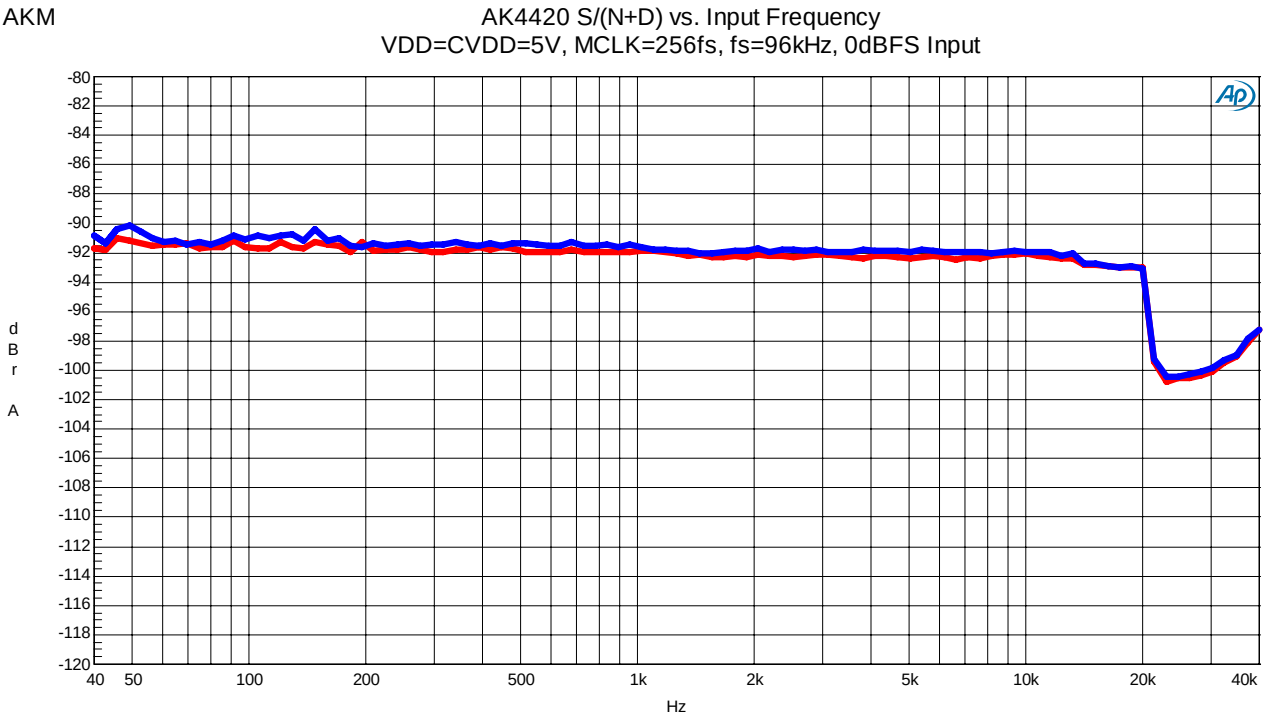


Figure 16. S/(N+D) vs. Input Frequency

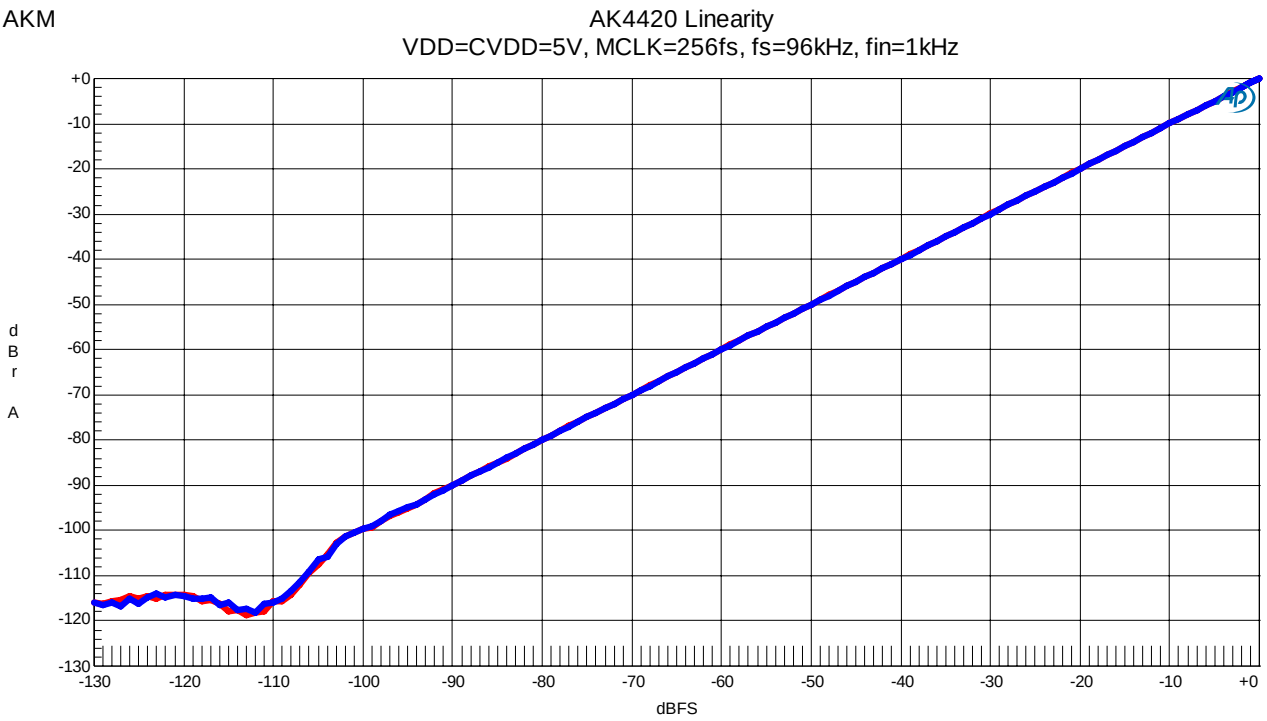


Figure 17. Linearity

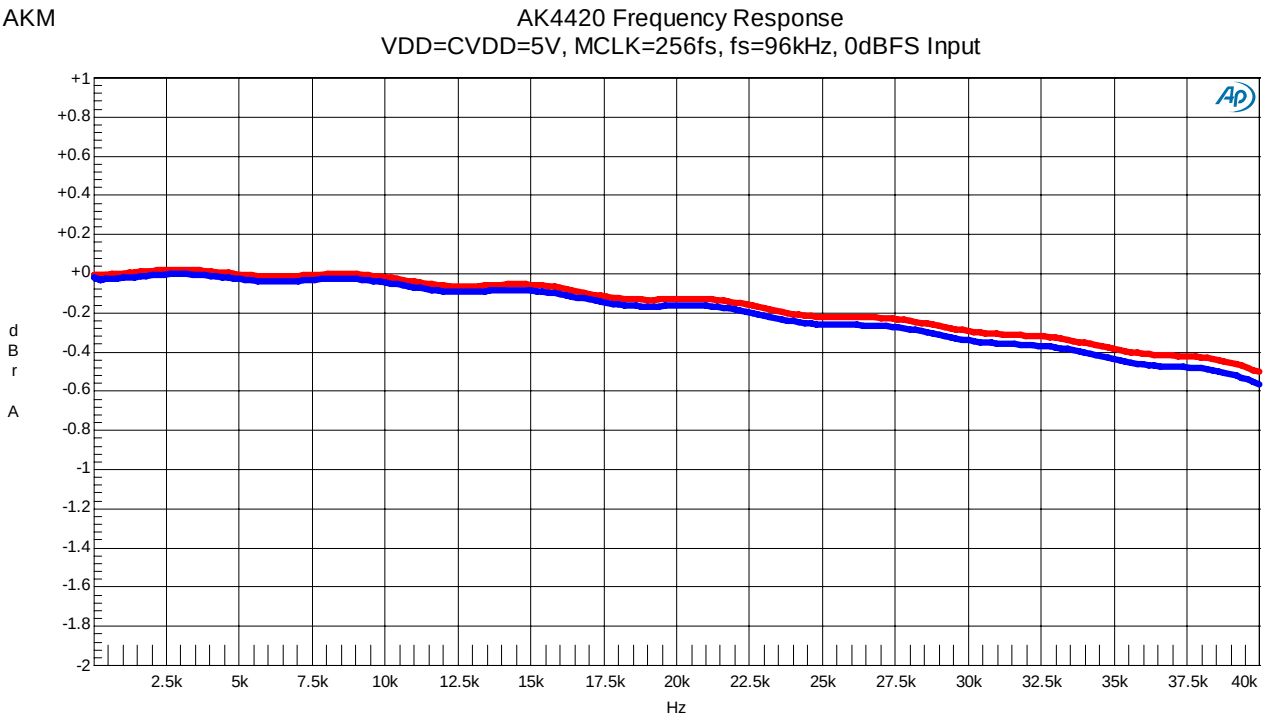


Figure 18. Frequency Response

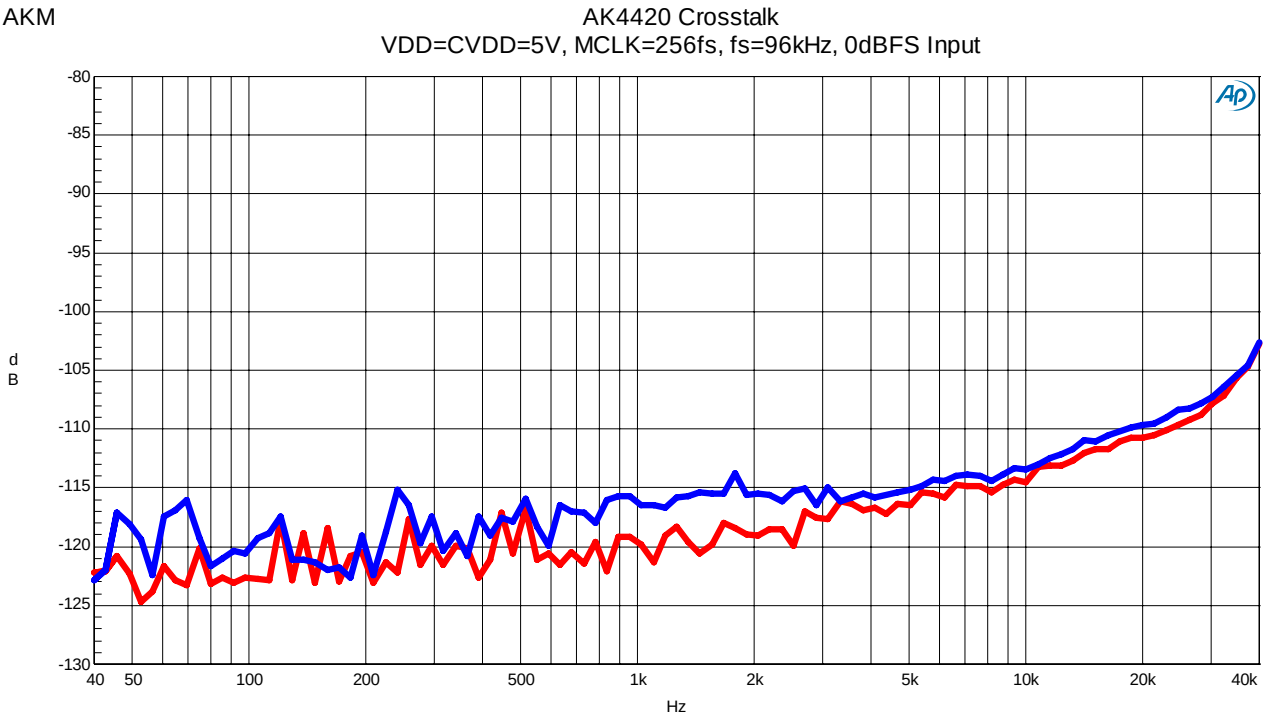


Figure 19. Crosstalk

(fs=192kHz)

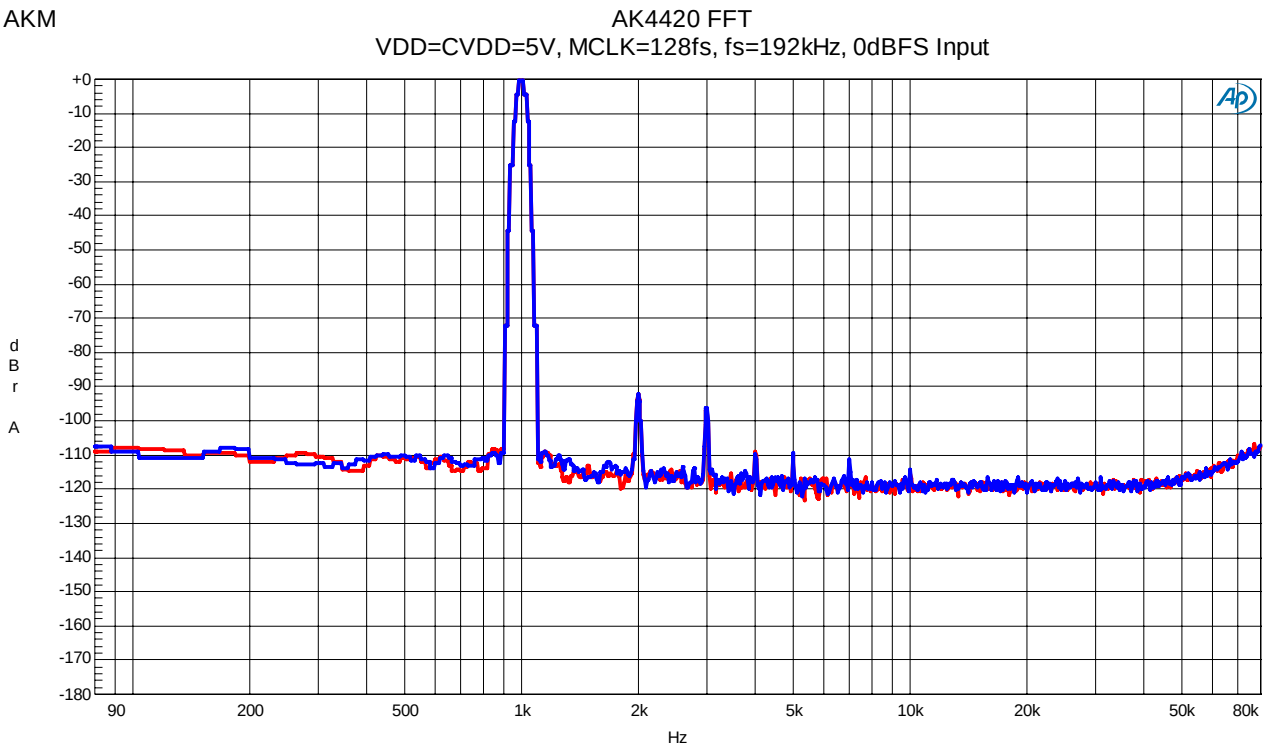


Figure 20. FFT (0dB)

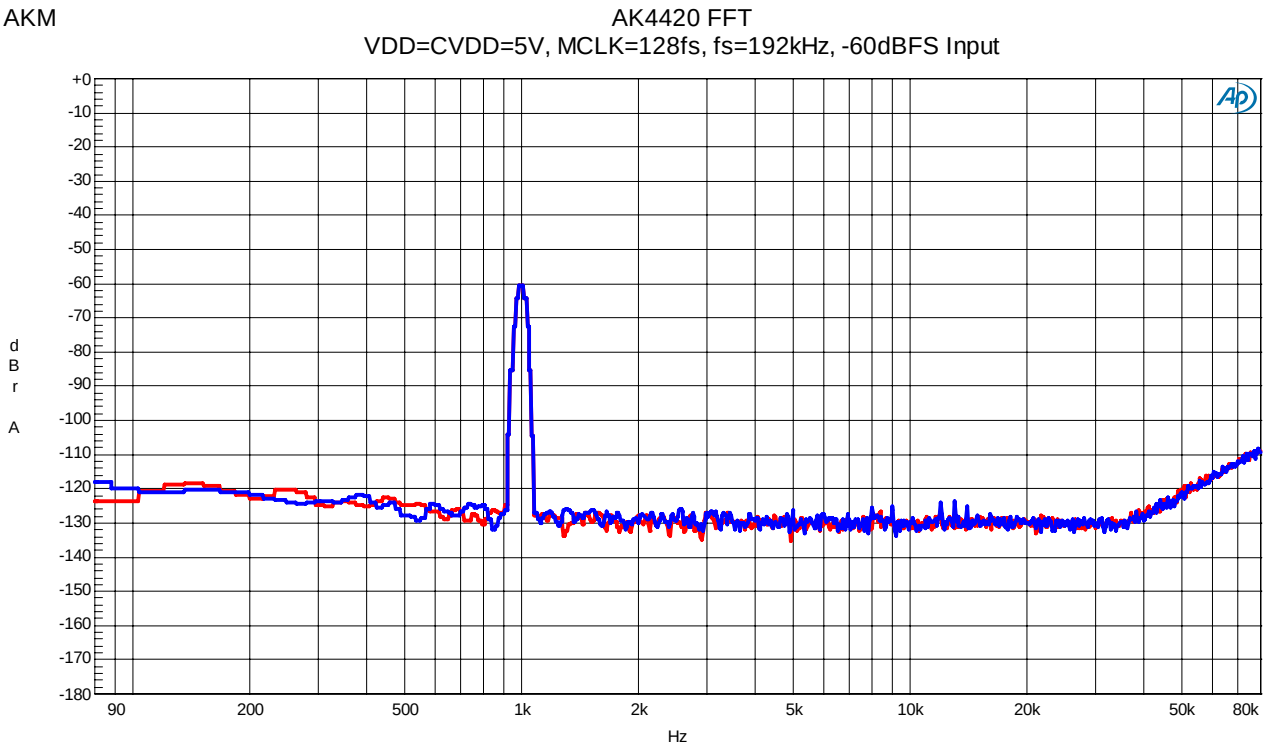


Figure 21. FFT (-60dB)

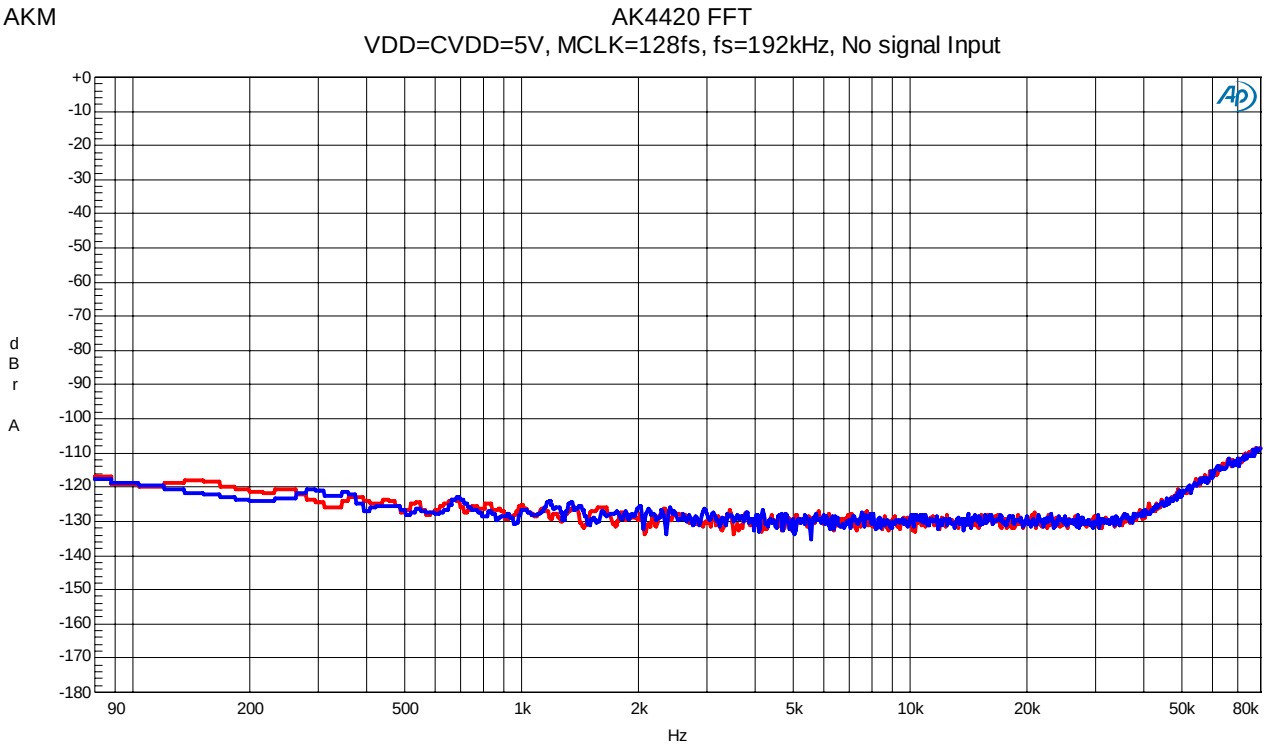


Figure 22. FFT (No Signal)

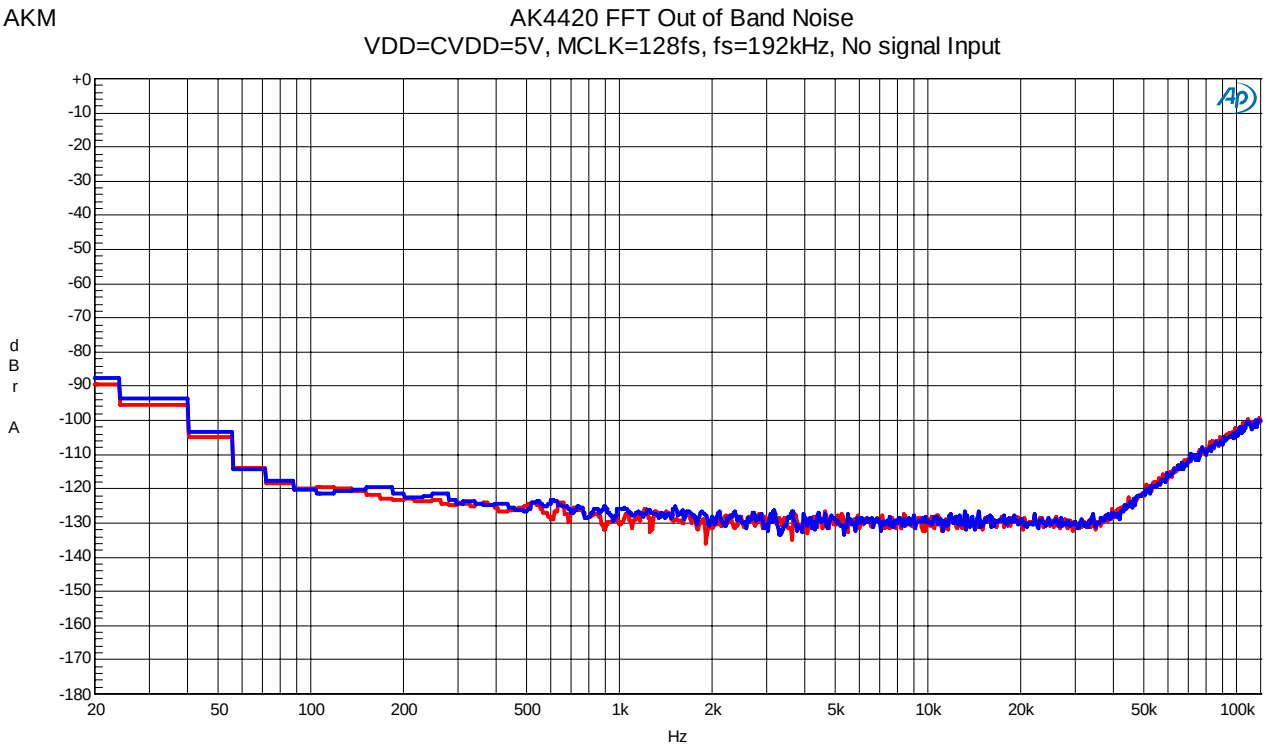


Figure 23. FFT (Out of Band Noise)

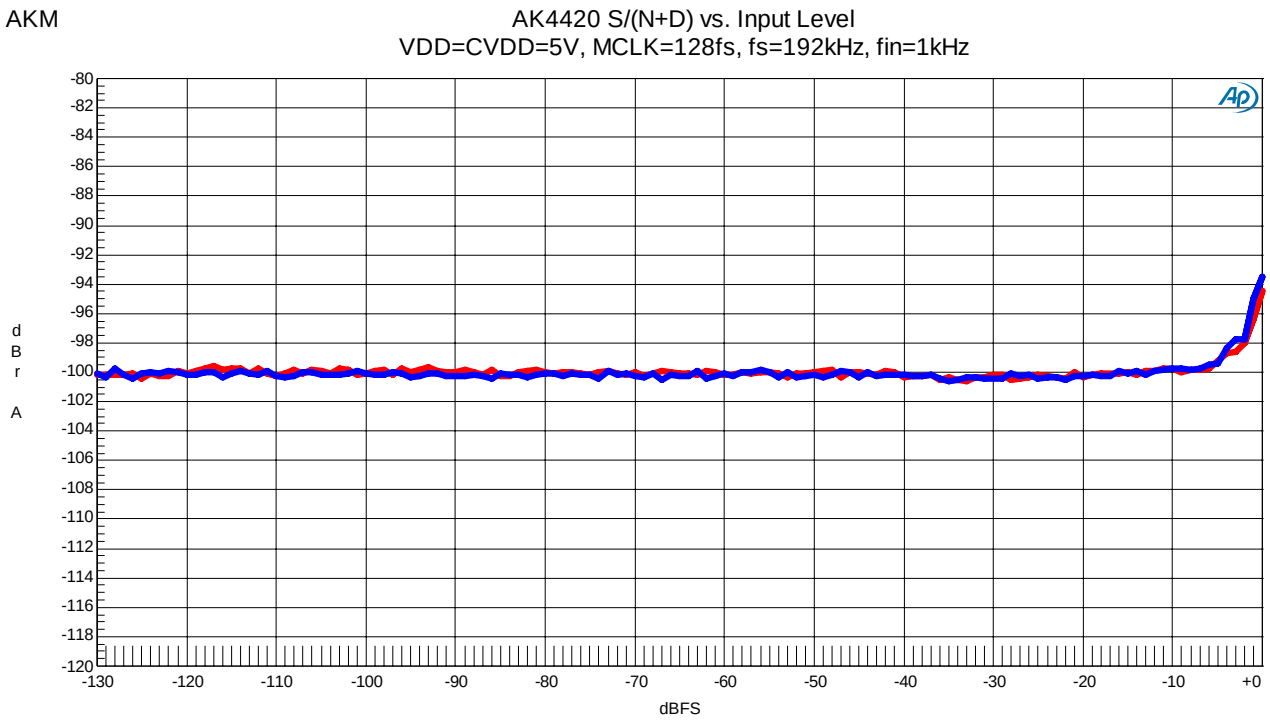


Figure 24. S/(N+D) vs. Input Level

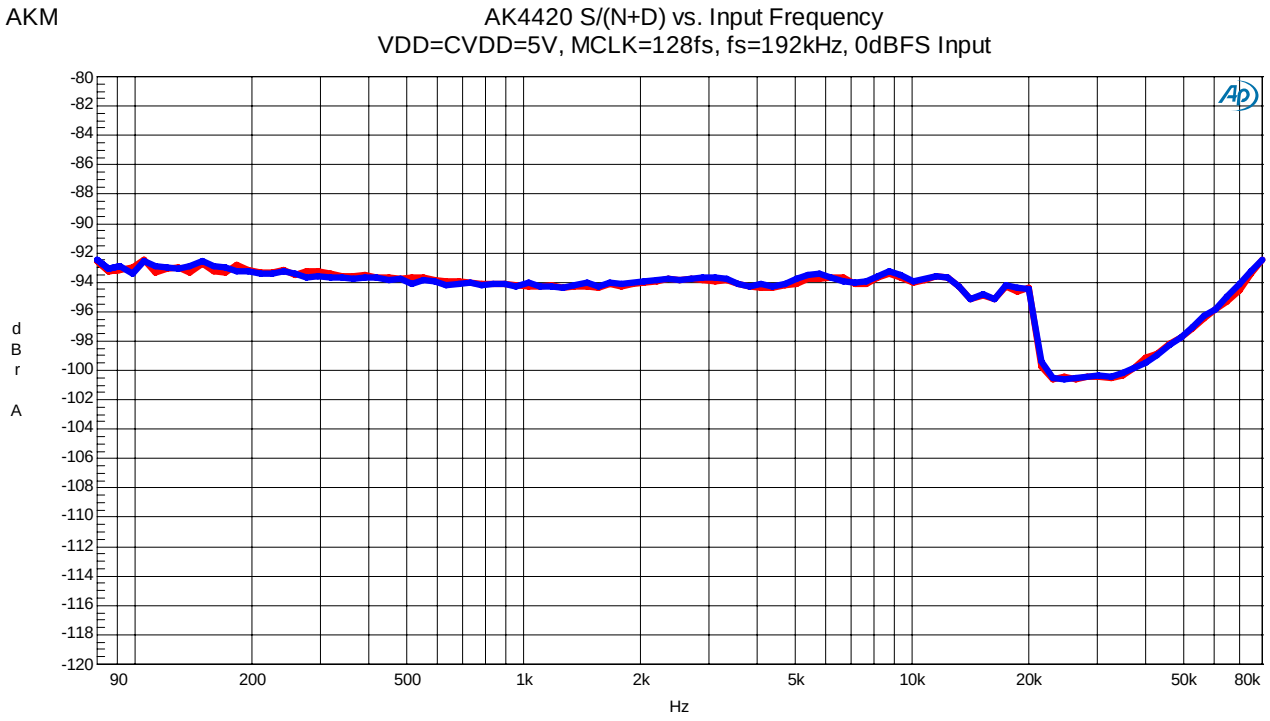


Figure 25. S/(N+D) vs. Input Frequency

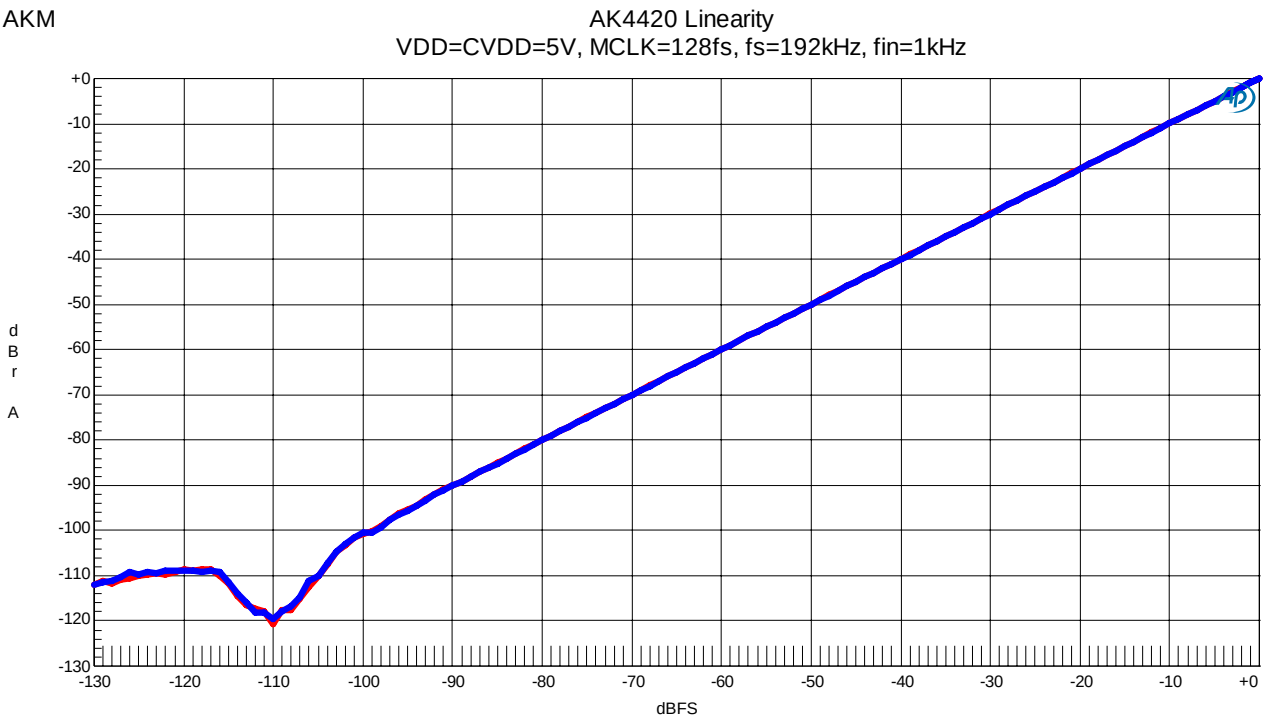


Figure 26. Linearity

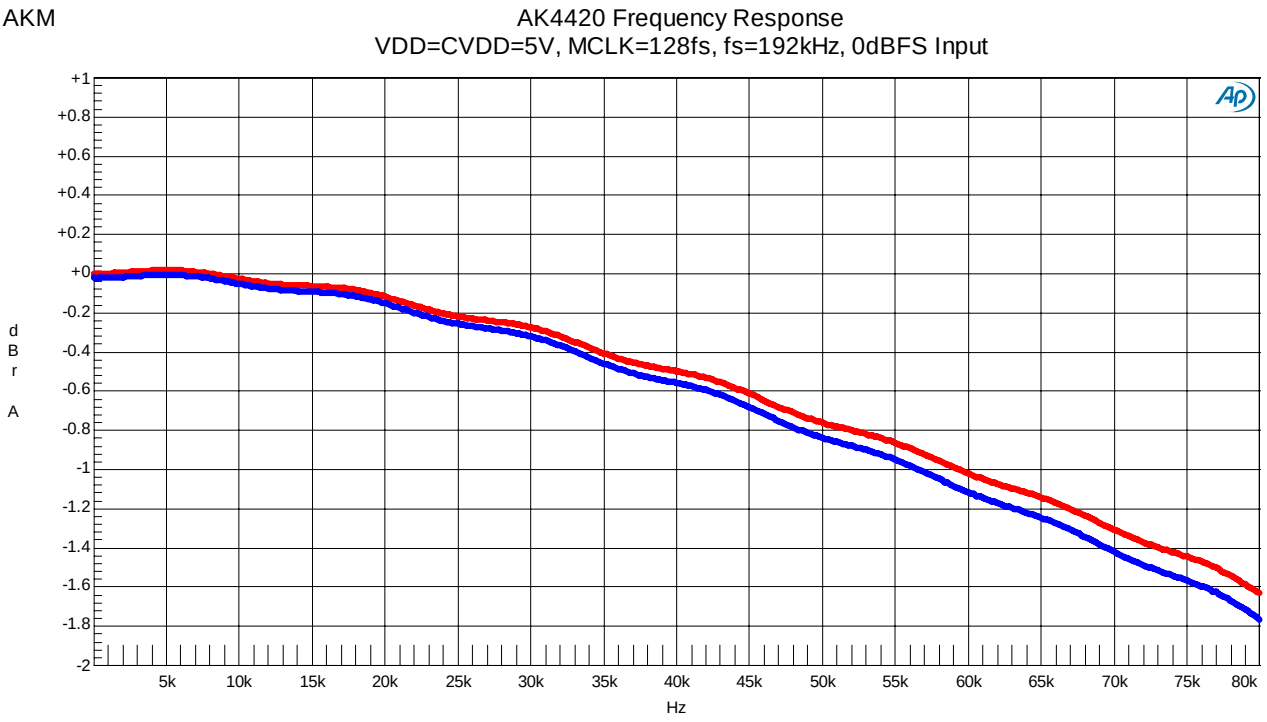


Figure 27. Frequency Response

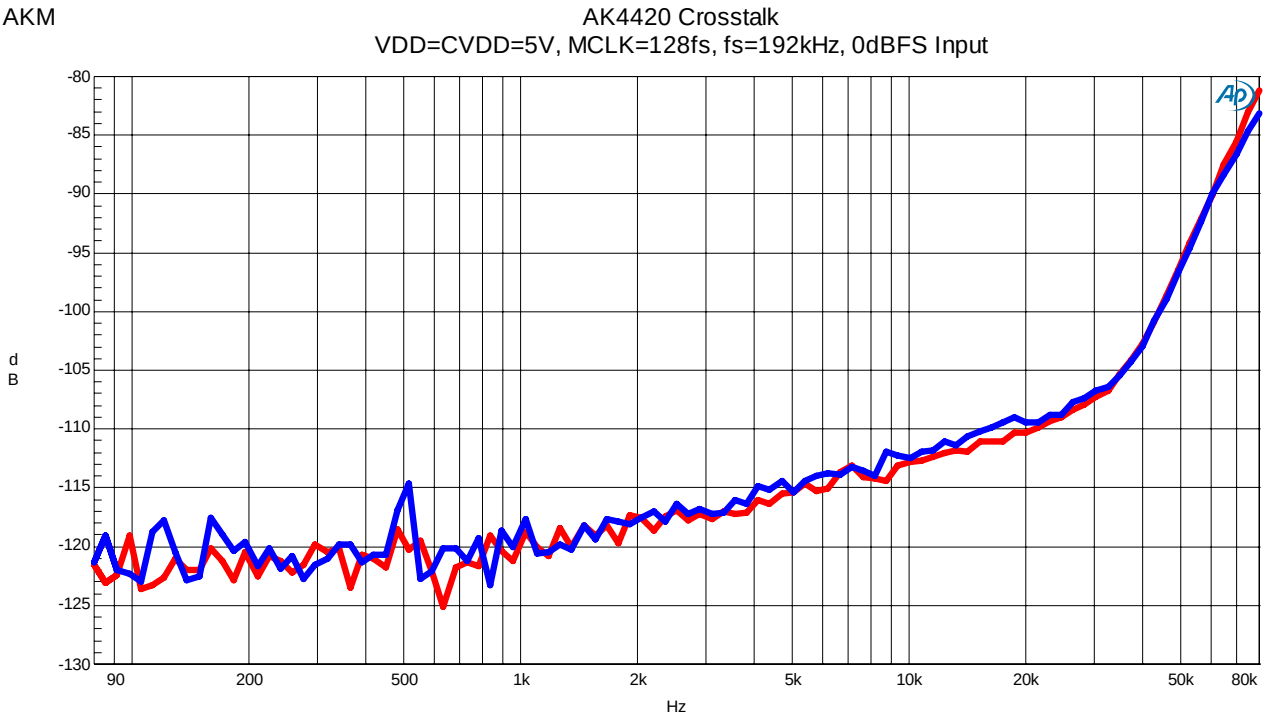
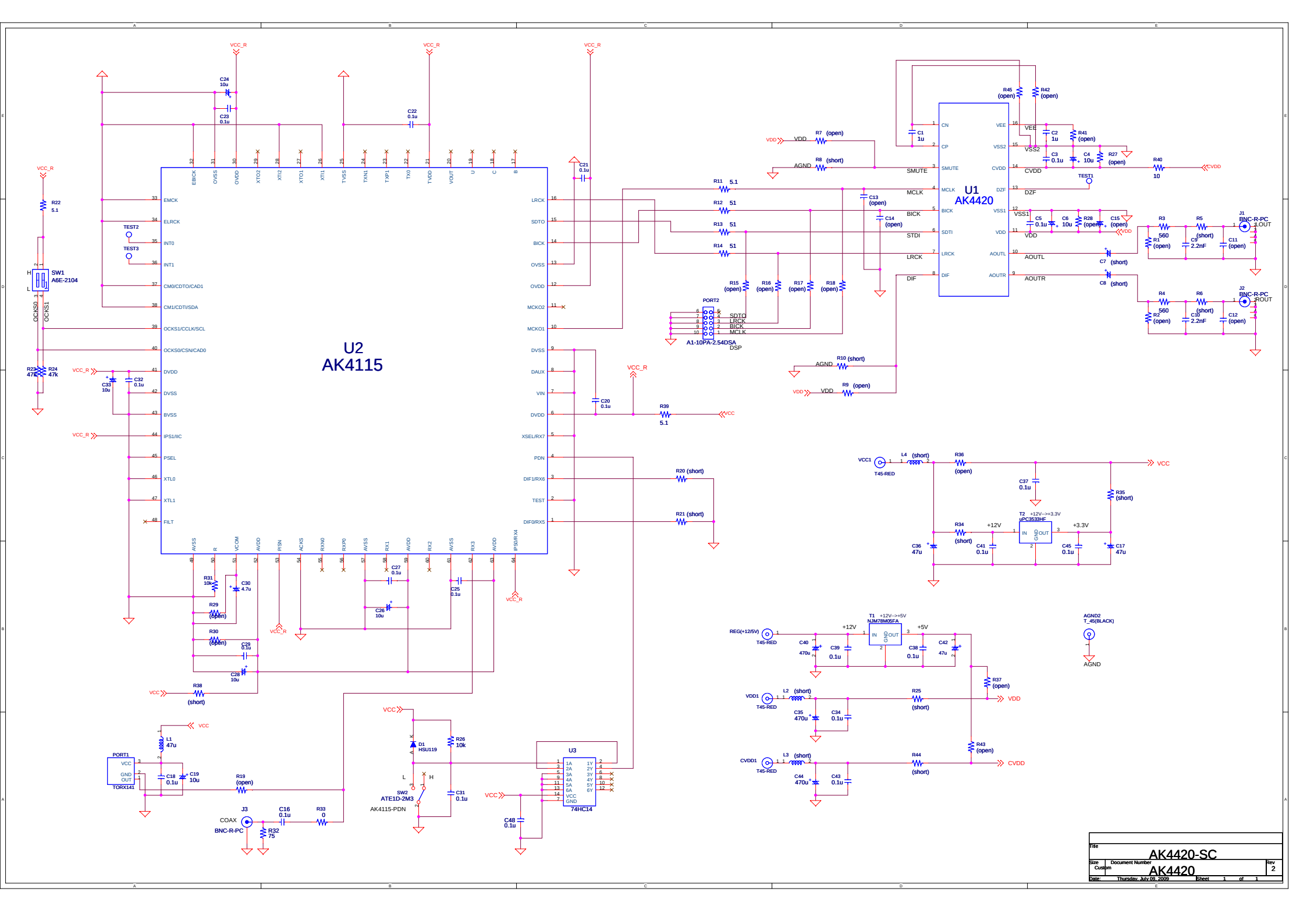


Figure 28. Crosstalk

REVISION HISTORY

Date (yy/mm/dd)	Manual Revision	Board Revision	Reason	Page	Contents
08/01/15	KM091900	0	First Edition		
08/02/25	KM091901	1	Change	12	Circuit diagram was changed. : Regulator: T2: TA48033F→uPC3533HF
				1	Figure 1. Block diagram was replaced.
				3	Table 1. Set up of power supply lines was replaced.
			Correction		Set up of power supply lines and setting of evaluation mode: error correction
08/08/22	KM091902	2	Change	3	Table 1. Set up of power supply lines:Explanation changed.
					Note 1, Note 2: Explanation changed.
				12	Circuit diagram was changed. : R34,R35: open → short R36: short → open
09/04/17	KM091903	2	Change	12	Circuit diagram was changed. : SW1: DSS102 → A6E-2104
09/07/09	KM091904	2	Modification	5-20	Update of measurement results and Plots.


U2
AK4115
U1
AK4420
U3
74HC14
SW1
A6E-2104
SW2
ATE1D-2M3
AK4115-PDN
PORT1
TORX141
PORT2
A1-10PA-2.54DSA
DSP
J1
BNC-R-PC
LOUT
J2
BNC-R-PC
ROUT
J3
COAX
BNC-R-PC
T1
NJM78M05FA
T2
uPC3533HF
D1
HSU119
REG(+12/5V)
T45-RED
AGND2
T_45(BLACK)
VCC_R
VCC
VDD
CVDD
AOUTL
AOUTR
SDTO
LRCK
BICK
MCLK
OCKS0
OCKS1
AK4420-SC
AK4420
Thursday, July 02, 2009