# 74HC373

Octal Transparent D-type Latches W ith 3-State Outputs

## GENERAL DESCRIPTION

74HC373 is fabricated with high-speed silicon gate CMOS technology. It has the high noise immunity and low power consumption of standard CMOS integrated circuits.

The eight latches in 74HC373 devices are transparent D-type latches. While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is low, the Q outputs are latched at the levels that were set up at the D inputs.

An output-enable input ($\overline{OE}$) makes the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pull-up components.

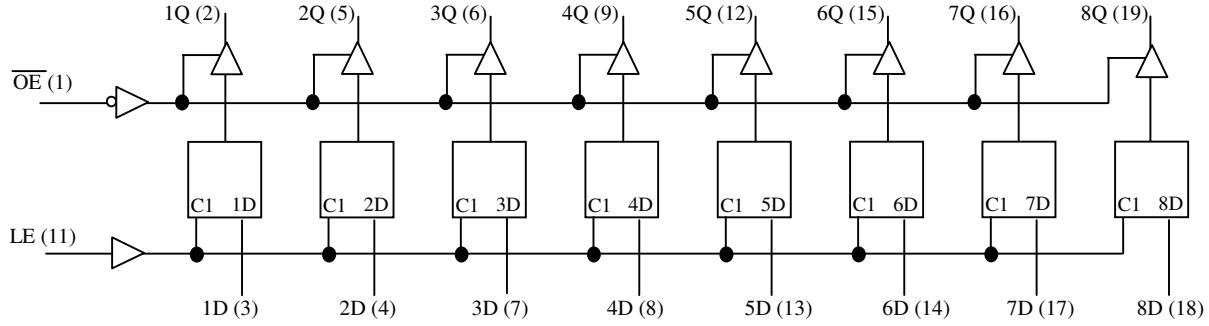
$\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off.

These 8-bit latches with 3-state outputs are designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bi-directional bus drivers, and working registers.

## FEATURES

- Wide operating supply voltage range: 2-6V
- 8 high-current latches with 3-state outputs in a single package
- Full parallel access for loading
- Low input current: 1μA (Max.)
- Low power consumption: 80μA (Max.)

## LOGIC DIAGRAM




## FUNCTIONAL DESCRIPTION

### Truth Table

| Inputs | | | Outputs |
|---|---|---|---|
| $\overline{OE}$ | LE | D | Q |
| L | H | H | H |
| L | H | L | L |
| L | L | X | $Q_0$ |
| H | X | X | Z |

H = High Level (steady state). L= Low Level (steady state)
X = Irrelevant (any input, including transitions)

## ABSOLUTE MAXIMUM RATINGS

| Parameter | Value | Unit |
|---|---|---|
| DC supply voltage (Vcc) | - 0.5 ~ + 7.0 | V |
| DC input or output Voltage ($V_{IN}$, $V_{OUT}$) | -0.5 to Vcc +0.5 | V |
| DC Current Drain per pin, any output ($I_{out}$) | ±35 | mA |
| DC Current per pin, Vcc or GND (Icc) | ±70 | mA |
| Storage Temperature( $T_{STG}$) | -65 ~ +150 | ℃ |

**Note:** 1. Absolute maximum ratings are those values beyond which the safety of the device cannot be guaranteed.

## RECOMMENDED OPERATING CONDITONS

| Parameter | | Min. | Normal | Max. | Unit |
|---|---|---|---|---|---|
| Vcc Supply Voltage | | 2.0 | 5.0 | 6.0 | V |
| $V_{IH}$ High-level Input Voltage | $V_{CC}$ = 2.0V<br>$V_{CC}$ = 4.5V<br>$V_{CC}$ = 6.0V | 1.5<br>3.15<br>4.2 | | | V |
| $V_{IL}$ Low-level Input Voltage | $V_{CC}$= 2.0V<br>$V_{CC}$ = 4.5V<br>$V_{CC}$ = 6.0V | | | 0.5<br>1.35<br>1.8 | V |
| $V_I$ Input Voltage | | 0 | | Vcc | V |
| $V_O$ Output Voltage | | 0 | | Vcc | V |
| Operating Temperature (TA) | 74HC373 | -40 | | +85 | ℃ |
| Input Rise/Fall Times (tr, tf) | $V_{CC}$ = 2.0V<br>$V_{CC}$ = 4.5V<br>$V_{CC}$ = 6.0V | | | 1000<br>500<br>400 | ns |

**Note**: 2. All unused inputs of the device must be held at Vcc or GND to ensure proper device operation.

## DC ELECTRICAL CHARACTERISTICS

( apply across temperature range unless otherwise specified)

| Parameter | Test Conditions | | Vcc | $T_A$=25°C Min. | Typ. | Max. | -40 ~ +85 Min. | Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | $V_I$ =$V_{IH}$ or $V_{IL}$ | $I_{OH}$ = -20uA | 2V | 1.9 | 1.998 | | 1.9 | | V |
| | | | 4.5V | 4.4 | 4.499 | | 4.4 | | |
| | | | 6V | 5.9 | 5.999 | | 5.9 | | |
| | | $I_{OH}$ = -6mA | 4.5V | 3.98 | 4.3 | | 3.84 | | |
| | | $I_{OH}$=-7.8mA | 6V | 5.48 | 5.8 | | 5.34 | | |
| $V_{OL}$ | $V_I$ =$V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 20uA | 2V | | 0.002 | 0.1 | | 0.1 | V |
| | | | 4.5V | | 0.001 | 0.1 | | 0.1 | |
| | | | 6V | | 0.001 | 0.1 | | 0.1 | |
| | | $I_{OL}$ = 6mA | 4.5V | | 0.17 | 0.26 | | 0.33 | |
| | | $I_{OL}$ = 7.8mA | 6V | | 0.15 | 0.26 | | 0.33 | |
| $I_I$ | $V_I$ = $V_{CC}$ or 0 | | 6V | | ±0.1 | ±100 | | ±1000 | nA |
| $I_{OZ}$ | $V_O$ = $V_{CC}$ or 0 | | 6V | | ±0.01 | ±0.5 | | ±5 | μA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or 0, $I_O$ = 0 | | 6V | | | 8 | | 80 | μA |
| $C_i$ | | | 2V～6V | | 3 | 10 | | 10 | pF |

**TIMING REQUIREMENTS OVER RECOMMENDED OPERATING TEMPERATURE**

(unless otherwise specified)

| Parameter | | $V_{DD}$ | $T_A$ = 25℃ | | -40 ~ +85 | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| tw | Pulse duration, LE high | 2.0 V | 80 | | 100 | | ns |
| | | 4.5V | 16 | | 20 | | |
| | | 6.0 V | 14 | | 17 | | |
| tsu | Setup time, data before LE ↓ | 2.0 V | 50 | | 63 | | ns |
| | | 4.5V | 10 | | 13 | | |
| | | 6.0 V | 9 | | 11 | | |
| th | Hold time, data after LE ↓ | 2.0 V | 20 | | 24 | | ns |
| | | 4.5V | 10 | | 12 | | |
| | | 6.0 V | 10 | | 12 | | |

**AC ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING TEMPERATURE, CL = 50 pF**

(unless otherwise specified)

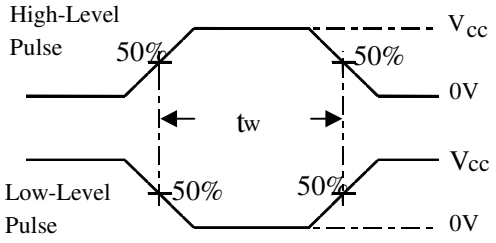
| Parameter | From (Input) | To (Output) | $V_{DD}$ | $T_A$ = 25℃ | | | -40 ~ +85 | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Max | |
| tpd | D | Q | 2.0 V | | 58 | 150 | | 190 | ns |
| | | | 4.5V | | 15 | 30 | | 38 | |
| | | | 6.0 V | | 13 | 26 | | 32 | |
| | LE | Any Q | 2.0 V | | 73 | 175 | | 220 | |
| | | | 4.5V | | 18 | 35 | | 44 | |
| | | | 6.0 V | | 15 | 30 | | 38 | |
| ten | $\overline{OE}$ | Any Q | 2.0 V | | 65 | 150 | | 190 | ns |
| | | | 4.5V | | 17 | 30 | | 38 | |
| | | | 6.0 V | | 14 | 26 | | 32 | |
| tdis | $\overline{OE}$ | Any Q | 2.0 V | | 50 | 150 | | 190 | ns |
| | | | 4.5V | | 15 | 30 | | 38 | |
| | | | 6.0 V | | 13 | 26 | | 32 | |
| $t_t$ | | Any Q | 2.0 V | | 28 | 60 | | 75 | |
| | | | 4.5V | | 8 | 12 | | 15 | |
| | | | 6.0 V | | 6 | 10 | | 13 | |

**AC ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING TEMPERATURE, CL = 150 pF**

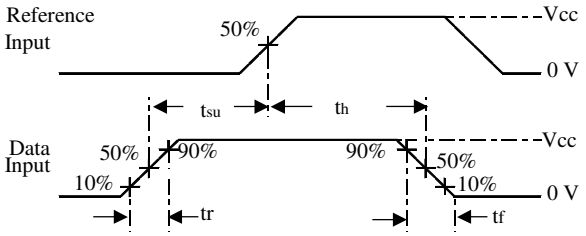
(unless otherwise specified)

| Parameter | From (Input) | To (Output) | $V_{DD}$ | $T_A$ = 25℃ | | | -40 ~ +85 | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Max | |
| tpd | D | Q | 2.0 V | | 82 | 200 | | 250 | ns |
| | | | 4.5V | | 22 | 40 | | 50 | |
| | | | 6.0 V | | 19 | 34 | | 43 | |
| | LE | Any Q | 2.0 V | | 100 | 225 | | 285 | |
| | | | 4.5V | | 24 | 45 | | 57 | |
| | | | 6.0 V | | 20 | 38 | | 48 | |
| ten | $\overline{OE}$ | Any Q | 2.0 V | | 90 | 200 | | 250 | ns |
| | | | 4.5V | | 23 | 40 | | 50 | |
| | | | 6.0 V | | 19 | 34 | | 43 | |
| $t_t$ | | Any Q | 2.0 V | | 45 | 210 | | 265 | ns |
| | | | 4.5V | | 17 | 42 | | 53 | |
| | | | 6.0 V | | 13 | 36 | | 45 | |

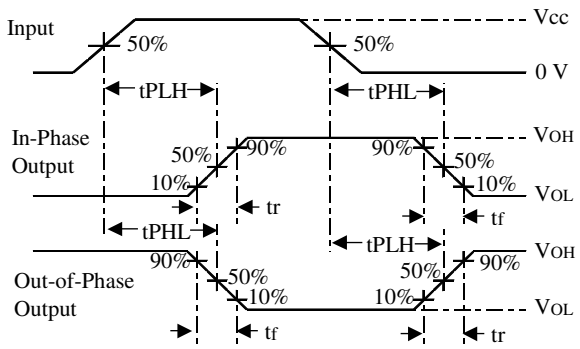
**AC SWITCHING WAVEFORM AND AC TEST CIRCUIT**



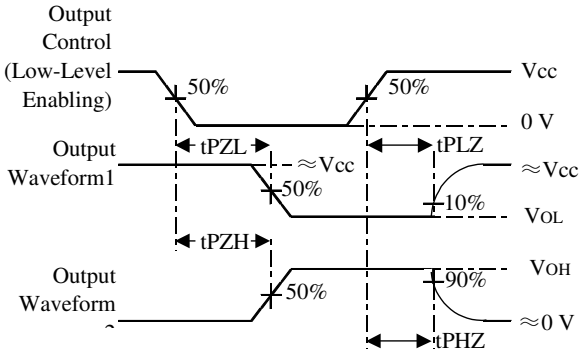

Voltage Waveforms
Pulse Durations



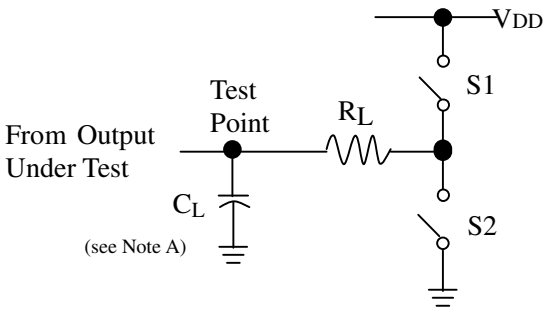

Voltage Waveforms
Setup & Hold and Input Rise & Fall Times




Voltage Waveforms
Propagation Delay and Output Transition Times




Voltage Waveforms
Enable and Disable Times for 3-State Outputs




| Parameter | | $R_L$ | $C_L$ | S1 | S2 |
|---|---|---|---|---|---|
| $t_{en}$ | $t_{PZH}$ | 1k Ω | 50 pF or 150 pF | Open | Closed |
| | $t_{PZL}$ | | | Closed | Open |
| $t_{dis}$ | $t_{PHZ}$ | 1k Ω | 50 pF | Open | Closed |
| | $t_{PLZ}$ | | | Closed | Open |
| $t_{pd}$ or $t_t$ | | - | 50 pF or 150 pF | Open | Open |

**Notes:**

A. $C_L$ includes probe and test-fixture capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:
PRR≤ 1 MHz, Zo = 50 Ω , $t_r$=6ns, $t_f$ =6ns.

D. The outputs are measured one at a time with one input transition per measurement.

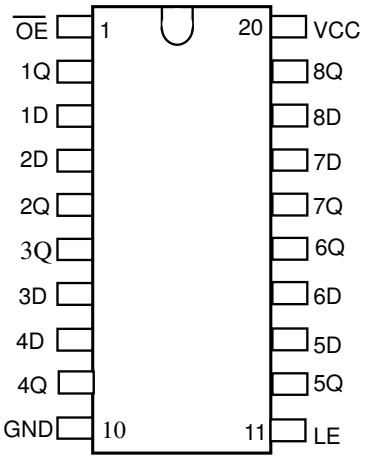
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.

F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.

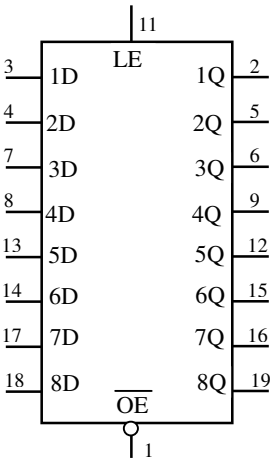
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

## PIN DESCRIPTION

| PIN NO. | SYMBOL | DESCRIPTION |
|---|---|---|
| 3, 4, 7, 8, 13, 14, 17, 18 | 1D - 8D | Data Inputs |
| 2, 5, 6, 9, 12, 15, 16, 19 | 1Q - 8Q | Outputs |
| 10 | GND | Ground (0V) |
| 1 | $\overline{OE}$ | Output-enable |
| 11 | LE | latch-enable |
| 20 | VCC | Positive power supply |

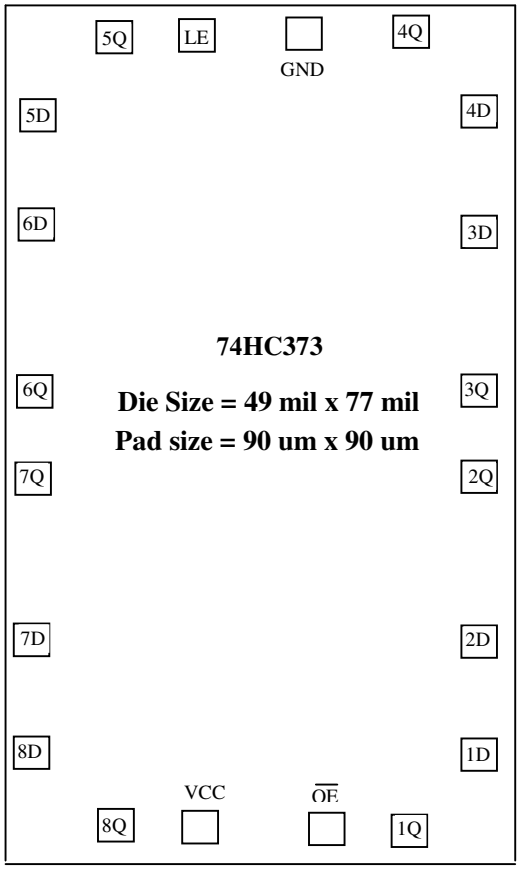



Pin Configuration (DIP-20)




Logic Symbol

**PAD DIAGRAM**




The Coordinate of Each Pad

| | | | |
|---|---|---|---|
| 8Q | (-326.1, -808.7) | 4Q | (237.7, 718.5) |
| $V_{CC}$ | (-151.7, -816.1) | GND | (42.5, 729.9) |
| $\overline{OE}$ | (82.5, -808.7) | LE | (-160.5, 718.6) |
| 1Q | (237.7, -808.7) | 5Q | (-326.1, 718.6) |
| 1D | (388.3, -673.1) | 5D | (-476.5, 568.7) |
| 2D | (388.3, -457.3) | 6D | (-476.5, 352.9) |
| 2Q | (388.0, -132.2) | 6Q | (-476.5, 24.7) |
| 3Q | (388.0, 25.6) | 7Q | (-476.5, -135.0) |
| 3D | (388.1, 351.8) | 7D | (-476.5, -457.2) |
| 4D | (388.1, 567.6) | 8D | (-476.5, -673.0) |

**Note:** Substrate should be connected to Vcc or left it open.