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REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device types 04 through 06. Update boilerplate. Editorial corrections throughout.	96-12-30	Ray Monnin

REV																				
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SHEET																				

REV STATUS OF SHEETS															
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
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DRAWING APPROVAL DATE
23 August 1988

REVISION LEVEL
A

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216

MICROCIRCUIT, DIGITAL, 1024K X 4 CMOS STATIC RAM WITH RESET, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-88588

SHEET 1 OF 14

DESC FORM 193
JUL 94

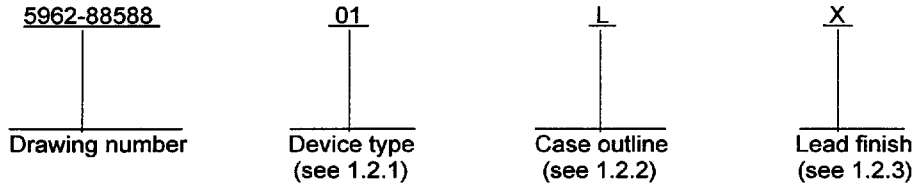
5962-E058-97

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	See 6.6	1024 X 4 CMOS static RAM	35 ns
02	See 6.6	1024 X 4 CMOS static RAM	25 ns
03	See 6.6	1024 X 4 CMOS static RAM	15 ns
04	See 6.6	1024 X 4 CMOS static RAM	35 ns
05	See 6.6	1024 X 4 CMOS static RAM	25 ns
06	See 6.6	1024 X 4 CMOS static RAM	15 ns

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
K	GDFP2-F24 or CDFP3-F24	24	Flat pack
L	GDIP3-T24 or CDIP4-T24	24	Dual-in-line
X	CQCC4-N28	28	Rectangular leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage to ground potential ..... -0.5 V dc to +7.0 V dc
DC voltage applied to outputs ..... -0.5 V dc to +7.0 V dc
DC input voltage ..... -3.0 V dc to +7.0 V dc
DC output current ..... 20 mA
Storage temperature range ..... -65°C to +150°C
Maximum power dissipation (P_D) ..... 1.0 W 1/
Lead temperature (soldering, 10 seconds) ..... +300°C
Thermal resistance, junction-to-case (Θ_{JC}):
Cases K, L, and X ..... See MIL-STD-1835
Junction temperature (T_J) ..... +150°C 2/

1.4 Recommended operating conditions.

Supply voltage range (V_{CC}) ..... 4.5 V dc minimum to 5.5 V dc maximum
High level input voltage range (V_{IH}) ..... 2.0 V dc to 6.0 V dc
Low level input voltage range (V_{IL}) ..... -3.0 V dc to +0.8 V dc
Case operating temperature range (T_C) ..... -55°C to +125°C

1/ Must withstand the added P_D due to short circuit test (e.g., I_{OS}).
2/ Maximum junction temperature may be increased to +175°C during burn-in and steady state life.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

MILITARY

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

HANDBOOKS

MILITARY

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 2.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103 (see 6.6 herein). For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required in accordance with MIL-PRF-38535, appendix A.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance.

d. Subgroups 7 and 8 shall include verification of the truth table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 4.5 V to 5.5 V unless otherwise specified	Group A subgroups	Device Type	Limits		Unit
					Min	Max	
Output high voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -4.0 mA, V_{IL} = 0.8 V, V_{IH} = 2.0 V	1, 2, 3	All	2.4		V
Output low voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 12.0 mA, V_{IL} = 0.8 V, V_{IH} = 2.0 V	1, 2, 3	All		0.4	V
Input load current	I_I	0 V $\le V_{IN} \le$ 5.5 V	1, 2, 3	All		±10	µA
Output current, high impedance	I_{OZ}	GND $\le V_{OUT} = V_{CC}$, output disabled	1, 2, 3	All		±50	µA
Output short-circuit output current 1/ 2/	I_{OS}	V_{CC} = 5.5 V, V_{OUT} = 0 V	1, 2, 3	All		-300	mA
Power supply current (dynamic)	I_{CC}	$\overline{WE}$, $\overline{OE}$, $\overline{RS}$ = 2.0 V, $\overline{CS}$ = 0.8 V, f= $1/t_{RC}$ All other inputs cycling between 2.0 V and 0.8 V	1, 2, 3	01-03		100	mA
				04-06		120	
Input capacitance	C_{IN}	V_{CC} = 5.0 V, f = 1.0 Mhz, T_A =+25°C, see 4.3.1c	4	01-03		5.0	pF
				04-06		7.0	
Output capacitance	C_{OUT}		4	01-03		7.0	
				04-06		9.0	
Functional tests		See 4.3.1d	7, 8A, 8B	All			
Read cycle time	t_{RC}	See figures 3 and 4 3/	9, 10, 11	01,04	35		ns
				02,05	25		
				03,06	15		
Address valid to data valid	t_{AA}		9, 10, 11	01,04		35	
				02,05		25	
				03,06		15	
Data hold from address change	t_{OHA}		9, 10, 11	All	2		
Chip select low to data valid	t_{ACS}		9, 10,11	01,04		20	
				02,05		15	
				03,06		12	
Chip select low to low Z	t_{LZCS}	See figures 3 and 4 2/ 4/	9, 10, 11	All	0		
Chip select high to high Z	t_{HZCS}	See figures 3 and 4 2/ 4/ 5/	9, 10, 11	01,04	0	25	ns
				02,05	0	20	
				03,06	0	11	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 4.5 V to 5.5 V unless otherwise specified	Group A subgroups	Device Type	Limits		Unit
					Min	Max	
Output enable low to data valid	t_{DOE}	See figures 3 and 4 2/ 3/	9, 10, 11	01,04		20	ns
				02,05		15	
				03,06		10	
Output enable low to low Z	t_{LZOE}	See figures 3 and 4 2/ 3/ 4/	9, 10, 11	All	0		ns
Output enable high to high Z	t_{HZOE}	See figures 3 and 4 2/ 4/ 5/	9, 10, 11	01,04	0	25	ns
				02,05	0	20	
				03,06	0	9	
Write cycle time	t_{WC}	See figures 3 and 5 3/	9, 10, 11	01,04	35		ns
				02,05	25		
				03,06	15		
Chip select low to write end	t_{SCS}		9, 10, 11	01,04	20		
				02,05	15		
				03,06	11		
Address set-up to write end	t_{AW}		9, 10, 11	01,04	30		
				02,05	20		
				03,06	13		
Address hold from write end	t_{HA}		9, 10, 11	All	5		
Address set-up to write start	t_{SA}		9, 10, 11	All	5		
Write enable pulse width	t_{PWE}		9, 10, 11	01,04	20		
				02,05	15		
				03,06	11		
Data set-up to write end	t_{SD}		9, 10, 11	01,04	20		
				02,05	15		
				03,06	11		
Data hold from write end	t_{HD}		9, 10, 11	All	5		
Write enable high to low Z	t_{LZWE}	See figures 3 and 5 2/ 3/ 4/	9, 10,11	All	0		ns
Write enable low to high Z	t_{HZWE}	See figures 3 and 5 2/ 4/ 5/	9, 10,11	01,04	0	25	ns
				02,05	0	20	
				03,06	0	12	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 4.5 V to 5.5 V unless otherwise specified	Group A subgroups	Device Type	Limits		Unit
					Min	Max	
Reset cycle time	t_{RRC}	See figures 3 and 6 3/	9, 10,11	01,04	70		ns
				02,05	50		
				03,06	30		
Address valid to beginning of reset	t_{SAR}		9, 10,11	All	0		
Write enable high to beginning of reset	t_{SWER}		9, 10,11	All	0		
Chip select low to beginning of reset	t_{SCSR}		9, 10,11	All	0		
Reset pulse width	t_{PRS}		9, 10,11	01,04	30		
				02,05	20		
				03,06	15		
Chip select hold after end of reset	t_{HCSR}		9, 10,11	All	0		
Write enable hold after end of reset	t_{HWER}		9, 10,11	01,04	40		
				02,05	30		
				03,06	15		
Address hold after end of reset	t_{HAR}		9, 10,11	01,04	40		
				02,05	30		
				03,06	15		
Reset high to output in low Z	t_{LZRS}	See figures 3 and 6 2/ 3/ 4/	9, 10,11	All	0		ns
Reset high to output in high Z	t_{HZRS}	See figures 3 and 6 2/ 4/ 5/	9, 10,11	01,04	0	25	ns
				02,05	0	20	
				03,06	0	12	

1/ Not more than one output should be shorted at a time, and duration of short circuit shall not exceed 30 seconds.
2/ Parameter guaranteed, if not tested.
3/ Test conditions assume signal transition times of 5.0 ns or less. Timing is referenced at input and output levels of 1.5 V. Output loading is equivalent to the specified I_{OL}/I_{OH} with a load capacitance of 30 pF.
4/ At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for any given device.
5/ Test conditions assume signal transition times of 5.0 ns or less. Transition is measured at steady state high level of -500 mV or steady state low level of +500 mV on the output and from 1.5 V level on the input with a load capacitance of 5.0 pF.

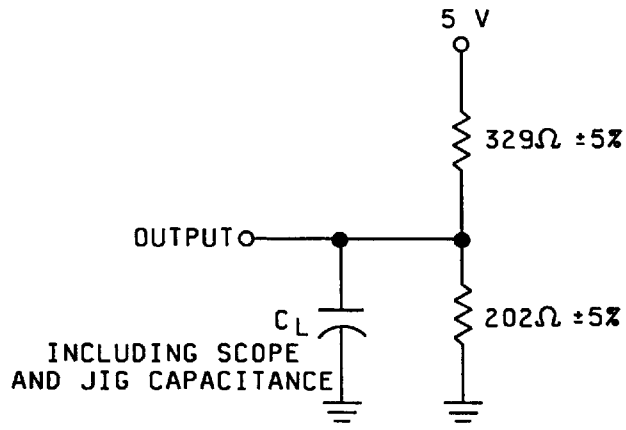
Device types	All	All
Case outlines	L and K	X
Terminal number	Terminal symbol	
1	A_3	NC
2	A_4	A_3
3	A_5	A_4
4	A_6	A_5
5	A_7	A_6
6	A_8	A_7
7	A_9	A_8
8	D_0	NC
9	D_1	A_9
10	O_0	D_0
11	O_1	D_1
12	GND	O_0
13	O_2	O_1
14	O_3	GND
15	D_2	NC
16	D_3	O_2
17	$\overline{OE}$	O_3
18	$\overline{WE}$	D_2
19	$\overline{CS}$	D_3
20	$\overline{RS}$	$\overline{OE}$
21	A_0	$\overline{WE}$
22	A_1	NC
23	A_2	$\overline{CS}$
24	V_{CC}	$\overline{RS}$
25	---	A_0
26	---	A_1
27	---	A_2
28	---	V_{CC}

FIGURE 1. Terminal connections.

Inputs				Output	Mode
$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	$\overline{RS}$	O_n	
H	X	X	X	High Z	Not selected
L	H	X	L	High Z	Reset
L	L	X	H	High Z	Write
L	H	L	H	O_0 - O_3	Read
L	X	H	H	High Z	Output disable

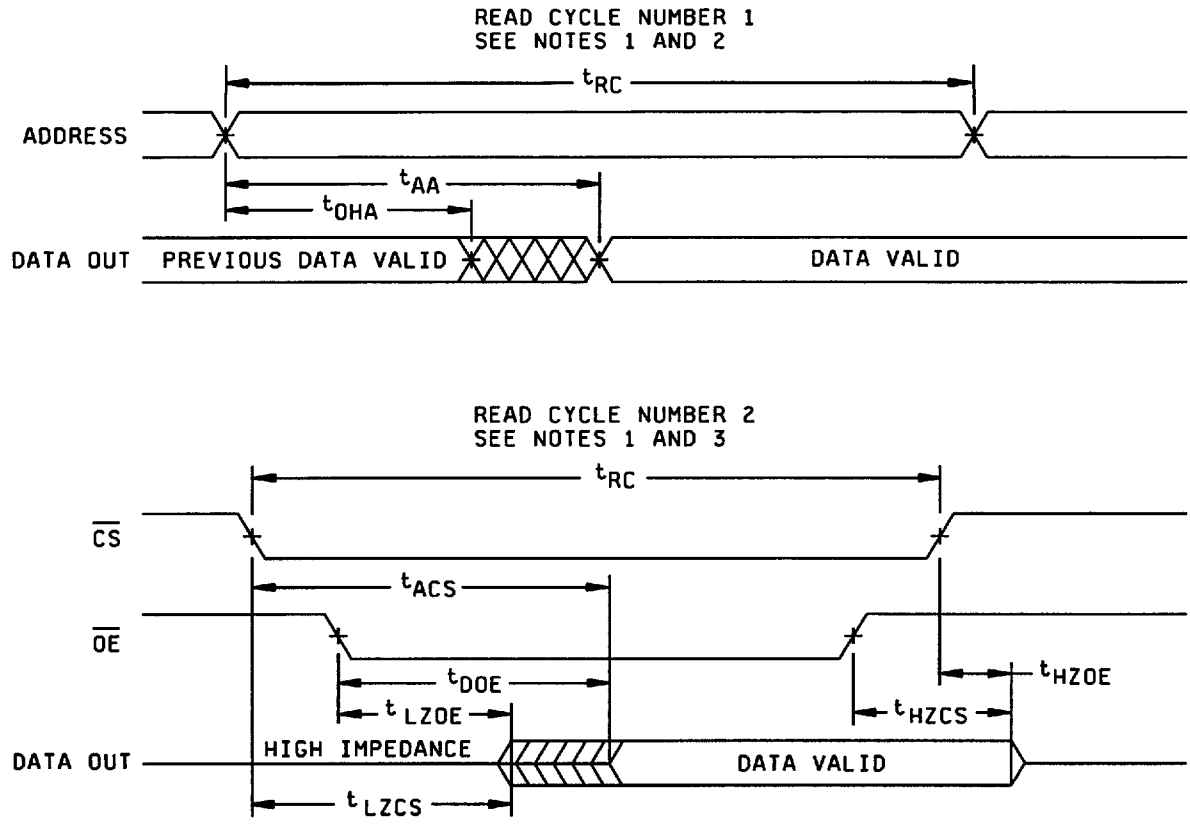
H = Logic 1 state
L = Logic 0 state
X = Don't care
High Z = High impedance state

FIGURE 2. Truth table.



Measurement	C_L including scope and jig capacitance (minimum)
t_{HZCS}, t_{HZOE}, t_{HZRS}, and t_{HZWE}	C_L = 5.0 pF
All others	C_L = 30 pF

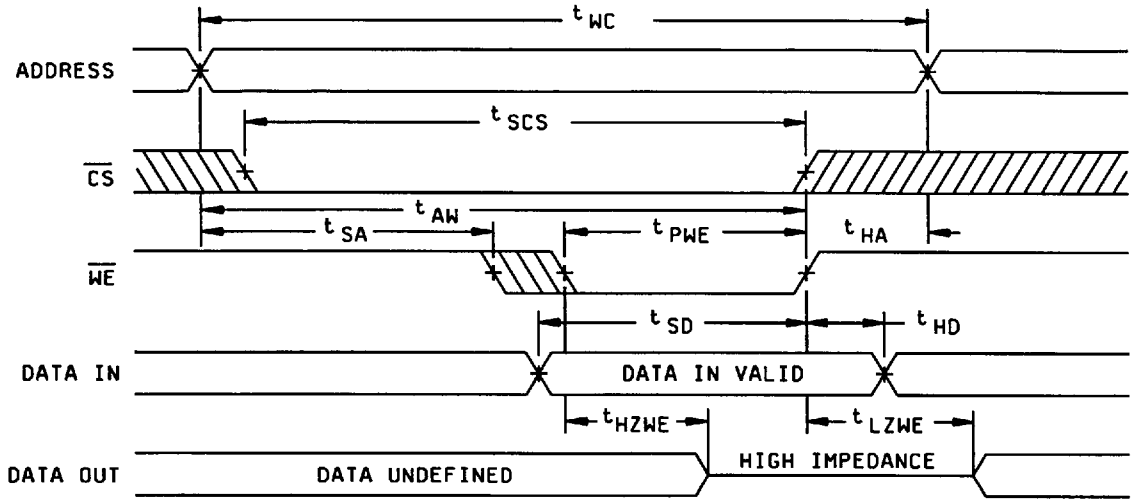
FIGURE 3. Output load circuit.



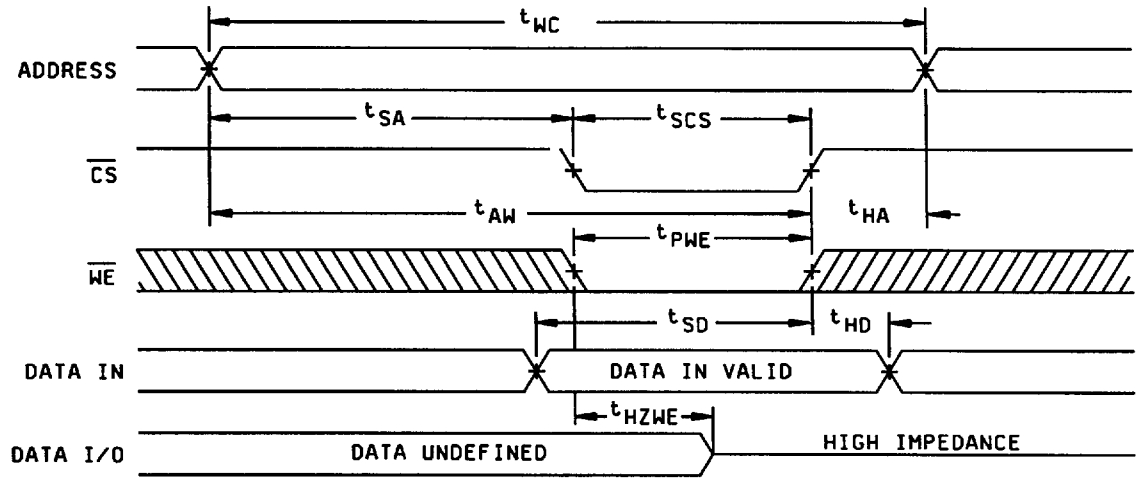
NOTES:
1. $\overline{WE}$ is HIGH for read cycle.
2. Device is continuously selected, $\overline{CS}$ and $\overline{OE}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition LOW.

FIGURE 4. Read cycle timing diagram.

WRITE CYCLE NUMBER 1 - $\overline{WE}$ CONTROLLED
SEE NOTE 1

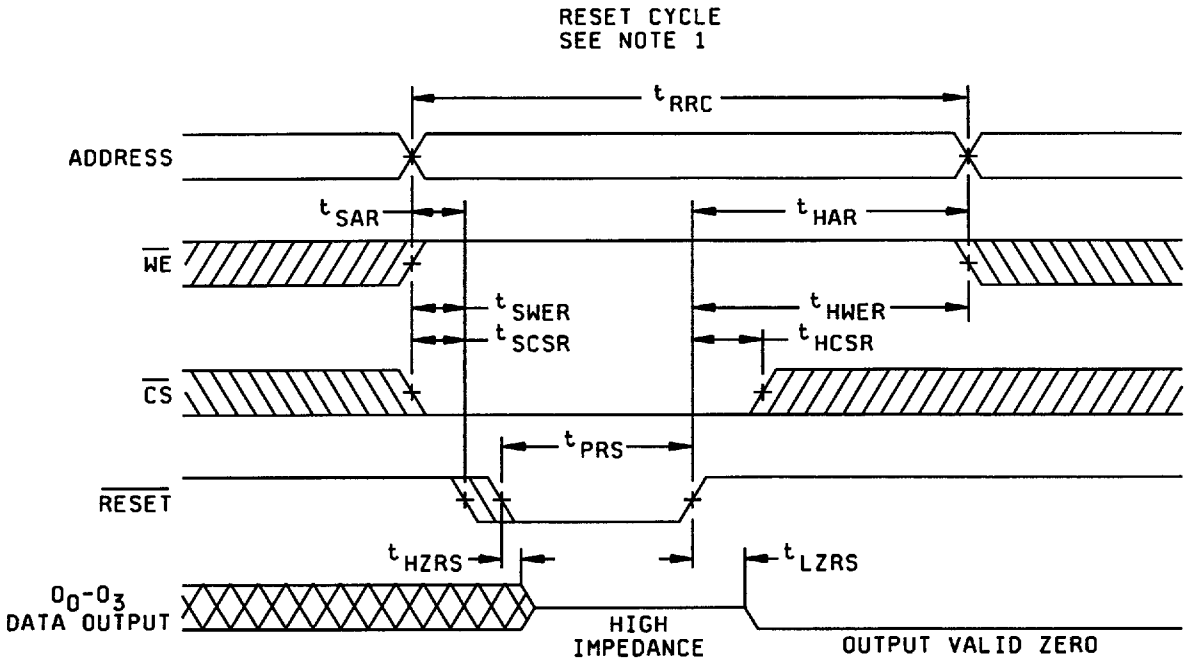


WRITE CYCLE NUMBER 2 - $\overline{CS}$ CONTROLLED
SEE NOTES 1 AND 2



NOTES:
1. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
2. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high impedence state.

FIGURE 5. Write cycle timing diagram.



NOTE: Reset cycle is defined by the overlap of $\overline{RS}$ and $\overline{CS}$ for the minimum reset pulse width.

FIGURE 6. Reset cycle timing diagram.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	
Final electrical test parameters (method 5004)	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 3, 7, 8A, 8B

* PDA applies to subgroup 1.
** See 4.3.1c.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 96-12-30

Approved sources of supply for SMD 5962-88588 are listed below for immediate acquisition only and shall be added to MIL-HDBK-103 during the next revision. MIL-HDBK-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103.

Standard microcircuit drawing PIN	Vendor CAGE number	Vendor similar PIN 1/
5962-8858801KX	2/	CY7C150-35KMB
5962-8858801LA	65786	CY7C150-35DMB
5962-8858801XX	2/	CY7C150-35LMB
5962-8858802KX	2/	CY7C150-25KMB
5962-8858802LA	65786	CY7C150-25DMB
5962-8858802XX	2/	CY7C150-25LMB
5962-8858803KX	2/	CY7C150-15KMB
5962-8858803LA	65786	CY7C150-15DMB
5962-8858803XX	2/	CY7C150-15LMB
5962-8858804KA	75569	P4C150-35FMB
5962-8858804LA	75569	P4C150-35DMB
5962-8858804XA	75569	P4C150-35LMB
5962-8858805KA	75569	P4C150-25FMB
5962-8858805LA	75569	P4C150-25DMB
5962-8858805XA	75569	P4C150-25LMB
5962-8858806KA	75569	P4C150-15FMB
5962-8858806LA	75569	P4C150-15DMB
5962-8858806XA	75569	P4C150-15LMB

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
2/ This part is not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
65786	Cypress Semiconductor 3901 N. First Street San Jose, CA 95134-1599
75569	Performance Semiconductor 630 East Weddell Drive Sunnyvale, CA 94089

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.