



## 40V 4.5A QUAD POWER HALF BRIDGE

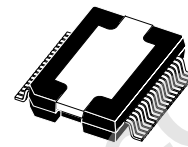
- MINIMUM INPUT OUTPUT PULSE WIDTH DISTORTION
- 200mΩ  $R_{dsON}$  COMPLEMENTARY DMOS OUTPUT STAGE
- CMOS COMPATIBLE LOGIC INPUTS
- THERMAL PROTECTION
- THERMAL WARNING OUTPUT
- UNDER VOLTAGE PROTECTION

### DESCRIPTION

STA508 is a monolithic quad half bridge stage in Multipower BCD Technology. The device can be used as dual bridge or reconfigured, by connecting CONFIG pin to V<sub>DD</sub> pin, as single bridge with double current capability, and as half bridge (Binary mode) with half current capability.

The device is particularly designed to make the output stage of a stereo All-Digital High Efficiency

### MULTIPOWER BCD TECHNOLOGY



PowerSO36

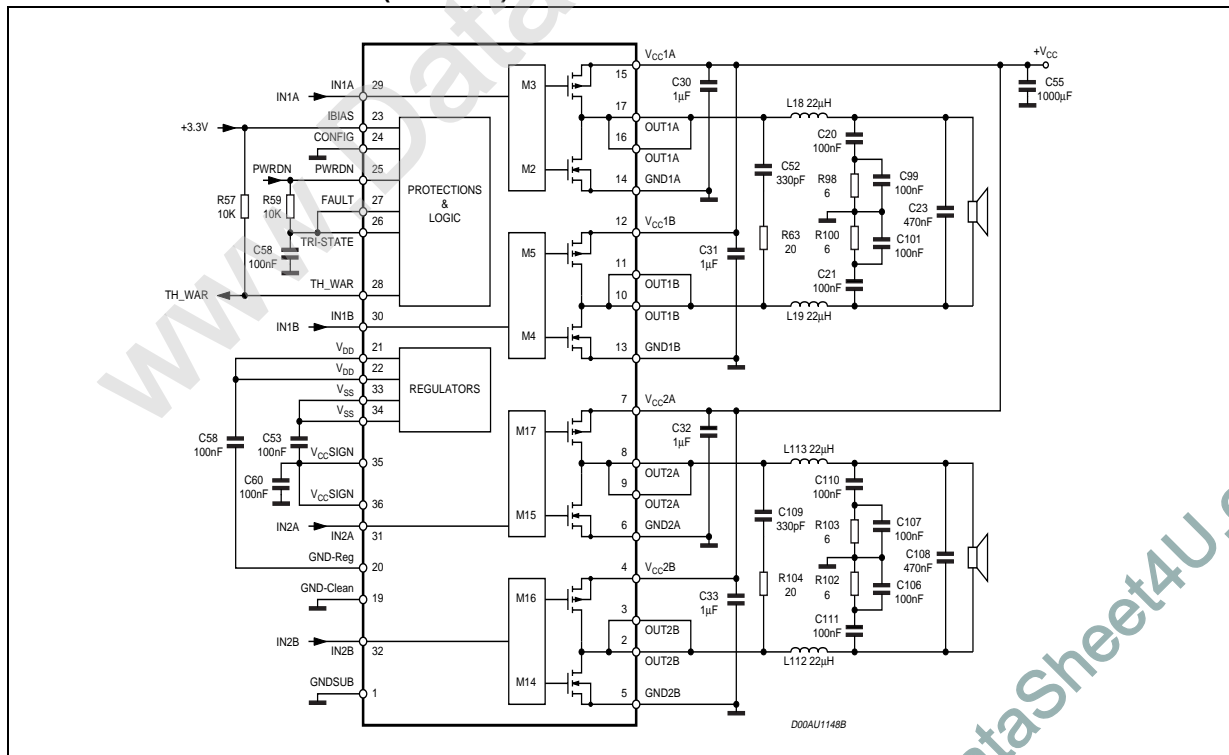
ORDERING NUMBER: STA508

(DDXT<sup>™</sup>) amplifier capable to deliver 80 + 80W @ THD = 10% at V<sub>CC</sub> 35V output power on 8Ω load.

In single BTL configuration is also capable to deliver a peak of 160W @ THD = 10% at V<sub>CC</sub> = 35V on 4Ω load (t ≤ 1sec)

The input pins have threshold proportional to I<sub>BIAS</sub> pin voltage.

### AUDIO APPLICATION CIRCUIT (Dual BTL)



**PIN FUNCTION**

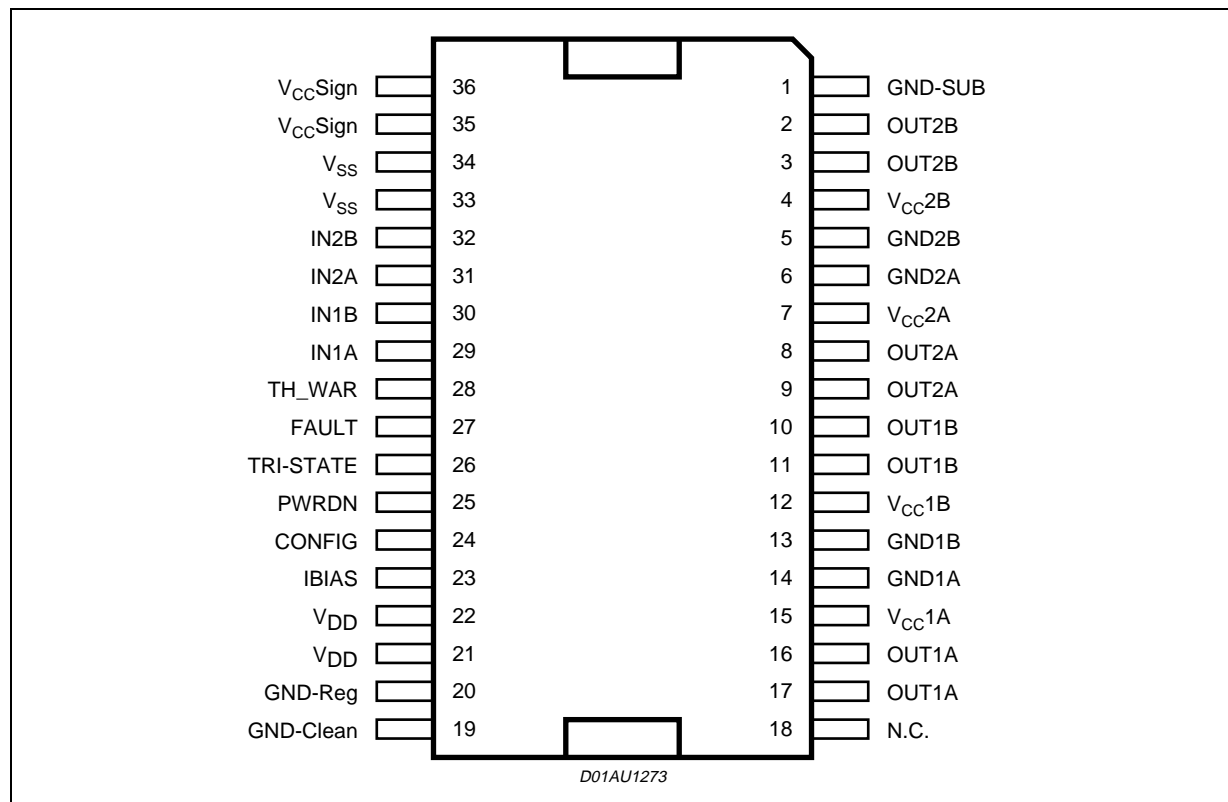
<b>N°</b>	<b>Pin</b>	<b>Description</b>
1	GND-SUB	Substrate Ground
35 ; 36	V <sub>CC</sub> Sign	Signal Positive Supply
15	V <sub>CC</sub> 1A	Positive Supply
12	V <sub>CC</sub> 1B	Positive Supply
7	V <sub>CC</sub> 2A	Positive Supply
4	V <sub>CC</sub> 2B	Positive Supply
14	GND1A	Negative Supply
13	GND1B	Negative Supply
6	GND2A	Negative Supply
5	GND2B	Negative Supply
16 ; 17	OUT1A	Output Half Bridge 1A
10 ; 11	OUT1B	Output Half Bridge 1B
8 ; 9	OUT2A	Output Half Bridge 2A
2 ; 3	OUT2B	Output Half Bridge 2B
29	IN1A	Input of Half Bridge 1A
30	IN1B	Input of Half Bridge 1B
31	IN2A	Input of Half Bridge 2A
32	IN2B	Input of Half Bridge 2B
21 ; 22	V <sub>dd</sub>	5V Regulator Referred to Ground
33 ; 34	V <sub>SS</sub>	5V Regulator Referred to +V <sub>CC</sub>
25	PWRDN	Stand-by pin
26	TRI-STATE	Hi-Z pin
27	FAULT	Fault pin Advisor
24	CONFIG	Configuration pin
28	TH-WAR	Thermal Warning Advisor
19	GND-clean	Logical Ground
23	IBIAS	High Logical State Setting Voltage
18	NC	Not Connected
20	GND-Reg	Ground for Regulator V <sub>dd</sub>

**FUNCTIONAL PIN STATUS**

PIN NAME	Logical value	IC -STATUS
FAULT	0	Fault detected (Short circuit, or Thermal ..)
FAULT (*)	1	Normal Operation
TRI-STATE	0	All powers in Hi-Z state
TRI-STATE	1	Normal operation
PWRDN	0	Low absorpion
PWRDN	1	Normal operation
THWAR	0	Temperature of the IC =130°C
THWAR(*)	1	Normal operation
CONFIG	0	Normal Operation
CONFIG(**)	1	OUT1A = OUT1B ; OUT2A=OUT2B (IF IN1A = IN1B; IN2A = IN2B)

(\*) : The pin is open collector. To have the high logic value, it needs to be pulled up by a resistor.  
 (\*\*): To put CONFIG = 1 means connect Pin 24 (CONFIG) to Pins 21, 22 (Vdd)

**PIN CONNECTION**



**THERMAL DATA**

Symbol	Description	Value	Unit
R <sub>th j-case</sub>	Thermal Resistance Junction-case	max 1.5	°C/W

**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
$V_{CE}$	DC Supply Voltage (Pin 4,7,12,15)	40	V
$V_{max}$	Maximum Voltage on pins 23 to 32	5.5	V
$P_{tot}$	Power Dissipation ( $T_{case} = 70^{\circ}C$ )	50	W
$T_{op}$	Operating Temperature Range	0 to 70	$^{\circ}C$
$T_{stg}, T_j$	Storage and Junction Temperature	-40 to 150	$^{\circ}C$

**ELECTRICAL CHARACTERISTICS** ( $I_{bias} = 3.3V$ ;  $V_{CC} = 30V$ ;  $T_{amb} = 25^{\circ}C$  unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$R_{dsON}$	Power Pchannel/Nchannel MOSFET RdsON	$I_d=1A$		200	270	m $\Omega$
$I_{dss}$	Power Pchannel/Nchannel leakage $I_{dss}$	$V_{CC} = 35V$			50	$\mu A$
$g_N$	Power Pchannel RdsON Matching	$I_d=1A$	95			%
$g_P$	Power Nchannel RdsON Matching	$I_d=1A$	95			%
$Dt_s$	Low current Dead Time (static)	see test circuit no.1; see fig. 1		10	20	ns
$Dt_d$	High current Dead Time (dynamic)	$L=22\mu H$ ; $C = 470nF$ ; $R_L = 8 \Omega$ $I_d=3.5A$ ; see fig. 3			50	ns
$t_{d ON}$	Turn-on delay time	Resistive load			100	ns
$t_{d OFF}$	Turn-off delay time	Resistive load			100	ns
$t_r$	Rise time	Resistive load; as fig.1			25	ns
$t_f$	Fall time	Resistive load; as fig. 1			25	ns
$V_{CC}$	Supply voltage operating voltage		9		36	V
$V_{IN-H}$	High level input voltage				$I_{bias}/2 + 300mV$	V
$V_{IN-L}$	Low level input voltage		$I_{bias}/2 - 300mV$			V
$I_{IN-H}$	Hi level Input current	Pin Voltage = $I_{bias}$		1		$\mu A$
$I_{IN-L}$	Low level input current	Pin Voltage = 0.3V		1		$\mu A$
$I_{PWRDN-H}$	Hi level PWRDN pin input current	$I_{bias} = 3.3V$		35		$\mu A$
$V_L$	Low logical state voltage $V_L$ (pin PWRDN, TRISTATE) (note 1)	$I_{bias} = 3.3V$	0.8			V
$V_H$	High logical state voltage $V_H$ (pin PWRDN, TRISTATE) (note 1)	$I_{bias} = 3.3V$			1.7	V

**ELECTRICAL CHARACTERISTICS** (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I <sub>VCC-PWRDN</sub>	Supply CURRENT from Vcc in Power Down	PWRDN = 0			3	mA
I <sub>FAULT</sub>	Output Current pins FAULT -TH-WARN when FAULT CONDITIONS	V <sub>pin</sub> = 3.3V		1		mA
I <sub>VCC-hiz</sub>	Supply Current from Vcc in Tri-state	V <sub>CC</sub> = 30V; Tri-state = 0		22		mA
I <sub>VCC</sub>	Supply Current from Vcc in operation both channel switching)	V <sub>CC</sub> =30V; Input Pulse width = 50% Duty; Switching Frequency = 384KHz; No LC filters;		80		mA
I <sub>VCC-q</sub>	Isc (short circuit current limit) (note 2)		4.5	6	9	A
V <sub>OUT-SH</sub>	Undervoltage protection threshold			7		V
V <sub>OV</sub>	Output minimum pulse width	No Load	70		150	ns

Notes: 1. The following table explains the VL, VH variation with I<sub>bias</sub>

I <sub>bias</sub>	VL <sub>min</sub>	VH <sub>max</sub>	Unit
2.7	0.7	1.5	V
3.3	0.8	1.7	V
5	0.85	1.85	V

Note 2: If used in single BTL configuration, the device may be not short circuit protected

**LOGIC TRUTH TABLE** (see fig. 2)

TRI-STATE	INxA	INxB	Q1	Q2	Q3	Q4	OUTPUT MODE
0	x	x	OFF	OFF	OFF	OFF	Hi-Z
1	0	0	OFF	OFF	ON	ON	DUMP
1	0	1	OFF	ON	ON	OFF	NEGATIVE
1	1	0	ON	OFF	OFF	ON	POSITIVE
1	1	1	ON	ON	OFF	OFF	Not used

Figure 1. Test Circuit.

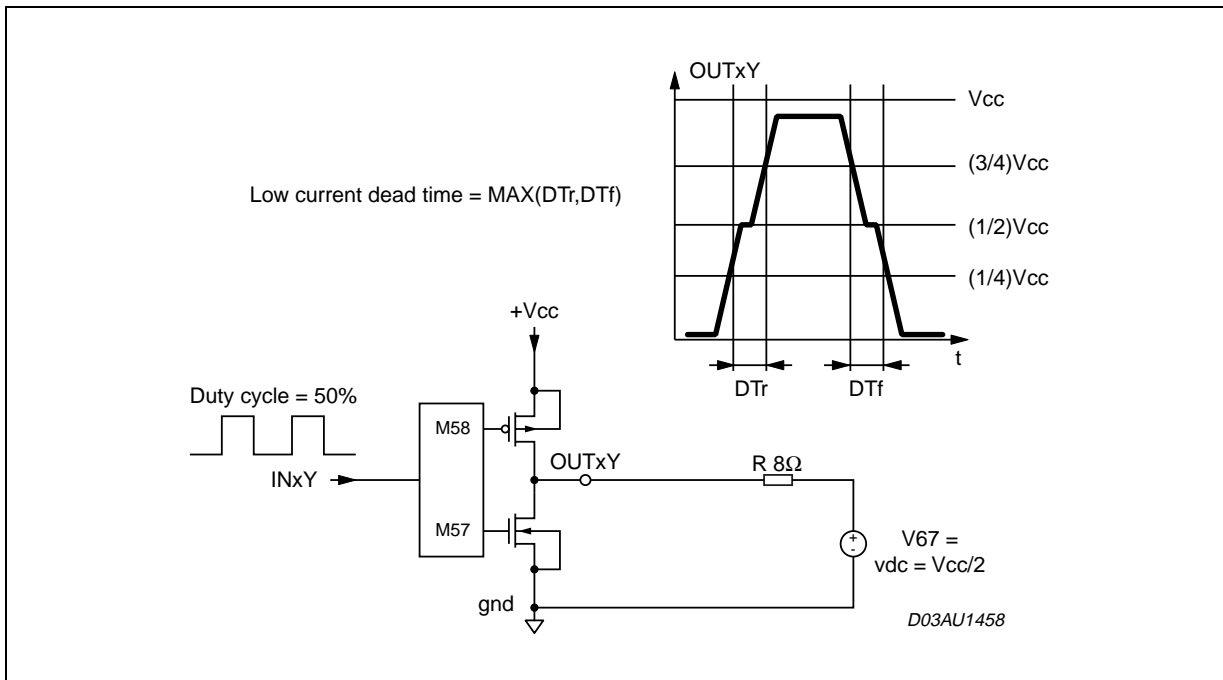


Figure 2.

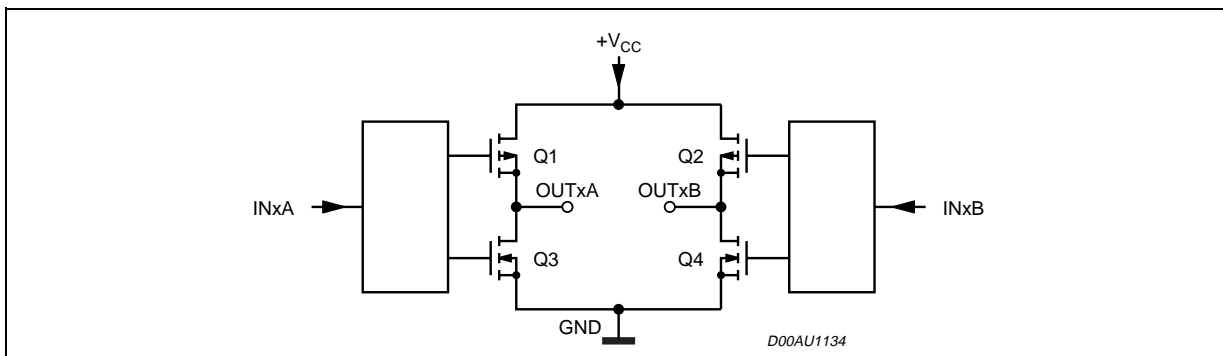


Figure 3.

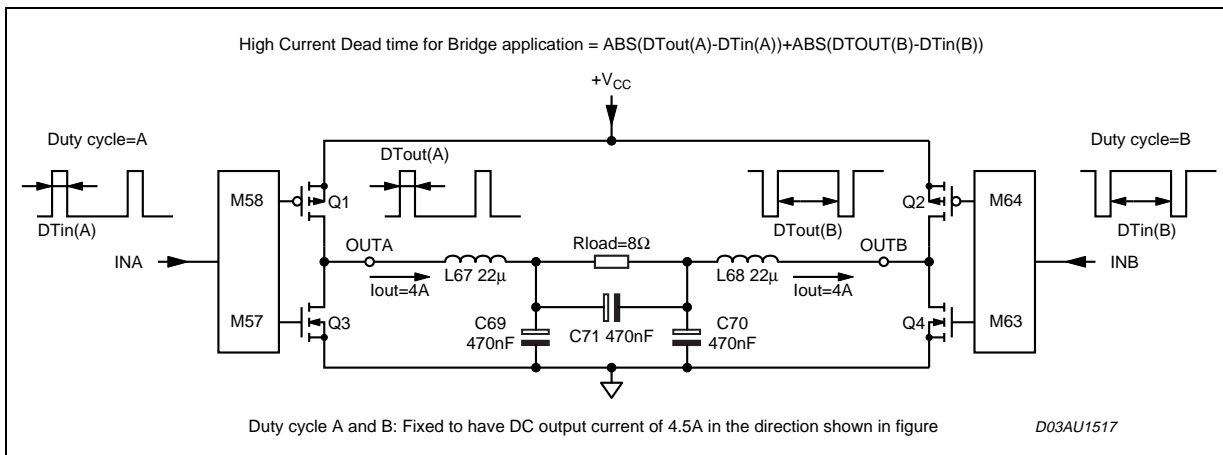


Figure 4. Typical Single BTL Configuration

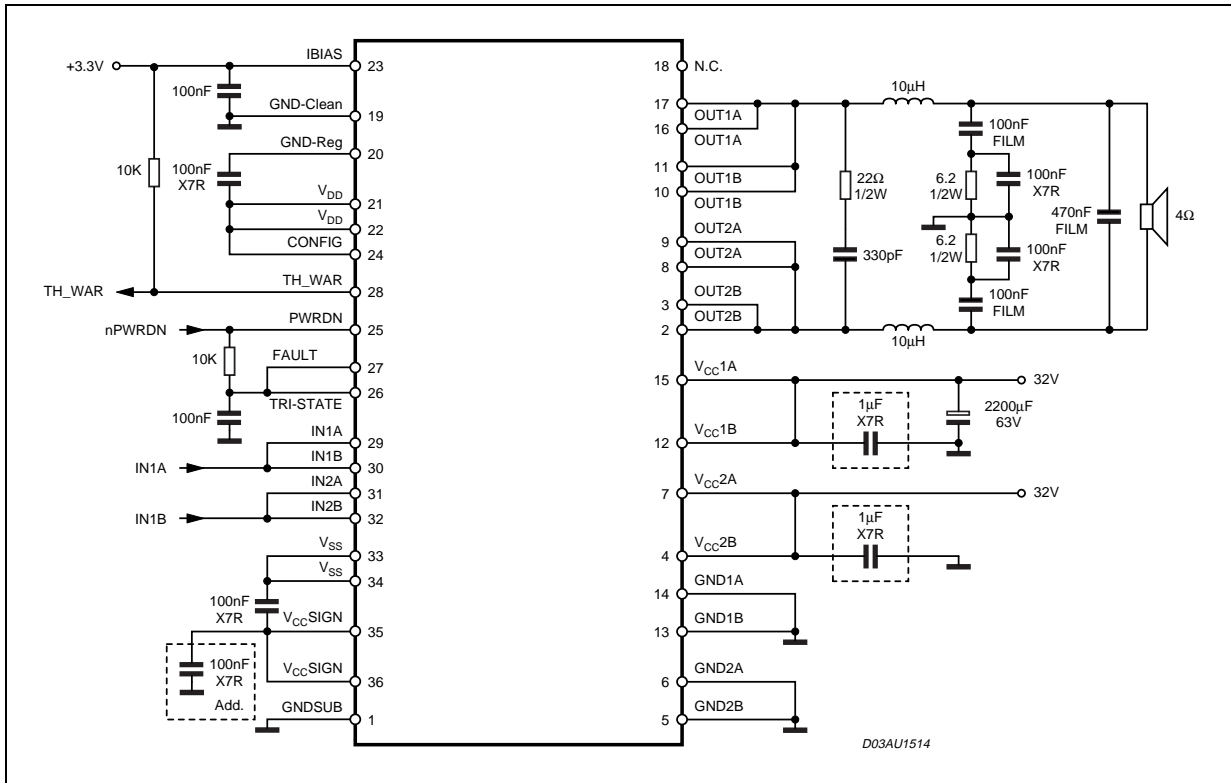
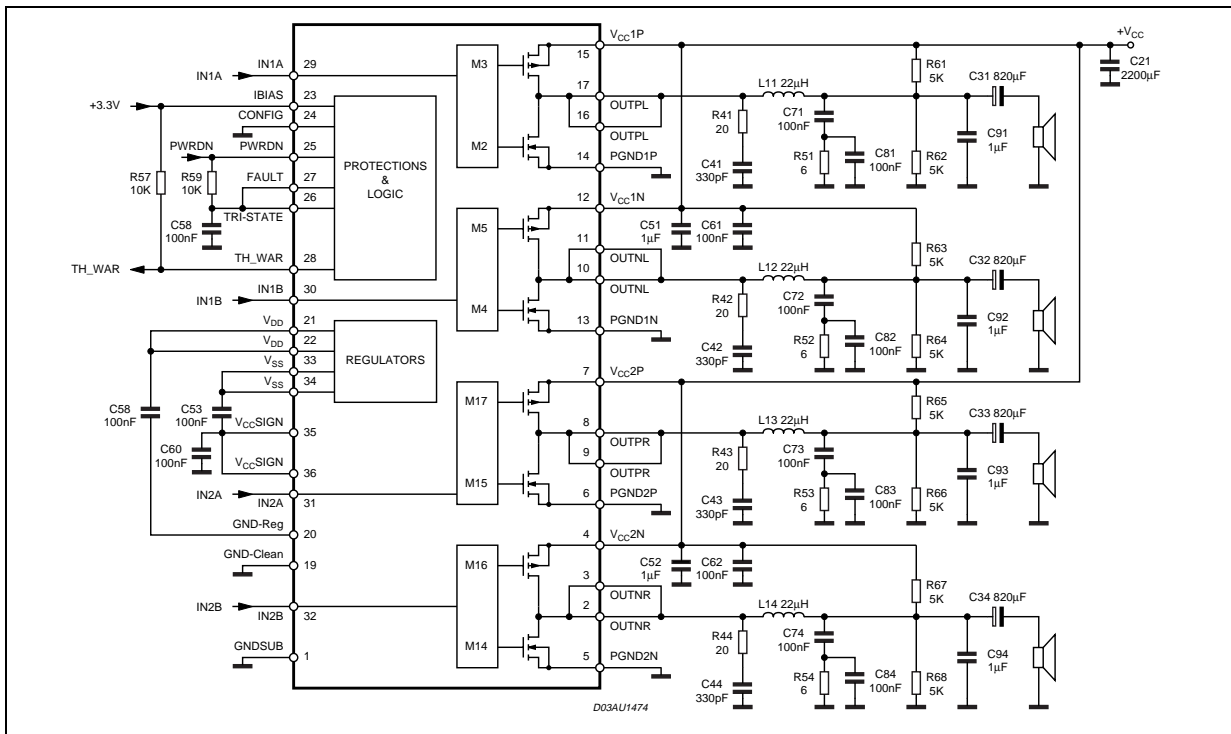


Figure 5. Typical Quad Half Bridge Configuration

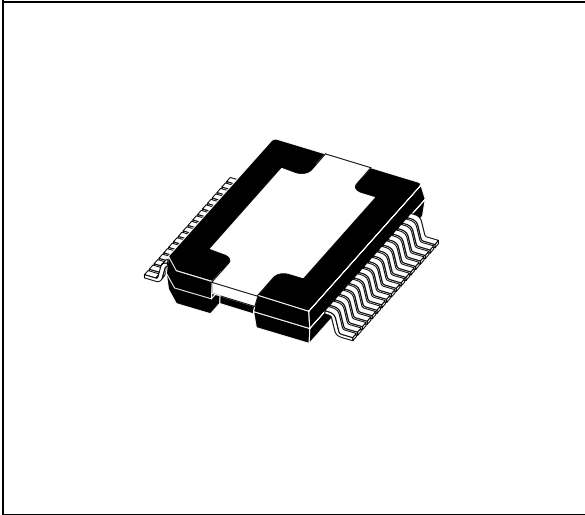


For more information refer to the application notes AN1456 and AN1661

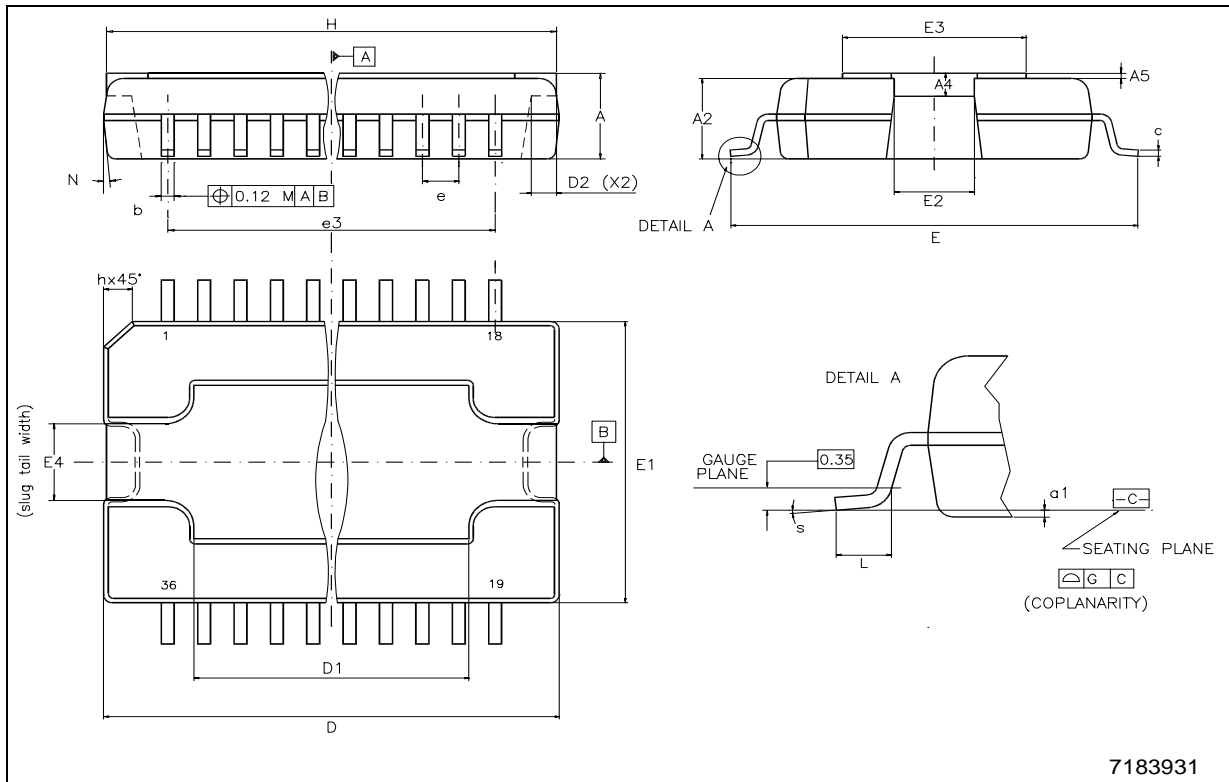
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	3.25		3.5	0.128		0.138
A2			3.3			0.13
A4	0.8		1	0.031		0.039
A5		0.2			0.008	
a1	0		0.075	0		0.003
b	0.22		0.38	0.008		0.015
c	0.23		0.32	0.009		0.012
D	15.8		16	0.622		0.630
D1	9.4		9.8	0.37		0.38
D2		1			0.039	
E	13.9		14.5	0.547		0.57
E1	10.9		11.1	0.429		0.437
E2			2.9			0.114
E3	5.8		6.2	0.228		0.244
E4	2.9		3.2	0.114		1.259
e		0.65			0.026	
e3		11.05			0.435	
G	0		0.075	0		0.003
H	15.5		15.9	0.61		0.625
h			1.1			0.043
L	0.8		1.1	0.031		0.043
N	10° (max)					
s	8° (max)					

- (1) "D and E1" do not include mold flash or protusions.  
Mold flash or protusions shall not exceed 0.15mm (0.006")
- (2) No intrusion allowed inwards the leads.

**OUTLINE AND MECHANICAL DATA**



**PowerSO36 (SLUG UP)**



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