

IMSH1G[U/E]03A1F1C(T)
IMSH2G[U/E]13A1F1C(T)

*240-Pin DDR3 Unbuffered Memory Modules
1-GByte and 2-GByte
EU RoHS compliant*

Advance
Internet Data Sheet

Rev. 0.63

IMSH[1G/2G][U/E]x3A1F1C(T)
DDR3 Unbuffered DIMM

IMSH1G[U/E]03A1F1C(T), IMSH2G[U/E]13A1F1C(T)	
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All	Data sheet for 1GByte and 2GByte Unbuffered DIMM Product Family.

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1 Overview

This chapter gives an overview of the 240-pin Unbuffered DDR3 Dual-In-Line memory modules product family and describes its main characteristics.

1.1 Features

- 240-pin 8-Byte DDR3 SDRAM unbuffered dual-in-line memory modules.
- Module organization: 128M × 64, 256M × 64, 128M × 72, 256M × 72
Chip organization: 128M × 8
- PC3-12800, PC3-10600, PC3-8500 and PC3-6400 module speed grades.
- 2GB, 1GB, 512MB modules built with 1Gb DDR3 SDRAMs in packages PG-TFBGA-78.
- DDR3 SDRAMs with a single 1.5 V (± 0.075 V) power supply.
- Asynchronous Reset.
- Programmable CAS Latency, CAS Write Latency, Additive Latency, Burst Length and Burst Type.
- On-Die-Termination (ODT) and Dynamic ODT for improved signal integrity.
- Refresh, Self Refresh and Power Down Modes.
- ZQ Calibration for output driver and ODT.
- System Level Timing Calibration Support via Write Leveling and Multi Purpose Register (MPR) Read Pattern.
- Serial Presence Detect with EEPROM.
- Thermal sensor functionality supported.
- UDIMM dimensions: 133.35 mm x 30 mm.
- Based on standard reference raw cards: 'A', 'B', 'D', and 'E'.
- RoHS compliant products¹⁾.

TABLE 1

Performance Table for DDR3–1600 and DDR3–1333

QAG Speed Code		-16J	-13G	-13H	Unit	Note ¹⁾
Module Speed Bin	PC3	-12800J	-10600G	-10600H		
Device Speed Bin	DDR3	-1600J	-1333G	-1333H		
CL- <i>n</i> _{RCD} - <i>n</i> _{RP}		10-10-10	8-8-8	9-9-9		
CL and CWL settings for maximum clock frequency		CL = 10 CWL = 8	CL = 8 CWL = 7	CL = 9 CWL = 7	MHz	
Maximum Clock Frequency and Data Rate with above CL and CWL settings		800 1600	667 1333	667 1333	MHz Mb/s	
Minimum Clock Frequency and Data Rate with above CL and CWL settings		667 1333	533 1066	533 1066	MHz Mb/s	

1) The available CL and CWL settings depend on the SDRAM device speed bin. The CL setting and CWL setting result in maximum but also minimum clock frequency requirements. When making a selection of operating clock frequency, both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting. For details, refer to **Chapter 4.1** Speed Bins.

1) RoHS Compliant Product: Restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment as defined in the directive 2002/95/EC issued by the European Parliament and of the Council of 27 January 2003. These substances include mercury, lead, cadmium, hexavalent chromium, polybrominated biphenyls and polybrominated biphenyl ethers. For more information please visit www.qimonda.com/green_products.



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TABLE 2

Performance Table for DDR3–1066 and DDR3–800

QAG Speed Code		–10F	–10G	–08D	–08E	Unit	Note 1)
Module Speed Bin	PC3	–8500F	–8500G	–6400D	–6400E		
Device Speed Bin	DDR3	–1066F	–1066G	–800D	–800E		
CL- <i>n</i> _{RCD} - <i>n</i> _{RP}		7-7-7	8-8-8	5-5-5	6-6-6		
CL and CWL settings for maximum clock frequency		CL = 7 CWL = 6	CL = 8 CWL = 6	CL = 5 CWL = 5	CL = 6 CWL = 5	MHz	
Maximum Clock Frequency and Data Rate with above CL and CWL settings		533 1066	533 1066	400 800	400 800	MHz Mb/s	
Minimum Clock Frequency and Data Rate with above CL and CWL settings		400 800	400 800	300 600	300 600	MHz Mb/s	

1) The available CL and CWL settings depend on the SDRAM device speed bin. The CL setting and CWL setting result in maximum but also minimum clock frequency requirements. When making a selection of operating clock frequency, both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting. For details, refer to [Chapter 4.1](#) Speed Bins.



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1.2 Description

Qimonda IMSH[1G/2G][U/E]x3A1F1C(T) are Unbuffered DIMM family with 30 mm height based on DDR3 SDRAM technology. DIMMs are available non-ECC modules in 128M × 64 (1GB), 256M × 64 (2GB), and as ECC modules in 128M × 72 (1GB), 256M × 72 (2GB) organization and density, intended for mounting into 240 pin connector sockets.

The memory array is designed with 1Gb Double Data Rate (DDR3) Synchronous DRAMs. De-coupling capacitors, stub resistors, calibration resistors and termination resistors are mounted on the PCB board. The DIMMs feature serial presence detect based on a 256 byte serial EEPROM device using the 2-pin I²C protocol. The first 176 bytes are programmed with module specific SPD data.



TABLE 3
Ordering Information Table for Modules without Thermal Sensor

QAG Part Number	Compliance Code	Description
1024 MByte Non-ECC Unbuffered DIMM IMSH1GU03A1F1C		
IMSH1GU03A1F1C-08D	1GB 1R×8 PC3-6400U-5-10-A0	240-pin 1024 MByte DDR3 Unbuffered DIMM with one rank for non-ECC applications. The memory rank consists of eight DDR3 components in x8 organization. Standard reference card A is used on this assembly Used DDR3 SDRAM Component Part Number: IDSH1G-03A1F1C Density: 1Gbit Organization: 128Mbit × 8 Address Bits (Row/Column/Bank): 14/10/3
IMSH1GU03A1F1C-08E	1GB 1R×8 PC3-6400U-6-10-A0	
IMSH1GU03A1F1C-10F	1GB 1R×8 PC3-8500U-7-10-A0	
IMSH1GU03A1F1C-10G	1GB 1R×8 PC3-8500U-8-10-A0	
IMSH1GU03A1F1C-13G	1GB 1R×8 PC3-10600U-8-10-A0	
IMSH1GU03A1F1C-13H	1GB 1R×8 PC3-10600U-9-10-A0	
IMSH1GU03A1F1C-16J	1GB 1R×8 PC3-12800U-10-10-A0	
2048 MByte Non-ECC Unbuffered DIMM IMSH2GU13A1F1C		
IMSH2GU13A1F1C-08D	2GB 2R×8 PC3-6400U-5-10-B0	240-pin 2048 MByte DDR3 Unbuffered DIMM with two ranks for non-ECC applications. Each memory rank consists of eight DDR3 components in x8 organization. Standard reference card B is used on this assembly Used DDR3 SDRAM Component Part Number: IDSH1G-03A1F1C Density: 1Gbit Organization: 128Mbit × 8 Address Bits (Row/Column/Bank): 14/10/3
IMSH2GU13A1F1C-08E	2GB 2R×8 PC3-6400U-6-10-B0	
IMSH2GU13A1F1C-10F	2GB 2R×8 PC3-8500U-7-10-B0	
IMSH2GU13A1F1C-10G	2GB 2R×8 PC3-8500U-8-10-B0	
IMSH2GU13A1F1C-13G	2GB 2R×8 PC3-10600U-8-10-B0	
IMSH2GU13A1F1C-13H	2GB 2R×8 PC3-10600U-9-10-B0	
IMSH2GU13A1F1C-16J	2GB 2R×8 PC3-12800U-10-10-B0	



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TABLE 4

Ordering Information Table for Modules with Thermal Sensor

QAG Part Number	Compliance Code	Description
1024 MByte ECC Unbuffered DIMM IMSH1GE03A1F1CT		
IMSH1GE03A1F1CT08D	1G 1Rx8 PC3-6400E-5-10-D0	240-pin 1024 MByte DDR3 Unbuffered DIMM with one rank and On-DIMM Thermal Sensor for ECC applications. The memory rank consists of nine DDR3 components in x8 organization. Standard reference card D is used on this assembly Used DDR3 SDRAM Component Part Number: IDSH1G-03A1F1C Density: 1Gbit Organization: 128Mbit x 8 Address Bits (Row/Column/Bank): 14/10/3
IMSH1GE03A1F1CT08E	1G 1Rx8 PC3-6400E-6-10-D0	
IMSH1GE03A1F1CT10F	1G 1Rx8 PC3-8500E-7-10-D0	
IMSH1GE03A1F1CT10G	1G 1Rx8 PC3-8500E-8-10-D0	
IMSH1GE03A1F1CT13G	1G 1Rx8 PC3-10600E-8-10-D0	
IMSH1GE03A1F1CT13H	1G 1Rx8 PC3-10600E-9-10-D0	
2048 MByte ECC Unbuffered DIMM IMSH2GE13A1F1CT		
IMSH2GE13A1F1CT08D	2GB 2Rx8 PC3-6400E-5-10-E0	240-pin 2048 MByte DDR3 Unbuffered DIMM with two ranks and On-DIMM Thermal Sensor for ECC applications. Each memory rank consists of nine DDR3 components in x8 organization. Standard reference card E is used on this assembly Used DDR3 SDRAM Component Part Number: IDSH1G-03A1F1C Density: 1Gbit Organization: 128Mbit x 8 Address Bits (Row/Column/Bank): 14/10/3
IMSH2GE13A1F1CT08E	2GB 2Rx8 PC3-6400E-6-10-E0	
IMSH2GE13A1F1CT10F	2GB 2Rx8 PC3-8500E-7-10-E0	
IMSH2GE13A1F1CT10G	2GB 2Rx8 PC3-8500E-8-10-E0	
IMSH2GE13A1F1CT13G	2GB 2Rx8 PC3-10600E-8-10-E0	
IMSH2GE13A1F1CT13H	2GB 2Rx8 PC3-10600E-9-10-E0	



2 Configuration

2.1 Pin Configuration

TABLE 5

Pin Configuration of DDR3 UDIMM - 240 Pins

Pin Name	EDA Signal Name ¹⁾	Pin No.	Pin Type	Buffer Type	Function
Clock Signals					
CK0	ck0_t	184	I	SSTL	Clock Inputs [1:0] and Differnetial Clock Inputs [1:0]
CK0	ck0_c	185	I	SSTL	
CK1	ck1_t	63	I	SSTL	
CK1	ck1_c	64	I	SSTL	
Control Signals					
CKE0	cke0	50	I	SSTL	Clock Enable [1:0]
CKE1/NC	cke1	169	I	SSTL	
ODT0	odt0	195	I	SSTL	On-Die Termination [1:0]
ODT1/NC	odt1	77	I		
S0	s0_n	193	I	SSTL	Chip Select [1:0]
S1/NC	s1_n	76	I	SSTL	
Command Signals					
RAS	ras_n	192	I	SSTL	Row Address Strobe
CAS	cas_n	74	I	SSTL	Column Address Strobe
WE	we_n	73	I	SSTL	Write Enable
Bank Address Signals					
BA0	ba0	71	I	SSTL	Bank Address Bus[2:0]
BA1	ba1	190	I	SSTL	
BA2	ba2	52	I	SSTL	
Address Signals					
A0	a0	188	I	SSTL	Address Bus [15:0]
A1	a1	181	I	SSTL	
A2	a2	61	I	SSTL	
A3	a3	180	I	SSTL	
A4	a4	59	I	SSTL	
A5	a5	58	I	SSTL	



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Pin Name	EDA Signal Name ¹⁾	Pin No.	Pin Type	Buffer Type	Function
A6	a6	178	I	SSTL	Address Bus [15:0]
A7	a7	56	I	SSTL	
A8	a8	177	I	SSTL	
A9	a9	175	I	SSTL	
A10/AP	a10	70	I	SSTL	
A11	a11	55	I	SSTL	
A12/ \overline{BC}	a12	174	I	SSTL	
A13	a13	196	I	SSTL	
A14	a14	172	I	SSTL	
A15/NC	a15	171	I	SSTL	
Data Signals					
DQ0	dq0	3	I/O	SSTL	Data Bus [63:0]
DQ1	dq1	4	I/O	SSTL	
DQ2	dq2	9	I/O	SSTL	
DQ3	dq3	10	I/O	SSTL	
DQ4	dq4	122	I/O	SSTL	
DQ5	dq5	123	I/O	SSTL	
DQ6	dq6	128	I/O	SSTL	
DQ7	dq7	129	I/O	SSTL	
DQ8	dq8	12	I/O	SSTL	
DQ9	dq9	13	I/O	SSTL	
DQ10	dq10	18	I/O	SSTL	
DQ11	dq11	19	I/O	SSTL	
DQ12	dq12	131	I/O	SSTL	
DQ13	dq13	132	I/O	SSTL	
DQ14	dq14	137	I/O	SSTL	
DQ15	dq15	138	I/O	SSTL	
DQ16	dq16	21	I/O	SSTL	
DQ17	dq17	22	I/O	SSTL	
DQ18	dq18	27	I/O	SSTL	
DQ19	dq19	28	I/O	SSTL	
DQ20	dq20	140	I/O	SSTL	
DQ21	dq21	141	I/O	SSTL	
DQ22	dq22	146	I/O	SSTL	
DQ23	dq23	147	I/O	SSTL	
DQ24	dq24	30	I/O	SSTL	
DQ25	dq25	31	I/O	SSTL	
DQ26	dq26	36	I/O	SSTL	
DQ27	dq27	37	I/O	SSTL	



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Pin Name	EDA Signal Name ¹⁾	Pin No.	Pin Type	Buffer Type	Function
DQ28	dq28	149	I/O	SSTL	Data Bus [63:0]
DQ29	dq29	150	I/O	SSTL	
DQ30	dq30	155	I/O	SSTL	
DQ31	dq31	156	I/O	SSTL	
DQ32	dq32	81	I/O	SSTL	
DQ33	dq33	82	I/O	SSTL	
DQ34	dq34	87	I/O	SSTL	
DQ35	dq35	88	I/O	SSTL	
DQ36	dq36	200	I/O	SSTL	
DQ37	dq37	201	I/O	SSTL	
DQ38	dq38	206	I/O	SSTL	
DQ39	dq39	207	I/O	SSTL	
DQ40	dq40	90	I/O	SSTL	
DQ41	dq41	91	I/O	SSTL	
DQ42	dq42	96	I/O	SSTL	
DQ43	dq43	97	I/O	SSTL	
DQ44	dq44	209	I/O	SSTL	
DQ45	dq45	210	I/O	SSTL	
DQ46	dq46	215	I/O	SSTL	
DQ47	dq47	216	I/O	SSTL	
DQ48	dq48	99	I/O	SSTL	
DQ49	dq49	100	I/O	SSTL	
DQ50	dq50	105	I/O	SSTL	
DQ51	dq51	106	I/O	SSTL	
DQ52	dq52	218	I/O	SSTL	
DQ53	dq53	219	I/O	SSTL	
DQ54	dq54	224	I/O	SSTL	
DQ55	dq55	225	I/O	SSTL	
DQ56	dq56	108	I/O	SSTL	
DQ57	dq57	109	I/O	SSTL	
DQ58	dq58	114	I/O	SSTL	
DQ59	dq59	115	I/O	SSTL	
DQ60	dq60	227	I/O	SSTL	
DQ61	dq61	228	I/O	SSTL	
DQ62	dq62	233	I/O	SSTL	
DQ63	dq63	234	I/O	SSTL	
CB0/NC	cb0	39	I/O	SSTL	Check Bit [7:0]
CB1/NC	cb1	40	I/O	SSTL	
CB2/NC	cb2	45	I/O	SSTL	



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Pin Name	EDA Signal Name ¹⁾	Pin No.	Pin Type	Buffer Type	Function
CB3/NC	cb3	46	I/O	SSTL	Check Bit [7:0]
CB4/NC	cb4	158	I/O	SSTL	
CB5/NC	cb5	159	I/O	SSTL	
CB6/NC	cb6	164	I/O	SSTL	
CB7/NC	cb7	165	I/O	SSTL	
DQS0	dqs0_t	7	I/O	SSTL	Data Strobe Signals [8:0] and Complementary Data Strobe Signals[8:0]
$\overline{\text{DQS0}}$	dqs0_c	6	I/O	SSTL	
DQS1	dqs1_t	16	I/O	SSTL	
$\overline{\text{DQS1}}$	dqs1_c	15	I/O	SSTL	
DQS2	dqs2_t	25	I/O	SSTL	
$\overline{\text{DQS2}}$	dqs2_c	24	I/O	SSTL	
DQS3	dqs3_t	34	I/O	SSTL	
$\overline{\text{DQS3}}$	dqs3_c	33	I/O	SSTL	
DQS4	dqs4_t	85	I/O	SSTL	
$\overline{\text{DQS4}}$	dqs4_c	84	I/O	SSTL	
DQS5	dqs5_t	94	I/O	SSTL	
$\overline{\text{DQS5}}$	dqs5_c	93	I/O	SSTL	
DQS6	dqs6_t	103	I/O	SSTL	
$\overline{\text{DQS6}}$	dqs6_c	102	I/O	SSTL	
DQS7	dqs7_t	112	I/O	SSTL	
$\overline{\text{DQS7}}$	dqs7_c	111	I/O	SSTL	
DQS8/NC	dqs8_t	43	I/O	SSTL	
$\overline{\text{DQS8/NC}}$	dqs8_c	42	I/O	SSTL	
DM0	dm0	125	I	SSTL	Data Mask Signals [8:0]
DM1	dm1	134	I	SSTL	
DM2	dm2	143	I	SSTL	
DM3	dm3	152	I	SSTL	
DM4	dm4	203	I	SSTL	
DM5	dm5	212	I	SSTL	
DM6	dm6	221	I	SSTL	
DM7	dm7	230	I	SSTL	
DM8/NC	dm8	161	I	SSTL	
EEPROM					
SCL	scl	118	I	CMOS	Serial Bus Clock
SDA	sda	238	I/O	OD	Serial Data Bus
SA0	sa0	117	I	CMOS	Serial Address Select Bus [2:0]
SA1	sa1	237	I	CMOS	
SA2	sa2	119	I	CMOS	
Power Supply					



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Pin Name	EDA Signal Name ¹⁾	Pin No.	Pin Type	Buffer Type	Function
V _{DD}	vdd	51, 54, 57, 60, 62, 65, 66, 69, 72, 75, 78, 170, 173, 176, 179, 182, 183, 186,	PWR	-	Power Supply
V _{DD}	vdd	189, 191, 194, 197	PWR	-	Power Supply
V _{SS}	vss	2, 5, 8, 11, 14, 17, 20, 23, 26, 29, 32, 35, 38, 41, 44, 47, 80, 83, 86, 89, 92, 95, 98, 101, 104, 107, 110, 113, 116, 121, 124, 127, 130, 133, 136, 139, 142, 145, 148, 151, 154, 157, 160, 163, 166, 199, 202, 205, 208, 211, 214, 217, 220, 223, 226, 229, 232, 235, 239	GND	-	Ground
V _{REF.DQ}	vrefdq	1	AI	-	Reference Voltage
V _{REF.CA}	vrefca	67	AI	-	Reference Voltage
V _{TT}	vtt	120 , 240	PWR	-	Termination Voltage
V _{DDSPD}	vddspd	236		-	EEPROM and Thermal Sensor Power Supply
Other Pins					
TEST/NC	-	167	I/O	-	TEST
EVENT / NC	event_n	187	O	-	EVENT
RESET	reset_n	168	I	CMOS	Asynchronous Reset
NC	nc	48, 49, 53, 68, 79, 126, 135, 144, 153, 162, 198, 204, 213, 222, 231			Not Connected

1) The EDA (Electronic Design Automation) Signal Name is used in Qimonda Simulation Models such as EBD (Electronic Board Description).

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Abbreviations for Pin Type

Abbreviation	Description
I	Standard Input pin only. Digital levels.
O	Standard Output pin only - Digital levels.
I/O	I/O is a bidirectional input/output signal.
AI	Input - Analog levels.
PWR	Power
GND	Ground
NC	Not Connected

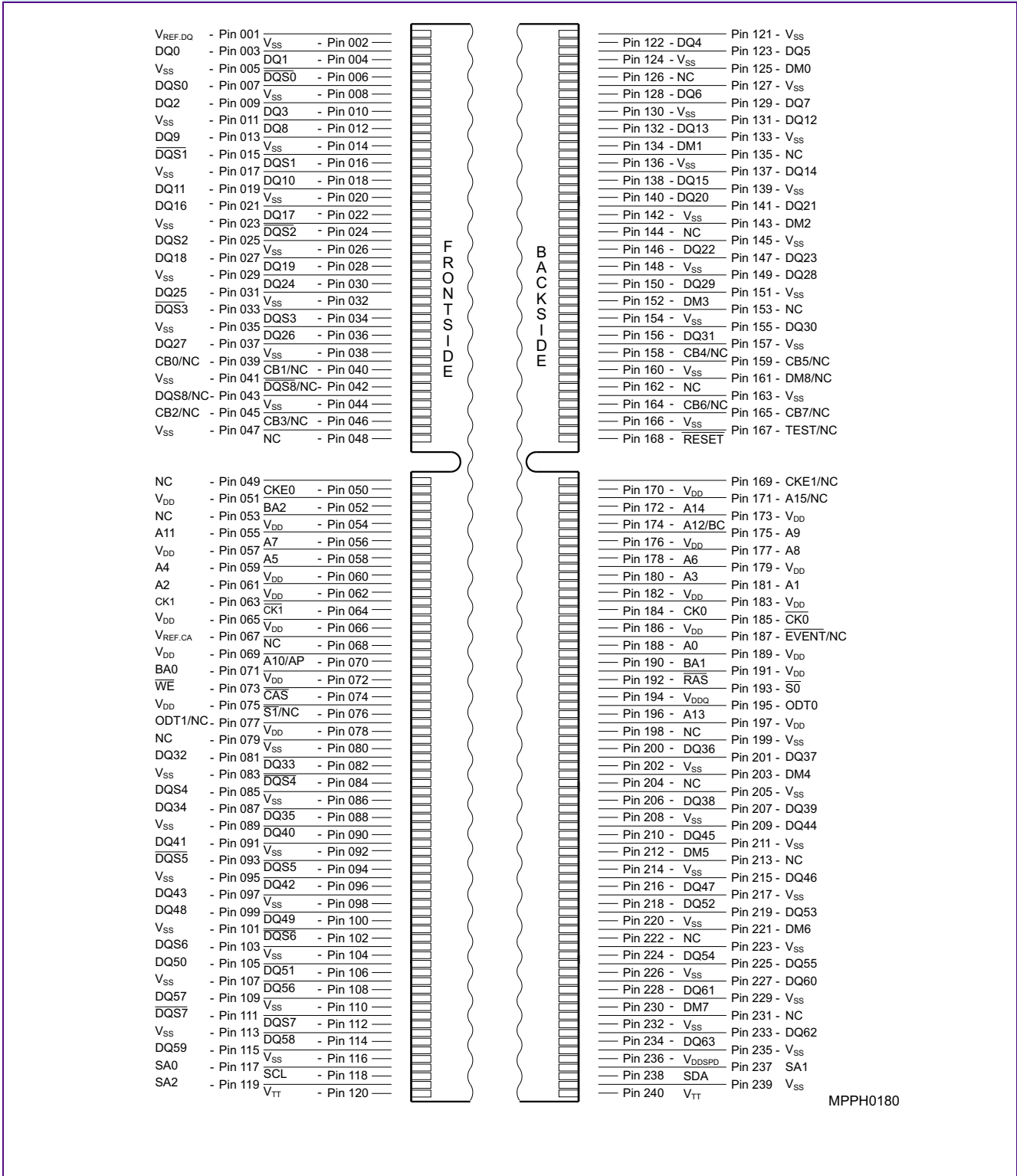
TABLE 7
Abbreviations for Buffer Type

Abbreviation	Description
SSTL	Serial Stub Terminated Logic
CMOS	CMOS Levels
OD	Open Drain. The corresponding pin has 2 operational states, active low and tri-state, and allows multiple devices to share as a wire-OR.



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FIGURE 1
Pin Configuration UDIMM - 240 Pin



MPPH0180



3 Operating Conditions

3.1 Absolute Maximum Ratings

TABLE 8
Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Note
		Min.	Max.		
Voltage on V_{DD} pin relative to V_{SS}	V_{DD}	-0.4	+1.975	V	1)
Voltage on V_{DDQ} pin relative to V_{SS}	V_{DDQ}	-0.4	+1.975	V	
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.4	+1.975	V	

1) V_{DD} and V_{DDQ} must be within 300mV of each other at all times. V_{REFDQ} and V_{REFCA} must not be greater than $0.6 \times V_{DDQ}$. When V_{DD} and V_{DDQ} are less than 500 mV, V_{REFDQ} and V_{REFCA} may be equal or less than 300 mV.

TABLE 9
Environmental Parameters

Parameter	Symbol	Rating		Unit	Note
		Min.	Max.		
Operating Temperature	T_{OPR}	0	55	°C	1)
Operating Humidity (relative)	H_{OPR}	10	90	%	
Storage Temperature	T_{STG}	-50	+100	°C	2)
Storage Humidity (without condensation)	H_{STG}	5	95	%	
Barometric Pressure (Operating and Storage)	P_{Bar}	69	105	KPascal	3)

- 1) The component maximum case temperature (t_{CASE}) shall not exceed the value specified in the DDR3 DRAM component specification..
 2) Storage Temperature is the case surface temperature on the center/top side of the SDRAM mentioned in Qimonda component datasheet.
 3) Up to 9850 ft.

Attention: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.



TABLE 10

DRAM Component Operating Temperature Range

Parameter	Symbol	Rating		Unit	Note
		Min.	Max.		
Normal Operating Temperature Range	T_{OPER}	0	85	°C	1)2)
Extended Temperature Range		85	95	°C	1)3)

- 1) Operating Temperature T_{OPER} is the case surface temperature on the center / top side of the SDRAM mentioned..
- 2) The Normal Temperature Range specifies the temperatures where all SDRAM specification will be supported.
- 3) Some application require operation of the DRAM in the Extended Temperature Range between 85 °C and 95 °C operating temperature. For more details please refer to Qimonda Component datasheet.

3.2 Recommended DC Operating Conditions

TABLE 11

DC Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply Voltage	V_{DD}	1.425	1.5	1.575	V	1)2)
Supply Voltage for EEPROM and Thermal Sensor	$V_{DD.SPD}$	3.0	3.3	3.6	V	1)2)
Supply Voltage for Output	V_{DDQ}	1.425	1.5	1.575	V	1)2)
Reference Voltage for DQ, DM inputs	$V_{REFDQ.DC}$	$0.49 \times V_{DD}$	$0.5 \times V_{DD}$	$0.51 \times V_{DD}$	V	3)4)
Reference Voltage for ADD, CMD inputs	$V_{REFCA.DC}$	$0.49 \times V_{DD}$	$0.5 \times V_{DD}$	$0.51 \times V_{DD}$	V	3)4)
Terminal Voltage	V_{TT}	$0.49 \times V_{DD}$	$0.5 \times V_{DD}$	$0.51 \times V_{DD}$	V	
External Calibration Resistor connected from ZQ pin to ground	R_{ZQ}	237.6	240.0	242.4	Ω	5)

- 1) V_{DDQ} tracks with V_{DD} . AC parameters are measured with V_{DD} and V_{DDQ} tied together
- 2) Under all conditions V_{DDQ} must be less than or equal to V_{DD} .
- 3) The ac peak noise on V_{REF} may not allow V_{REF} to deviate from $V_{REF.DC}$ by more than $\pm 1\% V_{DD}$ (for reference: approx. ± 15 mV).
- 4) For reference: approx. $V_{DD}/2 \pm 15$ mV.
- 5) The external calibration resistor R_{ZQ} can be time-shared among DRAMs in multi-rank DIMMs.



4 Speed Bins and Timing Parameters

AC timings are provided with $\overline{CK}/\overline{CK}$ and $\overline{DQS}/\overline{DQS}$ differential slew rate of 2.0 V/ns. Timings are further provided for calibrated OCD drive strength. The $\overline{CK}/\overline{CK}$ input reference level (for timing referenced to $\overline{CK} / \overline{CK}$) is the point at which \overline{CK} and \overline{CK} cross. The $\overline{DQS}/\overline{DQS}$ reference level (for timing referenced to $\overline{DQS}/\overline{DQS}$) is the point at which \overline{DQS} and \overline{DQS}

cross. Inputs are not recognized as valid until V_{REF} stabilizes. During the period before $V_{REF,CA}$ and $V_{REF,DQ}$ stabilizes, $CKE = 0.2 \times V_{DDQ}$ is recognized as low. The output timing reference voltage level is V_{TT} . For details of all relevant AC timing parameters see the QIMONDA DDR3 component datasheet.

4.1 Speed Bins

The following tables show DDR3 speed bins and relevant timing parameters. Other timing parameters are provided in the following chapter.

General Notes for Speed Bins:

- The CL setting and CWL setting result in $t_{CK,AVG,MIN}$ and $t_{CK,AVG,MAX}$ requirements. When making a selection of $t_{CK,AVG}$, both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting
- $t_{CK,AVG,MIN}$ limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be provided. An application should use the next smaller standard $t_{CK,AVG}$ value (2.5, 1.875, 1.5, or 1.25 ns) when calculating CL [nCK] = t_{AA} [ns] / $t_{CK,AVG}$ [ns], rounding up to the next 'Supported CL'
- $t_{CK,AVG,MAX}$ limits: Calculate $t_{CK,AVG} = t_{AA,MAX} / CL_{SELECTED}$ and round the resulting $t_{CK,AVG}$ down to the next valid speed bin limit (i.e. 3.3 ns or 2.5 ns or 1.875 ns or 1.25 ns). This result is $t_{CK,AVG,MAX}$ corresponding to $CL_{SELECTED}$

The absolute specification for all speed bins is T_{OPER} and $V_{DD} = V_{DDQ} = 1.5 V \pm 0.075 V$. In addition the following general notes apply.

- 'Reserved' settings are not allowed. User must program a different value
- Any DDR3-1066 speed bin also supports functional operation at lower frequencies as shown in the tables which are not subject to Production Tests but verified by Design/Characterization
- Any DDR3-1333 speed bin also supports functional operation at lower frequencies as shown in the tables which are not subject to Production Tests but verified by Design/Characterization
- Any DDR3-1600 speed bin also supports functional operation at lower frequencies as shown in the tables which are not subject to Production Tests but verified by Design/Characterization

TABLE 12

DDR3-800 Speed Bins and Operating Conditions

Speed Bin		DDR3-800D		DDR3-800E		Unit	Note
CL- n_{RCD} - n_{RP}		5-5-5		6-6-6			
QAG Partnumber Extension		-08D		-08E			
Parameter	Symbol	Min.	Max.	Min.	Max.		
Internal read command to first data	t_{AA}	12.5	20.0	15.0	20.0	ns	¹⁾
ACT to internal read or write delay time	t_{RCD}	12.5	—	15.0	—	ns	¹⁾
PRE command period	t_{RP}	12.5	—	15.0	—	ns	¹⁾
ACT to ACT or REF command period	t_{RC}	50.0	—	52.5	—	ns	¹⁾
Supported CL Settings	Sup_CL	5, 6		6		n_{CK}	¹⁾
Supported CWL Settings	Sup_CWL	5		5		n_{CK}	¹⁾



IMSH[1G/2G][U/E]x3A1F1C(T)
DDR3 Unbuffered DIMM

Speed Bin		DDR3-800D		DDR3-800E		Unit	Note
CL- n_{RCD} - n_{RP}		5-5-5		6-6-6			
QAG Partnumber Extension		-08D		-08E			
Parameter	Symbol	Min.	Max.	Min.	Max.		
Average Clock Period with CL = 5; CWL = 5	$t_{CK.AVG.CL05.CWL05}$	2.5	3.3	RESERVED		ns	1)2)
Average Clock Period with CL = 6; CWL = 5	$t_{CK.AVG.CL06.CWL05}$	2.5	3.3	2.5	3.3	ns	1)2)

- 1) Please refer to "General Notes for Speed Bins" at beginning of this chapter.
- 2) Max. limits are exclusive. E.g. if $t_{CK.AVG.MAX}$ value is 2.5 ns, $t_{CK.AVG}$ needs to be < 2.5 ns.

TABLE 13

DDR3-1066 Speed Bins and Operating Conditions

Speed Bin		DDR3-1066E		DDR3-1066F		DDR3-1066G		Unit	Note
CL- n_{RCD} - n_{RP}		6-6-6		7-7-7		8-8-8			
QAG Partnumber Extension		-10E		-10F		-10G			
Parameter	Symbol	Min.	Max.	Min.	Max.	Min.	Max.		
Internal read command to first data	t_{AA}	11.25	20.0	13.125	20.0	15.0	20.0	ns	1)
ACT to internal read or write delay time	t_{RCD}	11.25	—	13.125	—	15.0	—	ns	1)
PRE command period	t_{RP}	11.25	—	13.125	—	15.0	—	ns	1)
ACT to ACT or REF command period	t_{RC}	48.75	—	50.625	—	52.5	—	ns	1)
Supported CL Settings	Sup_CL	5, 6, 7, 8		6, 7, 8		6, 8		n_{CK}	1)
Supported CWL Settings	Sup_CWL	5, 6		5, 6		5, 6		n_{CK}	1)
Average Clock Period with CL = 5; CWL = 5	$t_{CK.AVG.CL05.CWL05}$	2.5	3.3	RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 5; CWL = 6	$t_{CK.AVG.CL05.CWL06}$	RESERVED		RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 6; CWL = 5	$t_{CK.AVG.CL06.CWL05}$	2.5	3.3	2.5	3.3	2.5	3.3	ns	1)2)
Average Clock Period with CL = 6; CWL = 6	$t_{CK.AVG.CL06.CWL06}$	1.875	2.5	RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 7; CWL = 5	$t_{CK.AVG.CL07.CWL05}$	RESERVED		RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 7; CWL = 6	$t_{CK.AVG.CL07.CWL06}$	1.875	2.5	1.875	2.5	RESERVED		ns	1)2)
Average Clock Period with CL = 8; CWL = 5	$t_{CK.AVG.CL08.CWL05}$	RESERVED		RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 8; CWL = 6	$t_{CK.AVG.CL08.CWL06}$	1.875	2.5	1.875	2.5	1.875	2.5	ns	1)2)

- 1) Please refer to "General Notes for Speed Bins" at beginning of this chapter.
- 2) Max. limits are exclusive. E.g. if $t_{CK.AVG.MAX}$ value is 2.5 ns, $t_{CK.AVG}$ needs to be < 2.5 ns.



TABLE 14
DDR3-1333 Speed Bins and Operating Conditions

Speed Bin		DDR3-1333G		DDR3-1333H		Unit	Note
CL-nRCD-nRP		8-8-8		9-9-9			
QAG Partnumber Extension		-13G		-13H			
Parameter	Symbol	Min.	Max.	Min.	Max.		
Internal read command to first data	t_{AA}	12.0	20.0	13.5	20.0	ns	1)
ACT to internal read or write delay time	t_{RCD}	12.0	—	13.5	—	ns	1)
PRE command period	t_{RP}	12.0	—	13.5	—	ns	1)
ACT to ACT or REF command period	t_{RC}	48.0	—	49.5	—	ns	1)
Supported CL Settings	Sup_CL	5, 6, 7, 8, 9, 10		6, 8, 9, 10		n_{CK}	1)
Supported CWL Settings	Sup_CWL	5, 6, 7		5, 6, 7		n_{CK}	1)
Average Clock Period with CL = 5; CWL = 5	$t_{CK.AVG.CL05.CWL05}$	2.5	3.3	RESERVED		ns	1)2)
Average Clock Period with CL = 5; CWL = 6	$t_{CK.AVG.CL05.CWL06}$	RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 5; CWL = 7	$t_{CK.AVG.CL05.CWL07}$	RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 6; CWL = 5	$t_{CK.AVG.CL06.CWL05}$	2.5	3.3	2.5	3.3	ns	1)2)
Average Clock Period with CL = 6; CWL = 6	$t_{CK.AVG.CL06.CWL06}$	RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 6; CWL = 7	$t_{CK.AVG.CL06.CWL07}$	RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 7; CWL = 5	$t_{CK.AVG.CL07.CWL05}$	RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 7; CWL = 6	$t_{CK.AVG.CL07.CWL06}$	1.875	2.5	RESERVED		ns	1)2)
Average Clock Period with CL = 7; CWL = 7	$t_{CK.AVG.CL07.CWL07}$	RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 8; CWL = 5	$t_{CK.AVG.CL08.CWL05}$	RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 8; CWL = 6	$t_{CK.AVG.CL08.CWL06}$	1.875	2.5	1.875	2.5	ns	1)2)
Average Clock Period with CL = 8; CWL = 7	$t_{CK.AVG.CL08.CWL07}$	1.5	1.875	RESERVED		ns	1)2)
Average Clock Period with CL = 9; CWL = 5	$t_{CK.AVG.CL09.CWL05}$	RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 9; CWL = 6	$t_{CK.AVG.CL09.CWL06}$	RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 9; CWL = 7	$t_{CK.AVG.CL09.CWL07}$	1.5	1.875	1.5	1.875	ns	1)2)
Average Clock Period with CL = 10; CWL = 5	$t_{CK.AVG.CL10.CWL05}$	RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 10; CWL = 6	$t_{CK.AVG.CL10.CWL06}$	RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 10; CWL = 7	$t_{CK.AVG.CL10.CWL07}$	1.5	1.875	1.5	1.875	ns	1)2)

- 1) Please refer to "General Notes for Speed Bins" at beginning of this chapter.
- 2) Max. limits are exclusive. E.g. if $t_{CK.AVG.MAX}$ value is 2.5 ns, $t_{CK.AVG}$ needs to be < 2.5 ns.



TABLE 15

DDR3-1600 Speed Bins and Operating Conditions

Speed Bin		DDR3-1600G		DDR3-1600H		DDR3-1600J		DDR3-1600K		Unit	Note
CL-nRCD-nRP		8-8-8		9-9-9		10-10-10		11-11-11			
QAG Partnumber Extension		-16G		-16H		-16J		-16K			
Parameter	Symbol	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Internal read command to first data	t_{AA}	10.0	20.0	11.25	20.0	12.5	20.0	13.75	20.0	ns	1)
ACT to internal read or write delay time	t_{RCD}	10.0	—	11.25	—	12.5	—	13.75	—	ns	1)
PRE command period	t_{RP}	10.0	—	11.25	—	12.5	—	13.75	—	ns	1)
ACT to ACT or REF command period	t_{RC}	45.0	—	46.25	—	47.5	—	48.75	—	ns	1)
Supported CL Settings	Sup_CL	5, 6, 7, 8, 9, 10, 11		5, 6, 7, 8, 9, 10, 11		5, 6, 7, 8, 9, 10, 11		6, 8, 10, 11		n_{CK}	1)
Supported CWL Settings	Sup_CWL	5, 6, 7, 8		5, 6, 7, 8		5, 6, 7, 8		5, 6, 7, 8		n_{CK}	1)
Average Clock Period with CL = 5; CWL = 5	$t_{CK.AVG.CL05.CWL05}$	2.5	3.3	2.5	3.3	2.5	3.3	RESERVED		ns	1)2)
Average Clock Period with CL = 5; CWL = 6	$t_{CK.AVG.CL05.CWL06}$	RESERVED		RESERVED		RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 5; CWL = 7	$t_{CK.AVG.CL05.CWL07}$	RESERVED		RESERVED		RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 5; CWL = 8	$t_{CK.AVG.CL05.CWL08}$	RESERVED		RESERVED		RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 6; CWL = 5	$t_{CK.AVG.CL06.CWL05}$	2.5	3.3	2.5	3.3	2.5	3.3	2.5	3.3	ns	1)2)
Average Clock Period with CL = 6; CWL = 6	$t_{CK.AVG.CL06.CWL06}$	1.875	2.5	1.875	2.5	RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 6; CWL = 7	$t_{CK.AVG.CL06.CWL07}$	RESERVED		RESERVED		RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 6; CWL = 8	$t_{CK.AVG.CL06.CWL08}$	RESERVED		RESERVED		RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 7; CWL = 5	$t_{CK.AVG.CL07.CWL05}$	RESERVED		RESERVED		RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 7; CWL = 6	$t_{CK.AVG.CL07.CWL06}$	1.875	2.5	1.875	2.5	1.875	2.5	RESERVED		ns	1)2)
Average Clock Period with CL = 7; CWL = 7	$t_{CK.AVG.CL07.CWL07}$	1.5	1.875	RESERVED		RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 7; CWL = 8	$t_{CK.AVG.CL07.CWL08}$	RESERVED		RESERVED		RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 8; CWL = 5	$t_{CK.AVG.CL08.CWL05}$	RESERVED		RESERVED		RESERVED		RESERVED		ns	1)2)



IMSH[1G/2G][U/E]x3A1F1C(T)
DDR3 Unbuffered DIMM

Speed Bin		DDR3-1600G		DDR3-1600H		DDR3-1600J		DDR3-1600K		Unit	Note
CL-nRCD-nRP		8-8-8		9-9-9		10-10-10		11-11-11			
QAG Partnumber Extension		-16G		-16H		-16J		-16K			
Parameter	Symbol	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Average Clock Period with CL = 8; CWL = 6	$t_{CK.AVG.CL08.CWL06}$	1.875	2.5	1.875	2.5	1.875	2.5	1.875	2.5	ns	1)2)
Average Clock Period with CL = 8; CWL = 7	$t_{CK.AVG.CL08.CWL07}$	1.5	1.875	1.5	1.875	RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 8; CWL = 8	$t_{CK.AVG.CL08.CWL08}$	1.25	1.5	RESERVED		RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 9; CWL = 5	$t_{CK.AVG.CL09.CWL05}$	RESERVED		RESERVED		RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 9; CWL = 6	$t_{CK.AVG.CL09.CWL06}$	RESERVED		RESERVED		RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 9; CWL = 7	$t_{CK.AVG.CL09.CWL07}$	1.5	1.875	1.5	1.875	1.5	1.875	RESERVED		ns	1)2)
Average Clock Period with CL = 9; CWL = 8	$t_{CK.AVG.CL09.CWL08}$	1.25	1.5	1.25	1.5	RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 10; CWL = 5	$t_{CK.AVG.CL10.CWL05}$	RESERVED		RESERVED		RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 10; CWL = 6	$t_{CK.AVG.CL10.CWL06}$	RESERVED		RESERVED		RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 10; CWL = 7	$t_{CK.AVG.CL10.CWL07}$	1.5	1.875	1.5	1.875	1.5	1.875	1.5	1.875	ns	1)2)
Average Clock Period with CL = 10; CWL = 8	$t_{CK.AVG.CL10.CWL08}$	1.25	1.5	1.25	1.5	1.25	1.5	RESERVED		ns	1)2)
Average Clock Period with CL = 11; CWL = 5	$t_{CK.AVG.CL11.CWL05}$	RESERVED		RESERVED		RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 11; CWL = 6	$t_{CK.AVG.CL11.CWL06}$	RESERVED		RESERVED		RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 11; CWL = 7	$t_{CK.AVG.CL11.CWL07}$	RESERVED		RESERVED		RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 11; CWL = 8	$t_{CK.AVG.CL11.CWL08}$	1.25	1.5	1.25	1.5	1.25	1.5	1.25	1.5	ns	1)2)

- 1) Please refer to "General Notes for Speed Bins" at beginning of this chapter.
- 2) Max. limits are exclusive. E.g. if $t_{CK.AVG.MAX}$ value is 2.5 ns, $t_{CK.AVG}$ needs to be < 2.5 ns.



5 SPD Codes

This chapter lists all hexadecimal byte values stored in the EEPROM of the products described in this data sheet. SPD stands for serial presence detect. All values with XX in the table are module specific bytes which are defined during production.

List of SPD Code Tables

- Table 16 “SPD Codes for IMSH1GU03A1F1C” on Page 21
- Table 17 “SPD Codes for IMSH1GU03A1F1C” on Page 25
- Table 18 “SPD Codes for IMSH2GU13A1F1C” on Page 28
- Table 19 “SPD Codes for IMSH2GU13A1F1C” on Page 31
- Table 20 “SPD Codes for IMSH1GE03A1F1CT” on Page 34
- Table 21 “SPD Codes for IMSH2GE13A1F1CT” on Page 38

TABLE 16

SPD Codes for IMSH1GU03A1F1C

Product Type		IMSH1GU03A1F1C-08D	IMSH1GU03A1F1C-08E	IMSH1GU03A1F1C-10F	IMSH1GU03A1F1C-10G
Organization		1 GByte ×64 1 Rank (×8)	1 GByte ×64 1 Rank (×8)	1 GByte ×64 1 Rank (×8)	1 GByte ×64 1 Rank (×8)
Label Code		PC3-6400U-5	PC3-6400U-6	PC3-8500U-7	PC3-8500U-8
JEDEC SPD Revision		Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0
Byte#	Description	HEX	HEX	HEX	HEX
0	# of SPD bytes utilized / # of bytes in SPD / CRC	92	92	92	92
1	SPD Revision	10	10	10	10
2	SDRAM technology key byte	0B	0B	0B	0B
3	DIMM module type	02	02	02	02
4	SDRAM density and banks	02	02	02	02
5	SDRAM addressing	11	11	11	11
6	Module physical attributes	00	00	00	00
7	Module organization	01	01	01	01
8	Module memory bus width	03	03	03	03
9	Fine time base (FTB) dividend and divisor	52	52	52	52
10	Medium time base (MTB) dividend	01	01	01	01



IMSH[1G/2G][U/E]x3A1F1C(T)
DDR3 Unbuffered DIMM

Product Type		IMSH1GU03A1F1C-08D	IMSH1GU03A1F1C-08E	IMSH1GU03A1F1C-10F	IMSH1GU03A1F1C-10G
Organization		1 GByte	1 GByte	1 GByte	1 GByte
		×64	×64	×64	×64
		1 Rank (×8)	1 Rank (×8)	1 Rank (×8)	1 Rank (×8)
Label Code		PC3-6400U-5	PC3-6400U-6	PC3-8500U-7	PC3-8500U-8
JEDEC SPD Revision		Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0
Byte#	Description	HEX	HEX	HEX	HEX
11	Medium time base (MTB) divisor	08	08	08	08
12	Minimum SDRAM cycle time ($t_{CK.MIN}$)	14	14	0F	0F
13	Reserved	00	00	00	00
14	CAS Latencies Supported - LSB	06	04	1C	14
15	CAS Latencies Supported - MSB	00	00	00	00
16	Minimum CAS Latency Time ($t_{CK.MIN}$)	64	78	69	78
17	Minimum Write Recovery Time ($t_{WR.MIN}$)	78	78	78	78
18	Minimum RAS# toCAS# Delay Time ($t_{RCD.MIN}$)	64	78	69	78
19	Minimum Row Active to Row Active Delay Time ($t_{RRD.MIN}$)	50	50	3C	3C
20	Minimum Row PrechargeTime ($t_{RP.MIN}$)	64	78	69	78
21	Upper Nibbles for t_{RAS} and t_{RC}	11	11	11	11
22	Minimum Active to Precharge Time ($t_{RAS.MIN}$), LSB	2C	2C	2C	2C
23	Minimum Active to Active/Refresh Time ($t_{RC.MIN}$), LSB	90	A4	95	A4
24	Minimum Refresh Recovery Time ($t_{RFC.MIN}$), LSB	70	70	70	70
25	Minimum Refresh Recovery Time ($t_{RFC.MIN}$), MSB	03	03	03	03
26	Minimum Internal Write to Read Command Delay Time ($t_{WTR.MIN}$)	3C	3C	3C	3C
27	Minimum Internal Read to Precharge Command Delay Time ($t_{RTP.MIN}$), MSB	3C	3C	3C	3C
28	Upper Nibble for t_{FAW}	01	01	01	01
29	Minimum Four Activate Window Delay Time ($t_{FAW.MIN}$)	40	40	2C	2C
30	SDRAM Output Drivers supported	02	02	02	02
31	SDRAM Refresh Options	81	81	81	81
32 - 59	Reserved	00	00	00	00
60	Module Nominal Height	10	10	10	10



IMSH[1G/2G][U/E]x3A1F1C(T)
DDR3 Unbuffered DIMM

Product Type		IMSH1GU03A1F1C-08D	IMSH1GU03A1F1C-08E	IMSH1GU03A1F1C-10F	IMSH1GU03A1F1C-10G
Organization		1 GByte	1 GByte	1 GByte	1 GByte
		×64	×64	×64	×64
		1 Rank (×8)	1 Rank (×8)	1 Rank (×8)	1 Rank (×8)
Label Code		PC3-6400U-5	PC3-6400U-6	PC3-8500U-7	PC3-8500U-8
JEDEC SPD Revision		Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0
Byte#	Description	HEX	HEX	HEX	HEX
61	Module Maximum Thickness	01	01	01	01
62	Raw Card used	00	00	00	00
63	Address Mapping from Edge Connector to DRAM	00	00	00	00
64 - 116	Reserved	00	00	00	00
117	DIMM Manufacturer's ID Code LSB	85	85	85	85
118	DIMM Manufacturer's ID Code MSB	51	51	51	51
119	Module Manufacturing Location	xx	xx	xx	xx
120 - 121	Module Manufacturing Date	xx	xx	xx	xx
122 - 125	Module Serial Number	xx	xx	xx	xx
126	Cyclical Redundancy Code LSB	9A	95	0D	6E
127	Cyclical Redundancy Code MSB	76	87	DE	2B
128	Product Type, Char 1	49	49	49	49
129	Product Type, Char 2	4D	4D	4D	4D
130	Product Type, Char 3	53	53	53	53
131	Product Type, Char 4	48	48	48	48
132	Product Type, Char 5	31	31	31	31
133	Product Type, Char 6	47	47	47	47
134	Product Type, Char 7	55	55	55	55
135	Product Type, Char 8	30	30	30	30
136	Product Type, Char 9	33	33	33	33
137	Product Type, Char 10	41	41	41	41
138	Product Type, Char 11	31	31	31	31
139	Product Type, Char 12	46	46	46	46
140	Product Type, Char 13	31	31	31	31



IMSH[1G/2G][U/E]x3A1F1C(T)
DDR3 Unbuffered DIMM

Product Type		IMSH1GU03A1F1C-08D	IMSH1GU03A1F1C-08E	IMSH1GU03A1F1C-10F	IMSH1GU03A1F1C-10G
Organization		1 GByte	1 GByte	1 GByte	1 GByte
		×64	×64	×64	×64
		1 Rank (×8)	1 Rank (×8)	1 Rank (×8)	1 Rank (×8)
Label Code		PC3-6400U-5	PC3-6400U-6	PC3-8500U-7	PC3-8500U-8
JEDEC SPD Revision		Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0
Byte#	Description	HEX	HEX	HEX	HEX
141	Product Type, Char 14	43	43	43	43
142	Product Type, Char 15	2D	2D	2D	2D
143	Product Type, Char 16	30	30	31	31
144	Product Type, Char 17	38	38	30	30
145	Product Type, Char 18	44	45	46	47
146	Module Revision Code, LSB	2x	2x	2x	2x
147	Module Revision Code, MSB	xx	xx	xx	xx
148	DRAM Manufacturer's ID Code, LSB	85	85	85	85
149	DRAM Manufacturer's ID Code, MSB	51	51	51	51
150 - 175	Manufactures's Specific Data	00	00	00	00
176 - 255	Blank for Customer Use	00	00	00	00



IMSH[1G/2G][U/E]x3A1F1C(T)
DDR3 Unbuffered DIMM

TABLE 17
SPD Codes for IMSH1GU03A1F1C

Product Type		IMSH1GU03A1F1C-13G	IMSH1GU03A1F1C-13H	IMSH1GU03A1F1C-16J
Organization		1 GByte	1 GByte	1 GByte
		×64	×64	×64
		1 Rank (×8)	1 Rank (×8)	1 Rank (×8)
Label Code		PC3-10600U-8	PC3-10600U-9	PC3-12800U-11
JEDEC SPD Revision		Rev. 1.0	Rev. 1.0	Rev. 1.0
Byte#	Description	HEX	HEX	HEX
0	# of SPD bytes utilized / # of bytes in SPD / CRC	92	92	92
1	SPD Revision	10	10	10
2	SDRAM technology key byte	0B	0B	0B
3	DIMM module type	02	02	02
4	SDRAM density and banks	02	02	02
5	SDRAM addressing	11	11	11
6	Module physical attributes	00	00	00
7	Module organization	01	01	01
8	Module memory bus width	03	03	03
9	Fine time base (FTB) dividend and divisor	52	52	52
10	Medium time base (MTB) dividend	01	01	01
11	Medium time base (MTB) divisor	08	08	08
12	Minimum SDRAM cycle time ($t_{CK.MIN}$)	0C	0C	0A
13	Reserved	00	00	00
14	CAS Latencies Supported - LSB	7E	7C	7E
15	CAS Latencies Supported - MSB	00	00	00
16	Minimum CAS Latency Time ($t_{CK.MIN}$)	60	69	64
17	Minimum Write Recovery Time ($t_{WR.MIN}$)	78	78	78
18	Minimum RAS# toCAS# Delay Time ($t_{RCD.MIN}$)	60	69	64
19	Minimum Row Active to Row Active Delay Time ($t_{RRD.MIN}$)	30	30	30
20	Minimum Row PrechargeTime ($t_{RP.MIN}$)	60	69	64
21	Upper Nibbles for t_{RAS} and t_{RC}	11	11	11
22	Minimum Active to Precharge Time ($t_{RAS.MIN}$), LSB	20	20	18



IMSH[1G/2G][U/E]x3A1F1C(T)
DDR3 Unbuffered DIMM

Product Type		IMSH1GU03A1F1C-13G	IMSH1GU03A1F1C-13H	IMSH1GU03A1F1C-16J
Organization		1 GByte	1 GByte	1 GByte
		×64	×64	×64
		1 Rank (×8)	1 Rank (×8)	1 Rank (×8)
Label Code		PC3-10600U-8	PC3-10600U-9	PC3-12800U-11
JEDEC SPD Revision		Rev. 1.0	Rev. 1.0	Rev. 1.0
Byte#	Description	HEX	HEX	HEX
23	Minimum Active to Active/Refresh Time ($t_{RC.MIN}$), LSB	80	8C	7C
24	Minimum Refresh Recovery Time ($t_{RFC.MIN}$), LSB	70	70	70
25	Minimum Refresh Recovery Time ($t_{RFC.MIN}$), MSB	03	03	03
26	Minimum Internal Write to Read Command Delay Time ($t_{WTR.MIN}$)	3C	3C	3C
27	Minimum Internal Read to Precharge Command Delay Time ($t_{RTP.MIN}$), MSB	3C	3C	3C
28	Upper Nibble for t_{FAW}	00	00	00
29	Minimum Four Activate Window Delay Time ($t_{FAW.MIN}$)	F0	F0	F0
30	SDRAM Output Drivers supported	02	02	02
31	SDRAM Refresh Options	81	81	81
32 - 59	Reserved	00	00	00
60	Module Nominal Height	10	10	10
61	Module Maximum Thickness	01	01	01
62	Raw Card used	00	00	00
63	Address Mapping from Edge Connector to DRAM	00	00	00
64 - 116	Reserved	00	00	00
117	DIMM Manufacturer's ID Code LSB	85	85	85
118	DIMM Manufacturer's ID Code MSB	51	51	51
119	Module Manufacturing Location	xx	xx	xx
120 - 121	Module Manufacturing Date	xx	xx	xx
122 - 125	Module Serial Number	xx	xx	xx
126	Cyclical Redundancy Code LSB	C9	D9	CC
127	Cyclical Redundancy Code MSB	51	CE	A8
128	Product Type, Char 1	49	49	49



IMSH[1G/2G][U/E]x3A1F1C(T)
DDR3 Unbuffered DIMM

Product Type		IMSH1GU03A1F1C-13G	IMSH1GU03A1F1C-13H	IMSH1GU03A1F1C-16J
Organization		1 GByte	1 GByte	1 GByte
		×64	×64	×64
		1 Rank (×8)	1 Rank (×8)	1 Rank (×8)
Label Code		PC3-10600U-8	PC3-10600U-9	PC3-12800U-11
JEDEC SPD Revision		Rev. 1.0	Rev. 1.0	Rev. 1.0
Byte#	Description	HEX	HEX	HEX
129	Product Type, Char 2	4D	4D	4D
130	Product Type, Char 3	53	53	53
131	Product Type, Char 4	48	48	48
132	Product Type, Char 5	31	31	31
133	Product Type, Char 6	47	47	47
134	Product Type, Char 7	55	55	55
135	Product Type, Char 8	30	30	30
136	Product Type, Char 9	33	33	33
137	Product Type, Char 10	41	41	41
138	Product Type, Char 11	31	31	31
139	Product Type, Char 12	46	46	46
140	Product Type, Char 13	31	31	31
141	Product Type, Char 14	43	43	43
142	Product Type, Char 15	2D	2D	2D
143	Product Type, Char 16	31	31	31
144	Product Type, Char 17	33	33	36
145	Product Type, Char 18	47	48	4A
146	Module Revision Code, LSB	3x	3x	0x
147	Module Revision Code, MSB	xx	xx	xx
148	DRAM Manufacturer's ID Code, LSB	85	85	85
149	DRAM Manufacturer's ID Code, MSB	51	51	51
150 - 175	Manufactures's Specific Data	00	00	00
176 - 255	Blank for Customer Use	00	00	00



TABLE 18
SPD Codes for IMSH2GU13A1F1C

Product Type		IMSH2GU13A1F1C-08D	IMSH2GU13A1F1C-08E	IMSH2GU13A1F1C-10F	IMSH2GU13A1F1C-10G
Organization		2 GByte ×64 2 Ranks (×8)	2 GByte ×64 2 Ranks (×8)	2 GByte ×64 2 Ranks (×8)	2 GByte ×64 2 Ranks (×8)
Label Code		PC3-6400U-5	PC3-6400U-6	PC3-8500U-7	PC3-8500U-8
JEDEC SPD Revision		Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0
Byte#	Description	HEX	HEX	HEX	HEX
0	# of SPD bytes utilized / # of bytes in SPD / CRC	92	92	92	92
1	SPD Revision	10	10	10	10
2	SDRAM technology key byte	0B	0B	0B	0B
3	DIMM module type	02	02	02	02
4	SDRAM density and banks	02	02	02	02
5	SDRAM addressing	11	11	11	11
6	Module physical attributes	00	00	00	00
7	Module organization	09	09	09	09
8	Module memory bus width	03	03	03	03
9	Fine time base (FTB) dividend and divisor	52	52	52	52
10	Medium time base (MTB) dividend	01	01	01	01
11	Medium time base (MTB) divisor	08	08	08	08
12	Minimum SDRAM cycle time ($t_{CK.MIN}$)	14	14	0F	0F
13	Reserved	00	00	00	00
14	CAS Latencies Supported - LSB	06	04	1C	14
15	CAS Latencies Supported - MSB	00	00	00	00
16	Minimum CAS Latency Time ($t_{CK.MIN}$)	64	78	69	78
17	Minimum Write Recovery Time ($t_{WR.MIN}$)	78	78	78	78
18	Minimum RAS# toCAS# Delay Time ($t_{RCD.MIN}$)	64	78	69	78
19	Minimum Row Active to Row Active Delay Time ($t_{RRD.MIN}$)	50	50	3C	3C
20	Minimum Row PrechargeTime ($t_{RP.MIN}$)	64	78	69	78
21	Upper Nibbles for t_{RAS} and t_{RC}	11	11	11	11



IMSH[1G/2G][U/E]x3A1F1C(T)
DDR3 Unbuffered DIMM

Product Type		IMSH2GU13A1F1C-08D	IMSH2GU13A1F1C-08E	IMSH2GU13A1F1C-10F	IMSH2GU13A1F1C-10G
Organization		2 GByte	2 GByte	2 GByte	2 GByte
		×64	×64	×64	×64
		2 Ranks (×8)	2 Ranks (×8)	2 Ranks (×8)	2 Ranks (×8)
Label Code		PC3-6400U-5	PC3-6400U-6	PC3-8500U-7	PC3-8500U-8
JEDEC SPD Revision		Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0
Byte#	Description	HEX	HEX	HEX	HEX
22	Minimum Active to Precharge Time ($t_{RAS.MIN}$), LSB	2C	2C	2C	2C
23	Minimum Active to Active/Refresh Time ($t_{RC.MIN}$), LSB	90	A4	95	A4
24	Minimum Refresh Recovery Time ($t_{RFC.MIN}$), LSB	70	70	70	70
25	Minimum Refresh Recovery Time ($t_{RFC.MIN}$), MSB	03	03	03	03
26	Minimum Internal Write to Read Command Delay Time ($t_{WTR.MIN}$)	3C	3C	3C	3C
27	Minimum Internal Read to Precharge Command Delay Time ($t_{RTP.MIN}$), MSB	3C	3C	3C	3C
28	Upper Nibble for t_{FAW}	01	01	01	01
29	Minimum Four Activate Window Delay Time ($t_{FAW.MIN}$)	40	40	2C	2C
30	SDRAM Output Drivers supported	02	02	02	02
31	SDRAM Refresh Options	81	81	81	81
32 - 59	Reserved	00	00	00	00
60	Module Nominal Height	10	10	10	10
61	Module Maximum Thickness	11	11	11	11
62	Raw Card used	01	01	01	01
63	Address Mapping from Edge Connector to DRAM	01	01	01	01
64 - 116	Reserved	00	00	00	00
117	DIMM Manufacturer's ID Code LSB	85	85	85	85
118	DIMM Manufacturer's ID Code MSB	51	51	51	51
119	Module Manufacturing Location	xx	xx	xx	xx
120 - 121	Module Manufacturing Date	xx	xx	xx	xx
122 - 125	Module Serial Number	xx	xx	xx	xx
126	Cyclical Redundancy Code LSB	E7	E8	70	13
127	Cyclical Redundancy Code MSB	BF	4E	17	E2



IMSH[1G/2G][U/E]x3A1F1C(T)
DDR3 Unbuffered DIMM

Product Type		IMSH2GU13A1F1C-08D	IMSH2GU13A1F1C-08E	IMSH2GU13A1F1C-10F	IMSH2GU13A1F1C-10G
Organization		2 GByte	2 GByte	2 GByte	2 GByte
		×64	×64	×64	×64
		2 Ranks (×8)	2 Ranks (×8)	2 Ranks (×8)	2 Ranks (×8)
Label Code		PC3-6400U-5	PC3-6400U-6	PC3-8500U-7	PC3-8500U-8
JEDEC SPD Revision		Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0
Byte#	Description	HEX	HEX	HEX	HEX
128	Product Type, Char 1	49	49	49	49
129	Product Type, Char 2	4D	4D	4D	4D
130	Product Type, Char 3	53	53	53	53
131	Product Type, Char 4	48	48	48	48
132	Product Type, Char 5	32	32	32	32
133	Product Type, Char 6	47	47	47	47
134	Product Type, Char 7	55	55	55	55
135	Product Type, Char 8	31	31	31	31
136	Product Type, Char 9	33	33	33	33
137	Product Type, Char 10	41	41	41	41
138	Product Type, Char 11	31	31	31	31
139	Product Type, Char 12	46	46	46	46
140	Product Type, Char 13	31	31	31	31
141	Product Type, Char 14	43	43	43	43
142	Product Type, Char 15	2D	2D	2D	2D
143	Product Type, Char 16	30	30	31	31
144	Product Type, Char 17	38	38	30	30
145	Product Type, Char 18	44	45	46	47
146	Module Revision Code, LSB	2x	2x	2x	2x
147	Module Revision Code, MSB	xx	xx	xx	xx
148	DRAM Manufacturer's ID Code, LSB	85	85	85	85
149	DRAM Manufacturer's ID Code, MSB	51	51	51	51
150 - 175	Manufactures's Specific Data	00	00	00	00
176 - 255	Blank for Customer Use	00	00	00	00



TABLE 19
SPD Codes for IMSH2GU13A1F1C

Product Type		IMSH2GU13A1F1C-13G	IMSH2GU13A1F1C-13H	IMSH2GU13A1F1C-16J
Organization		2 GByte ×64 2 Ranks (×8)	2 GByte ×64 2 Ranks (×8)	2 GByte ×64 2 Ranks (×8)
Label Code		PC3-10600U-8	PC3-10600U-9	PC3-12800U-11
JEDEC SPD Revision		Rev. 1.0	Rev. 1.0	Rev. 1.0
Byte#	Description	HEX	HEX	HEX
0	# of SPD bytes utilized / # of bytes in SPD / CRC	92	92	92
1	SPD Revision	10	10	10
2	SDRAM technology key byte	0B	0B	0B
3	DIMM module type	02	02	02
4	SDRAM density and banks	02	02	02
5	SDRAM addressing	11	11	11
6	Module physical attributes	00	00	00
7	Module organization	09	09	09
8	Module memory bus width	03	03	03
9	Fine time base (FTB) dividend and divisor	52	52	52
10	Medium time base (MTB) dividend	01	01	01
11	Medium time base (MTB) divisor	08	08	08
12	Minimum SDRAM cycle time ($t_{CK.MIN}$)	0C	0C	0A
13	Reserved	00	00	00
14	CAS Latencies Supported - LSB	7E	7C	7E
15	CAS Latencies Supported - MSB	00	00	00
16	Minimum CAS Latency Time ($t_{CK.MIN}$)	60	69	64
17	Minimum Write Recovery Time ($t_{WR.MIN}$)	78	78	78
18	Minimum RAS# toCAS# Delay Time ($t_{RCD.MIN}$)	60	69	64
19	Minimum Row Active to Row Active Delay Time ($t_{RRD.MIN}$)	30	30	30
20	Minimum Row PrechargeTime ($t_{RP.MIN}$)	60	69	64
21	Upper Nibbles for t_{RAS} and t_{RC}	11	11	11
22	Minimum Active to Precharge Time ($t_{RAS.MIN}$), LSB	20	20	18



IMSH[1G/2G][U/E]x3A1F1C(T)
DDR3 Unbuffered DIMM

Product Type		IMSH2GU13A1F1C-13G	IMSH2GU13A1F1C-13H	IMSH2GU13A1F1C-16J
Organization		2 GByte ×64 2 Ranks (×8)	2 GByte ×64 2 Ranks (×8)	2 GByte ×64 2 Ranks (×8)
Label Code		PC3-10600U-8	PC3-10600U-9	PC3-12800U-11
JEDEC SPD Revision		Rev. 1.0	Rev. 1.0	Rev. 1.0
Byte#	Description	HEX	HEX	HEX
23	Minimum Active to Active/Refresh Time ($t_{RC.MIN}$), LSB	80	8C	7C
24	Minimum Refresh Recovery Time ($t_{RFC.MIN}$), LSB	70	70	70
25	Minimum Refresh Recovery Time ($t_{RFC.MIN}$), MSB	03	03	03
26	Minimum Internal Write to Read Command Delay Time ($t_{WTR.MIN}$)	3C	3C	3C
27	Minimum Internal Read to Precharge Command Delay Time ($t_{RTP.MIN}$), MSB	3C	3C	3C
28	Upper Nibble for t_{FAW}	00	00	00
29	Minimum Four Activate Window Delay Time ($t_{FAW.MIN}$)	F0	F0	F0
30	SDRAM Output Drivers supported	02	02	02
31	SDRAM Refresh Options	81	81	81
32 - 59	Reserved	00	00	00
60	Module Nominal Height	10	10	10
61	Module Maximum Thickness	11	11	11
62	Raw Card used	01	01	01
63	Address Mapping from Edge Connector to DRAM	01	01	01
64 - 116	Reserved	00	00	00
117	DIMM Manufacturer's ID Code LSB	85	85	85
118	DIMM Manufacturer's ID Code MSB	51	51	51
119	Module Manufacturing Location	xx	xx	xx
120 - 121	Module Manufacturing Date	xx	xx	xx
122 - 125	Module Serial Number	xx	xx	xx
126	Cyclical Redundancy Code LSB	B4	A4	B1
127	Cyclical Redundancy Code MSB	98	07	61
128	Product Type, Char 1	49	49	49



IMSH[1G/2G][U/E]x3A1F1C(T)
DDR3 Unbuffered DIMM

Product Type		IMSH2GU13A1F1C-13G	IMSH2GU13A1F1C-13H	IMSH2GU13A1F1C-16J
Organization		2 GByte ×64 2 Ranks (×8)	2 GByte ×64 2 Ranks (×8)	2 GByte ×64 2 Ranks (×8)
Label Code		PC3-10600U-8	PC3-10600U-9	PC3-12800U-11
JEDEC SPD Revision		Rev. 1.0	Rev. 1.0	Rev. 1.0
Byte#	Description	HEX	HEX	HEX
129	Product Type, Char 2	4D	4D	4D
130	Product Type, Char 3	53	53	53
131	Product Type, Char 4	48	48	48
132	Product Type, Char 5	32	32	32
133	Product Type, Char 6	47	47	47
134	Product Type, Char 7	55	55	55
135	Product Type, Char 8	31	31	31
136	Product Type, Char 9	33	33	33
137	Product Type, Char 10	41	41	41
138	Product Type, Char 11	31	31	31
139	Product Type, Char 12	46	46	46
140	Product Type, Char 13	31	31	31
141	Product Type, Char 14	43	43	43
142	Product Type, Char 15	2D	2D	2D
143	Product Type, Char 16	31	31	31
144	Product Type, Char 17	33	33	36
145	Product Type, Char 18	47	48	4A
146	Module Revision Code, LSB	3x	3x	0x
147	Module Revision Code, MSB	xx	xx	xx
148	DRAM Manufacturer's ID Code, LSB	85	85	85
149	DRAM Manufacturer's ID Code, MSB	51	51	51
150 - 175	Manufactures's Specific Data	00	00	00
176 - 255	Blank for Customer Use	00	00	00



IMSH[1G/2G][U/E]x3A1F1C(T)
DDR3 Unbuffered DIMM

TABLE 20
SPD Codes for IMSH1GE03A1F1CT

Product Type		IMSH1GE03A1F1CT08D	IMSH1GE03A1F1CT08E	IMSH1GE03A1F1CT10F	IMSH1GE03A1F1CT10G	IMSH1GE03A1F1CT13G	IMSH1GE03A1F1CT13H
Organization		1 GByte ×72 1 Rank (×8)	1 GByte ×72 1 Rank (×8)	1 GByte ×72 1 Rank (×8)	1 GByte ×72 1 Rank (×8)	1 GByte ×72 1 Rank (×8)	1 GByte ×72 1 Rank (×8)
Label Code		PC3– 6400E– 5	PC3– 6400E– 6	PC3– 8500E– 7	PC3– 8500E– 8	PC3– 10600E –8	PC3– 10600E –9
JEDEC SPD Revision		Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0
Byte#	Description	HEX	HEX	HEX	HEX	HEX	HEX
0	# of SPD bytes utilized / # of bytes in SPD / CRC	92	92	92	92	92	92
1	SPD Revision	10	10	10	10	10	10
2	SDRAM technology key byte	0B	0B	0B	0B	0B	0B
3	DIMM module type	02	02	02	02	02	02
4	SDRAM density and banks	02	02	02	02	02	02
5	SDRAM addressing	11	11	11	11	11	11
6	Module physical attributes	00	00	00	00	00	00
7	Module organization	01	01	01	01	01	01
8	Module memory bus width	0B	0B	0B	0B	0B	0B
9	Fine time base (FTB) dividend and divisor	52	52	52	52	52	52
10	Medium time base (MTB) dividend	01	01	01	01	01	01
11	Medium time base (MTB) divisor	08	08	08	08	08	08
12	Minimum SDRAM cycle time ($t_{CK.MIN}$)	14	14	0F	0F	0C	0C
13	Reserved	00	00	00	00	00	00
14	CAS Latencies Supported - LSB	06	04	1C	14	7E	7C
15	CAS Latencies Supported - MSB	00	00	00	00	00	00
16	Minimum CAS Latency Time ($t_{CK.MIN}$)	64	78	69	78	60	69
17	Minimum Write Recovery Time ($t_{WR.MIN}$)	78	78	78	78	78	78
18	Minimum RAS# toCAS# Delay Time ($t_{RCD.MIN}$)	64	78	69	78	60	69
19	Minimum Row Active to Row Active Delay Time ($t_{RRD.MIN}$)	50	50	3C	3C	30	30
20	Minimum Row PrechargeTime ($t_{RP.MIN}$)	64	78	69	78	60	69



IMSH[1G/2G][U/E]x3A1F1C(T)
DDR3 Unbuffered DIMM

Product Type		IMSH1GE03A1F1CT08D	IMSH1GE03A1F1CT08E	IMSH1GE03A1F1CT10F	IMSH1GE03A1F1CT10G	IMSH1GE03A1F1CT13G	IMSH1GE03A1F1CT13H
Organization		1 GByte	1 GByte	1 GByte	1 GByte	1 GByte	1 GByte
		×72	×72	×72	×72	×72	×72
		1 Rank (×8)	1 Rank (×8)	1 Rank (×8)	1 Rank (×8)	1 Rank (×8)	1 Rank (×8)
Label Code		PC3–6400E–5	PC3–6400E–6	PC3–8500E–7	PC3–8500E–8	PC3–10600E–8	PC3–10600E–9
JEDEC SPD Revision		Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0
Byte#	Description	HEX	HEX	HEX	HEX	HEX	HEX
21	Upper Nibbles for t_{RAS} and t_{RC}	11	11	11	11	11	11
22	Minimum Active to Precharge Time ($t_{RAS.MIN}$), LSB	2C	2C	2C	2C	20	20
23	Minimum Active to Active/Refresh Time ($t_{RC.MIN}$), LSB	90	A4	95	A4	80	8C
24	Minimum Refresh Recovery Time ($t_{RFC.MIN}$), LSB	70	70	70	70	70	70
25	Minimum Refresh Recovery Time ($t_{RFC.MIN}$), MSB	03	03	03	03	03	03
26	Minimum Internal Write to Read Command Delay Time ($t_{WTR.MIN}$)	3C	3C	3C	3C	3C	3C
27	Minimum Internal Read to Precharge Command Delay Time ($t_{RTP.MIN}$), MSB	3C	3C	3C	3C	3C	3C
28	Upper Nibble for t_{FAW}	01	01	01	01	00	00
29	Minimum Four Activate Window Delay Time ($t_{FAW.MIN}$)	40	40	2C	2C	F0	F0
30	SDRAM Output Drivers supported	02	02	02	02	02	02
31	SDRAM Refresh Options	81	81	81	81	81	81
32 - 59	Reserved	00	00	00	00	00	00
60	Module Nominal Height	10	10	10	10	10	10
61	Module Maximum Thickness	01	01	01	01	01	01
62	Raw Card used	03	03	03	03	03	03
63	Address Mapping from Edge Connector to DRAM	00	00	00	00	00	00
64 - 116	Reserved	00	00	00	00	00	00
117	DIMM Manufacturer's ID Code LSB	85	85	85	85	85	85
118	DIMM Manufacturer's ID Code MSB	51	51	51	51	51	51
119	Module Manufacturing Location	xx	xx	xx	xx	xx	xx
120 - 121	Module Manufacturing Date	xx	xx	xx	xx	xx	xx



IMSH[1G/2G][U/E]x3A1F1C(T)
DDR3 Unbuffered DIMM

Product Type		IMSH1GE03A1F1CT08D	IMSH1GE03A1F1CT08E	IMSH1GE03A1F1CT10F	IMSH1GE03A1F1CT10G	IMSH1GE03A1F1CT13G	IMSH1GE03A1F1CT13H
Organization		1 GByte	1 GByte	1 GByte	1 GByte	1 GByte	1 GByte
		×72	×72	×72	×72	×72	×72
		1 Rank (×8)	1 Rank (×8)	1 Rank (×8)	1 Rank (×8)	1 Rank (×8)	1 Rank (×8)
Label Code		PC3–6400E–5	PC3–6400E–6	PC3–8500E–7	PC3–8500E–8	PC3–10600E–8	PC3–10600E–9
JEDEC SPD Revision		Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0
Byte#	Description	HEX	HEX	HEX	HEX	HEX	HEX
122 - 125	Module Serial Number	xx	xx	xx	xx	xx	xx
126	Cyclical Redundancy Code LSB	08	07	9F	FC	5B	4B
127	Cyclical Redundancy Code MSB	4E	BF	E6	13	69	F6
128	Product Type, Char 1	49	49	49	49	49	49
129	Product Type, Char 2	4D	4D	4D	4D	4D	4D
130	Product Type, Char 3	53	53	53	53	53	53
131	Product Type, Char 4	48	48	48	48	48	48
132	Product Type, Char 5	31	31	31	31	31	31
133	Product Type, Char 6	47	47	47	47	47	47
134	Product Type, Char 7	45	45	45	45	45	45
135	Product Type, Char 8	30	30	30	30	30	30
136	Product Type, Char 9	33	33	33	33	33	33
137	Product Type, Char 10	41	41	41	41	41	41
138	Product Type, Char 11	31	31	31	31	31	31
139	Product Type, Char 12	46	46	46	46	46	46
140	Product Type, Char 13	31	31	31	31	31	31
141	Product Type, Char 14	43	43	43	43	43	43
142	Product Type, Char 15	54	54	54	54	54	54
143	Product Type, Char 16	30	30	31	31	31	31
144	Product Type, Char 17	38	38	30	30	33	33
145	Product Type, Char 18	44	45	46	47	47	48
146	Module Revision Code, LSB	2x	2x	2x	2x	2x	2x
147	Module Revision Code, MSB	xx	xx	xx	xx	xx	xx



IMSH[1G/2G][U/E]x3A1F1C(T)
DDR3 Unbuffered DIMM

Product Type		IMSH1GE03A1F1CT08D	IMSH1GE03A1F1CT08E	IMSH1GE03A1F1CT10F	IMSH1GE03A1F1CT10G	IMSH1GE03A1F1CT13G	IMSH1GE03A1F1CT13H
Organization		1 GByte	1 GByte	1 GByte	1 GByte	1 GByte	1 GByte
		×72	×72	×72	×72	×72	×72
		1 Rank (×8)	1 Rank (×8)	1 Rank (×8)	1 Rank (×8)	1 Rank (×8)	1 Rank (×8)
Label Code		PC3–6400E–5	PC3–6400E–6	PC3–8500E–7	PC3–8500E–8	PC3–10600E–8	PC3–10600E–9
JEDEC SPD Revision		Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0
Byte#	Description	HEX	HEX	HEX	HEX	HEX	HEX
148	DRAM Manufacturer's ID Code, LSB	85	85	85	85	85	85
149	DRAM Manufacturer's ID Code, MSB	51	51	51	51	51	51
150 - 175	Manufactures's Specific Data	00	00	00	00	00	00
176 - 255	Blank for Customer Use	00	00	00	00	00	00



TABLE 21
SPD Codes for IMSH2GE13A1F1CT

Product Type		IMSH2GE13A1F1CT08D	IMSH2GE13A1F1CT08E	IMSH2GE13A1F1CT10F	IMSH2GE13A1F1CT10G	IMSH2GE13A1F1CT13G	IMSH2GE13A1F1CT13H
Organization		2 GByte ×72 2 Ranks (×8)	2 GByte ×72 2 Ranks (×8)	2 GByte ×72 2 Ranks (×8)	2 GByte ×72 2 Ranks (×8)	2 GByte ×72 2 Ranks (×8)	2 GByte ×72 2 Ranks (×8)
Label Code		PC3– 6400E– 5	PC3– 6400E– 6	PC3– 8500E– 7	PC3– 8500E– 8	PC3– 10600E –8	PC3– 10600E –9
JEDEC SPD Revision		Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0
Byte#	Description	HEX	HEX	HEX	HEX	HEX	HEX
0	# of SPD bytes utilized / # of bytes in SPD / CRC	92	92	92	92	92	92
1	SPD Revision	10	10	10	10	10	10
2	SDRAM technology key byte	0B	0B	0B	0B	0B	0B
3	DIMM module type	02	02	02	02	02	02
4	SDRAM density and banks	02	02	02	02	02	02
5	SDRAM addressing	11	11	11	11	11	11
6	Module physical attributes	00	00	00	00	00	00
7	Module organization	09	09	09	09	09	09
8	Module memory bus width	0B	0B	0B	0B	0B	0B
9	Fine time base (FTB) dividend and divisor	52	52	52	52	52	52
10	Medium time base (MTB) dividend	01	01	01	01	01	01
11	Medium time base (MTB) divisor	08	08	08	08	08	08
12	Minimum SDRAM cycle time ($t_{CK,MIN}$)	14	14	0F	0F	0C	0C
13	Reserved	00	00	00	00	00	00
14	CAS Latencies Supported - LSB	06	04	1C	14	7E	7C
15	CAS Latencies Supported - MSB	00	00	00	00	00	00
16	Minimum CAS Latency Time ($t_{CK,MIN}$)	64	78	69	78	60	69
17	Minimum Write Recovery Time ($t_{WR,MIN}$)	78	78	78	78	78	78
18	Minimum RAS# toCAS# Delay Time ($t_{RCD,MIN}$)	64	78	69	78	60	69
19	Minimum Row Active to Row Active Delay Time ($t_{RRD,MIN}$)	50	50	3C	3C	30	30



IMSH[1G/2G][U/E]x3A1F1C(T)
DDR3 Unbuffered DIMM

Product Type		IMSH2GE13A1F1CT08D	IMSH2GE13A1F1CT08E	IMSH2GE13A1F1CT10F	IMSH2GE13A1F1CT10G	IMSH2GE13A1F1CT13G	IMSH2GE13A1F1CT13H
Organization		2 GByte	2 GByte	2 GByte	2 GByte	2 GByte	2 GByte
		×72	×72	×72	×72	×72	×72
		2 Ranks (×8)	2 Ranks (×8)	2 Ranks (×8)	2 Ranks (×8)	2 Ranks (×8)	2 Ranks (×8)
Label Code		PC3–6400E–5	PC3–6400E–6	PC3–8500E–7	PC3–8500E–8	PC3–10600E–8	PC3–10600E–9
JEDEC SPD Revision		Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0
Byte#	Description	HEX	HEX	HEX	HEX	HEX	HEX
20	Minimum Row PrechargeTime ($t_{RP.MIN}$)	64	78	69	78	60	69
21	Upper Nibbles for t_{RAS} and t_{RC}	11	11	11	11	11	11
22	Minimum Active to Precharge Time ($t_{RAS.MIN}$), LSB	2C	2C	2C	2C	20	20
23	Minimum Active to Active/Refresh Time ($t_{RC.MIN}$), LSB	90	A4	95	A4	80	8C
24	Minimum Refresh Recovery Time ($t_{RFC.MIN}$), LSB	70	70	70	70	70	70
25	Minimum Refresh Recovery Time ($t_{RFC.MIN}$), MSB	03	03	03	03	03	03
26	Minimum Internal Write to Read Command Delay Time ($t_{WTR.MIN}$)	3C	3C	3C	3C	3C	3C
27	Minimum Internal Read to Precharge Command Delay Time ($t_{RTP.MIN}$), MSB	3C	3C	3C	3C	3C	3C
28	Upper Nibble for t_{FAW}	01	01	01	01	00	00
29	Minimum Four Activate Window Delay Time ($t_{FAW.MIN}$)	40	40	2C	2C	F0	F0
30	SDRAM Output Drivers supported	02	02	02	02	02	02
31	SDRAM Refresh Options	81	81	81	81	81	81
32 - 59	Reserved	00	00	00	00	00	00
60	Module Nominal Height	10	10	10	10	10	10
61	Module Maximum Thickness	11	11	11	11	11	11
62	Raw Card used	04	04	04	04	04	04
63	Address Mapping from Edge Connector to DRAM	01	01	01	01	01	01
64 - 116	Reserved	00	00	00	00	00	00
117	DIMM Manufacturer's ID Code LSB	85	85	85	85	85	85
118	DIMM Manufacturer's ID Code MSB	51	51	51	51	51	51
119	Module Manufacturing Location	xx	xx	xx	xx	xx	xx



IMSH[1G/2G][U/E]x3A1F1C(T)
DDR3 Unbuffered DIMM

Product Type		IMSH2GE13A1F1CT08D	IMSH2GE13A1F1CT08E	IMSH2GE13A1F1CT10F	IMSH2GE13A1F1CT10G	IMSH2GE13A1F1CT13G	IMSH2GE13A1F1CT13H
Organization		2 GByte	2 GByte	2 GByte	2 GByte	2 GByte	2 GByte
		×72	×72	×72	×72	×72	×72
		2 Ranks (×8)	2 Ranks (×8)	2 Ranks (×8)	2 Ranks (×8)	2 Ranks (×8)	2 Ranks (×8)
Label Code		PC3–6400E–5	PC3–6400E–6	PC3–8500E–7	PC3–8500E–8	PC3–10600E–8	PC3–10600E–9
JEDEC SPD Revision		Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0
Byte#	Description	HEX	HEX	HEX	HEX	HEX	HEX
120 - 121	Module Manufacturing Date	xx	xx	xx	xx	xx	xx
122 - 125	Module Serial Number	xx	xx	xx	xx	xx	xx
126	Cyclical Redundancy Code LSB	CB	C4	5C	3F	98	88
127	Cyclical Redundancy Code MSB	59	A8	F1	04	7E	E1
128	Product Type, Char 1	49	49	49	49	49	49
129	Product Type, Char 2	4D	4D	4D	4D	4D	4D
130	Product Type, Char 3	53	53	53	53	53	53
131	Product Type, Char 4	48	48	48	48	48	48
132	Product Type, Char 5	32	32	32	32	32	32
133	Product Type, Char 6	47	47	47	47	47	47
134	Product Type, Char 7	45	45	45	45	45	45
135	Product Type, Char 8	31	31	31	31	31	31
136	Product Type, Char 9	33	33	33	33	33	33
137	Product Type, Char 10	41	41	41	41	41	41
138	Product Type, Char 11	31	31	31	31	31	31
139	Product Type, Char 12	46	46	46	46	46	46
140	Product Type, Char 13	31	31	31	31	31	31
141	Product Type, Char 14	43	43	43	43	43	43
142	Product Type, Char 15	54	54	54	54	54	54
143	Product Type, Char 16	30	30	31	31	31	31
144	Product Type, Char 17	38	38	30	30	33	33
145	Product Type, Char 18	44	45	46	47	47	48



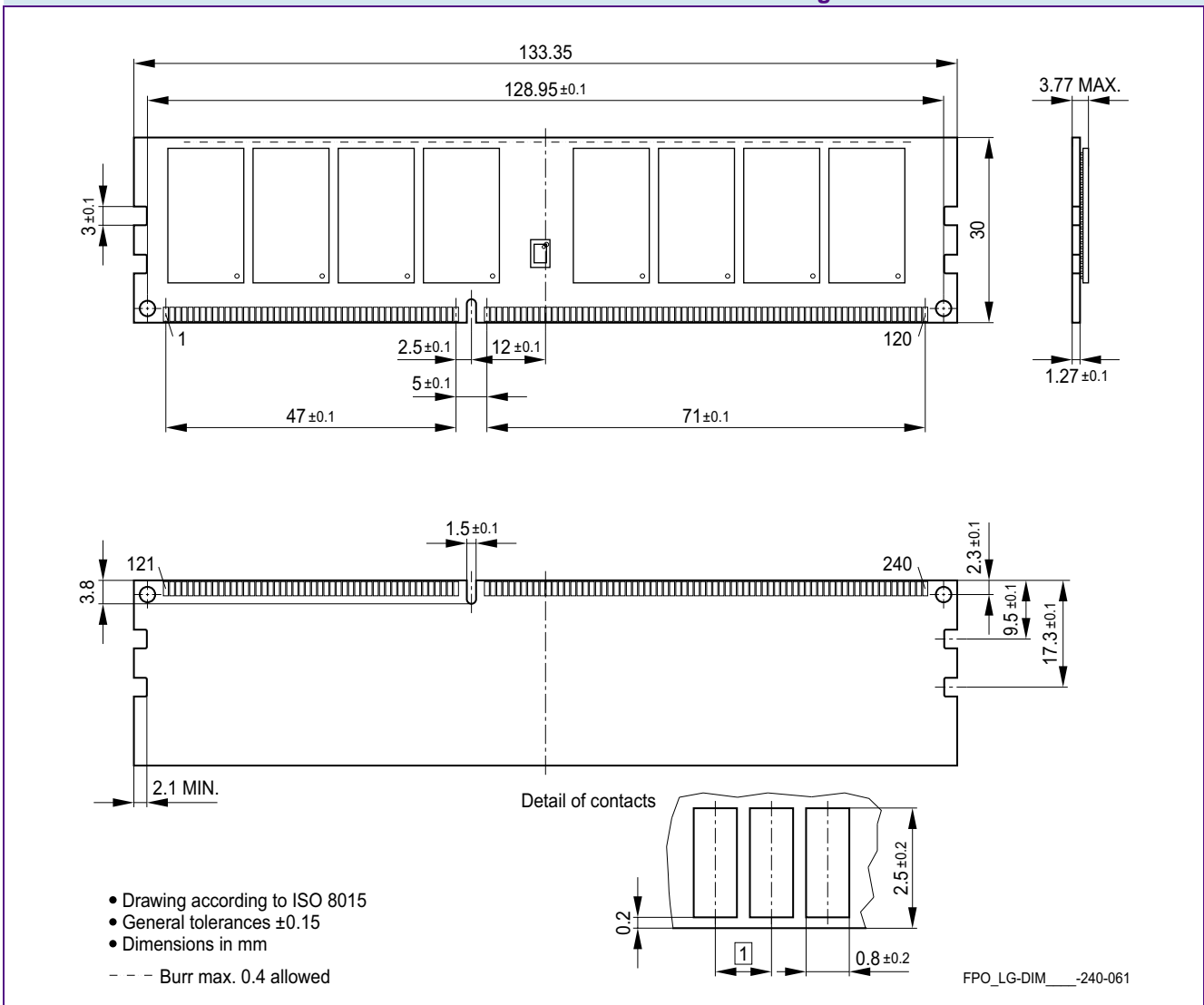
IMSH[1G/2G][U/E]x3A1F1C(T)
DDR3 Unbuffered DIMM

Product Type		IMSH2GE13A1F1CT08D	IMSH2GE13A1F1CT08E	IMSH2GE13A1F1CT10F	IMSH2GE13A1F1CT10G	IMSH2GE13A1F1CT13G	IMSH2GE13A1F1CT13H
Organization		2 GByte	2 GByte	2 GByte	2 GByte	2 GByte	2 GByte
		×72	×72	×72	×72	×72	×72
		2 Ranks (×8)	2 Ranks (×8)	2 Ranks (×8)	2 Ranks (×8)	2 Ranks (×8)	2 Ranks (×8)
Label Code		PC3–6400E–5	PC3–6400E–6	PC3–8500E–7	PC3–8500E–8	PC3–10600E–8	PC3–10600E–9
JEDEC SPD Revision		Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0
Byte#	Description	HEX	HEX	HEX	HEX	HEX	HEX
146	Module Revision Code, LSB	2x	2x	2x	2x	2x	2x
147	Module Revision Code, MSB	xx	xx	xx	xx	xx	xx
148	DRAM Manufacturer's ID Code, LSB	85	85	85	85	85	85
149	DRAM Manufacturer's ID Code, MSB	51	51	51	51	51	51
150 - 175	Manufactures's Specific Data	00	00	00	00	00	00
176 - 255	Blank for Customer Use	00	00	00	00	00	00



6 Package Outline Diagrams

FIGURE 2
Package Outline LG-DIM-240-061 R/C A

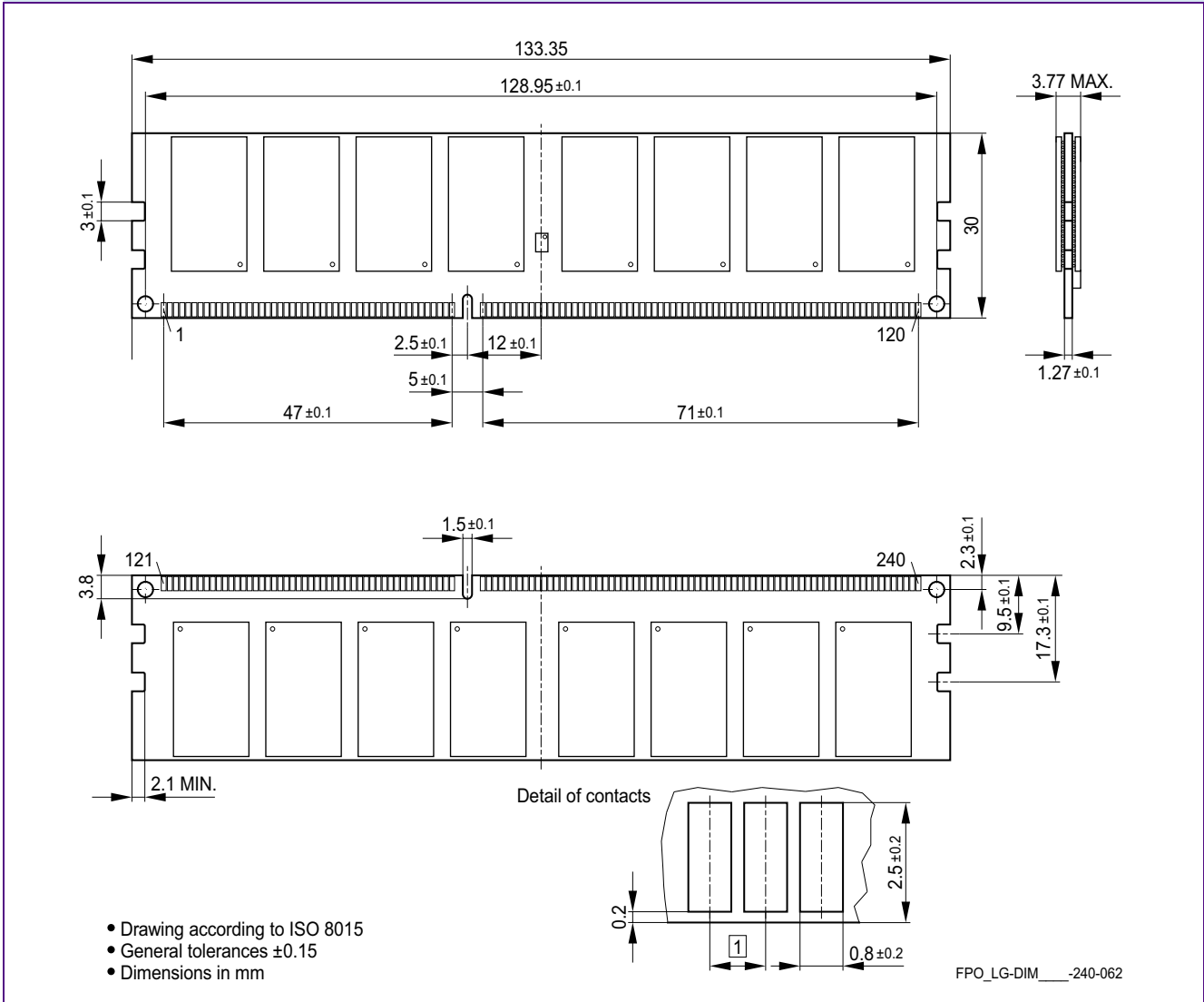


Note: SDRAM component outlines are symbolic representation of the device placement. For actual SDRAM outline details please refer to SDRAM Component Data Sheet.



IMSH[1G/2G][U/E]x3A1F1C(T)
DDR3 Unbuffered DIMM

FIGURE 3
Package Outline LG-DIM-240-062 R/C B

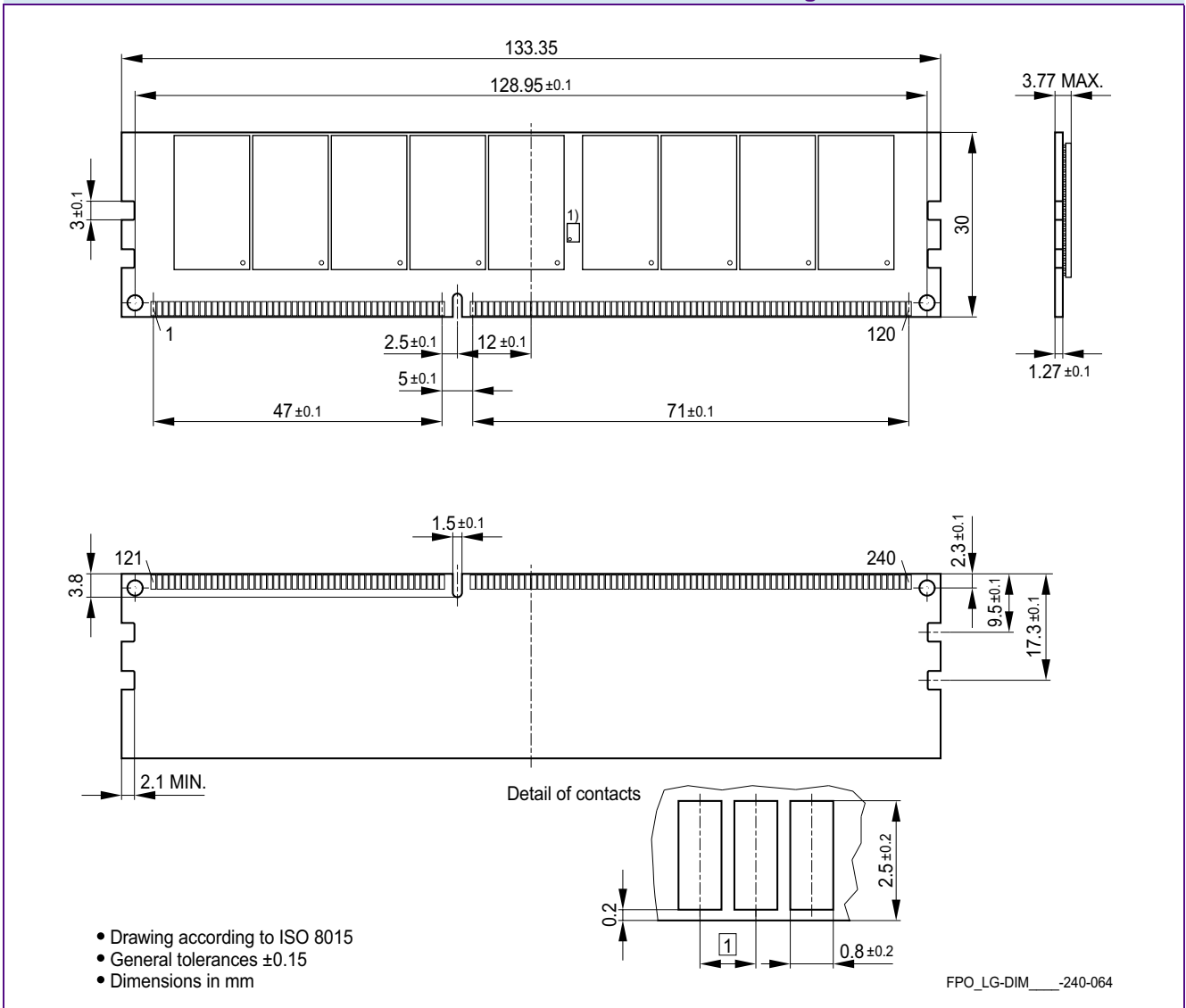


Note: SDRAM component outlines are symbolic representation of the device placement. For actual SDRAM outline details please refer to SDRAM Component Data Sheet.



IMSH[1G/2G][U/E]x3A1F1C(T)
DDR3 Unbuffered DIMM

FIGURE 4
Package Outline LG-DIM-240-064 R/C D

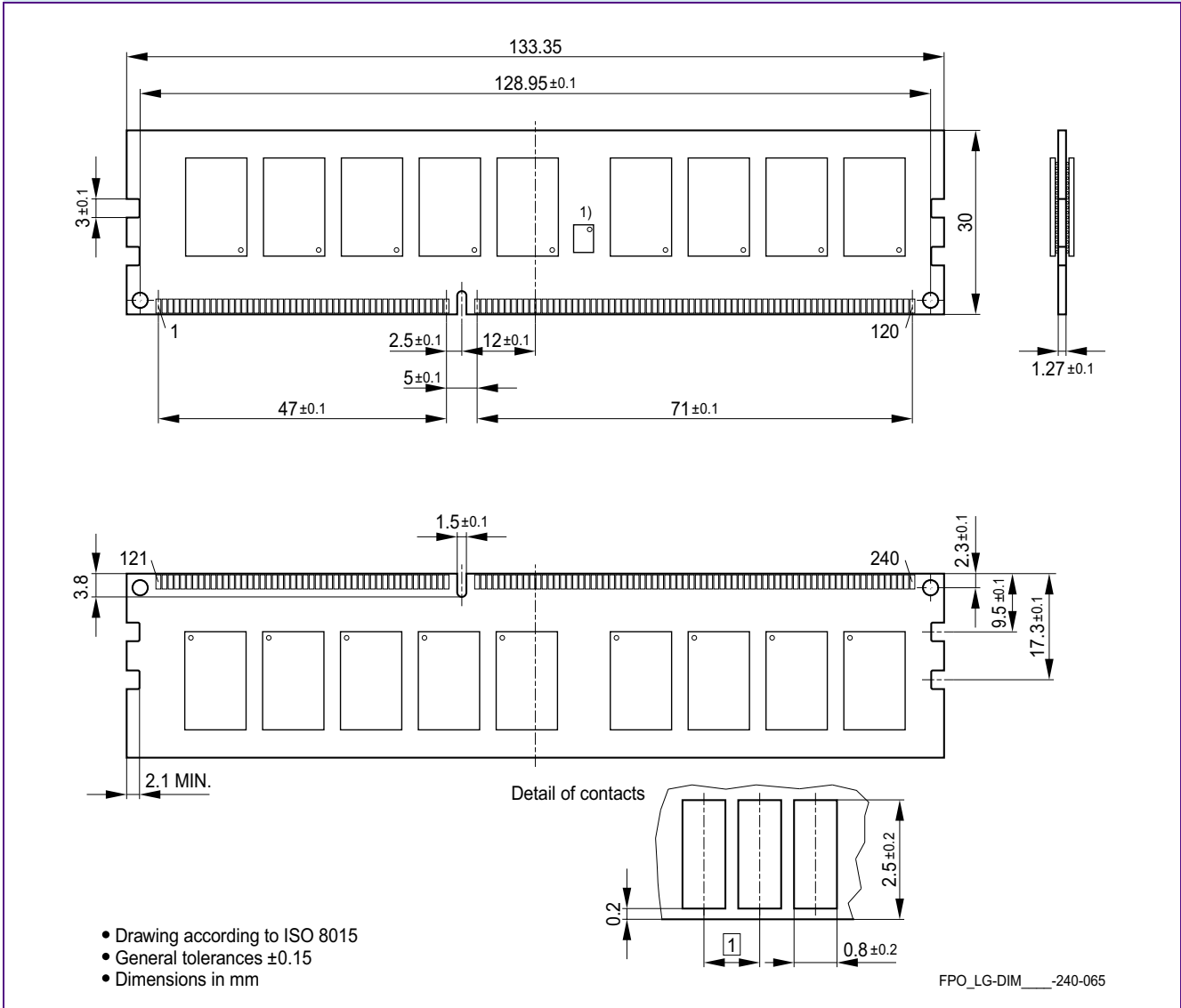


Notes

1. Option to place either combi device (SPD with integrated Thermal Sensor) or only SPD.
2. SDRAM component outlines are symbolic representation of the device placement. For actual SDRAM outline details please refer to SDRAM Component Data Sheet.



FIGURE 5
Package Outline LG-DIM-240-065 R/C E



Notes

1. Option to place either combi device (SPD with integrated Thermal Sensor) or only SPD.
2. SDRAM component outlines are symbolic representation of the device placement. For actual SDRAM outline details please refer to SDRAM Component Data Sheet.



7 Product Type Nomenclature

For reference the applicable Qimonda DDR3 DIMM module nomenclature is listed in this chapter.

TABLE 22

Example: DDR3 1GByte Unbuffered Module

Field Number	1+2	3	4	5+6	7	8	9	10+11	12+13	14	15	16+17	18
QAG Part Number	IM	S	H	1G	U	0	3	A1	F1	C	-/T	08	E

TABLE 23
DDR3 DIMM Nomenclature

Field	Description	Value	Coding
1+2	Qimonda Identifier	IM	Qimonda DIMM modules
3	Power or Application	S	Standard
		L	Low Power
4	Product Family	H	DDR3
5+6	Density	51	512 MBytes
		1G	1024 MBytes
		2G	2048 MBytes
		4G	4096 MBytes
7	Module Type / ECC Support	U	240 pin unbuffered DIMMs - Non-ECC
		E	240 pin unbuffered DIMMs - ECC
		S	204 pin Small Outline DIMMs - Non-ECC
		R	240 pin Registered DIMMs - ECC
		P	240 pin Registered DIMMs with Parity Bit - ECC
8	Number of Ranks	0	One Rank of SDRAMs
		1	Two Ranks of SDRAMs
		2	Four Ranks of SDRAMs
9	DRAM Device Number of IOs	2	x4 components (2 ²)
		3	x8 components (2 ³)
		4	x16 components (2 ⁴)
10+11	Die Revision	A1	First
12+13	Package	F1	Planar FBGA, lead- and halogen-free
		F2	Dual Die FBGA, lead- and halogen-free
14	Temperature Range	C	Commercial (0 °C - 95 °C)
15	RFU/Thermal Sensor	-/T	Reserved for future use/ Modules with thermal sensor.

IMSH[1G/2G][U/E]x3A1F1C(T)
DDR3 Unbuffered DIMM

Field	Description	Value	Coding
16+17	Band Width	08	PC3-6400, 6.4 GB/s, $t_{CK} = 2.5$ ns, $f_{CK} = 400$ MHz
		10	PC3-8500, 8.5 GB/s, $t_{CK} = 1.875$ ns, $f_{CK} = 533$ MHz
		13	PC3-10600, 10.66 GB/s, $t_{CK} = 1.5$ ns, $f_{CK} = 667$ MHz
		16	PC3-12800, 12.8 GB/s, $t_{CK} = 1.25$ ns, $f_{CK} = 800$ MHz
18	Latencies	D	CL-RCD-RP = 5-5-5
		E	CL-RCD-RP = 6-6-6
		F	CL-RCD-RP = 7-7-7
		G	CL-RCD-RP = 8-8-8
		H	CL-RCD-RP = 9-9-9
		J	CL-RCD-RP = 10-10-10



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