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BLF6G22-180RN; BLF6G22LS-180RN

Power LDMOS transistor

Rev. 01 — 20 November 2008 Product data sheet

1. Product profile

1.1 General description

180 W LDMOS power transistor for base station applications at frequencies from 2000 MHz to 2200 MHz.

Table 1. Typical performance

Typical RF performance at T_{case} = 25 °C in a class-AB production test circuit.

Mode of operation	f (MHz)	V_{DS} (V)	$P_{L(AV)}$ (W)	G_p (dB)	η_D (%)	IMD3 (dBc)	ACPR (dBc)
2-carrier W-CDMA	2110 to 2170	30	40	16.0	25	–38[1]	–42[1]

[1] Test signal: 3GPP; test model 1; 64 DPCH; PAR = 7 dB at 0.01 % probability on CCDF per carrier; carrier spacing 10 MHz.

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling.

1.2 Features

- Typical 2-carrier W-CDMA performance at frequencies of 2110 MHz and 2170 MHz, a supply voltage of 30 V and an I_{Dq} of 1400 mA:
  - Average output power = 40 W
  - Power gain = 16.0 dB
  - Efficiency = 25 %
  - IMD3 = –38 dBc
  - ACPR = –42 dBc
- Easy power control
- Integrated ESD protection
- Enhanced ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (2000 MHz to 2200 MHz)
- Internally matched for ease of use

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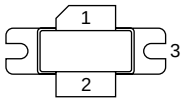
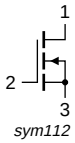
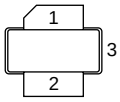
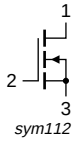
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- RF power amplifiers for GSM, GSM EDGE, W-CDMA and CDMA base stations and multi carrier applications in the 2000 MHz to 2200 MHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description		Simplified outline	Graphic symbol
BLF6G22-180RN (SOT502A)				
1	drain			
2	gate			
3	source	[1]		
BLF6G22LS-180RN (SOT502B)				
1	drain			
2	gate			
3	source	[1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF6G22-180RN	-	flanged LDMOST ceramic package; 2 mounting holes; 2 leads	SOT502A
BLF6G22LS-180RN	-	earless flanged LDMOST ceramic package; 2 leads	SOT502B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		–0.5	+13	V
I_D	drain current		-	49	A
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		-	225	°C

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5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Type	Typ	Unit
$R_{th(j-case)}$	thermal resistance from junction to case	T_{case} = 80 °C; P_L = 40 W	BLF6G22-180RN	0.50	K/W
			BLF6G22LS-180RN	0.37	K/W

6. Characteristics

Table 6. Characteristics

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.9 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 270 mA	1.4	2.0	2.4	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 28 V; I_D = 1.62 A	1.5	2.0	2.5	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	5	µA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	40	45	-	A
I_{GSS}	gate leakage current	V_{GS} = 13 V; V_{DS} = 0 V	-	-	450	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 13.5 A	-	19.5	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 9.45 A	-	0.06	-	Ω
C_{rs}	feedback capacitance	V_{GS} = 0 V; V_{DS} = 30 V; f = 1 MHz	-	3.3	-	pF

7. Application information

Table 7. Application information

Mode of operation: 2-carrier W-CDMA; PAR = 7 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 1-64 PDPCH; f_1 = 2112.5 MHz; f_2 = 2122.5 MHz; f_3 = 2157.5 MHz; f_4 = 2167.5 MHz; RF performance at V_{DS} = 30 V; I_{Dq} = 1400 mA; T_{case} = 25 °C; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_{L(AV)}$	average output power		-	40	-	W
G_p	power gain	$P_{L(AV)}$ = 40 W	15.0	16.0	-	dB
RL_{in}	input return loss	$P_{L(AV)}$ = 40 W	-	–11	–8	dB
η_D	drain efficiency	$P_{L(AV)}$ = 40 W	22	25	-	%
IMD3	third order intermodulation distortion	$P_{L(AV)}$ = 40 W	-	–38	–34.5	dBc
ACPR	adjacent channel power ratio	$P_{L(AV)}$ = 40 W	-	–42	–39	dBc

7.1 Ruggedness in class-AB operation

The BLF6G22-180RN and BLF6G22LS-180RN are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 30 V; I_{Dq} = 1400 mA; P_L = 180 W (CW); f = 2170 MHz.

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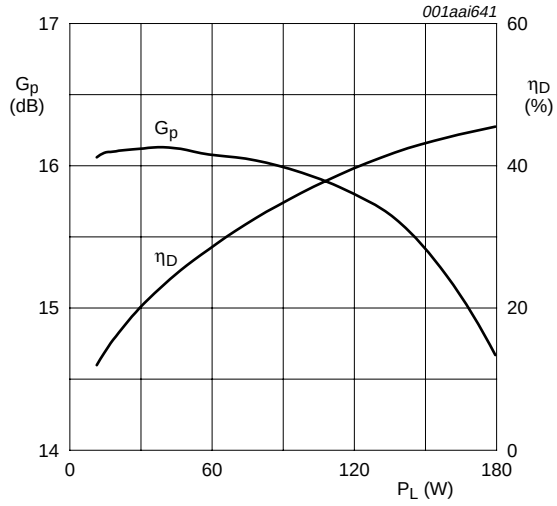
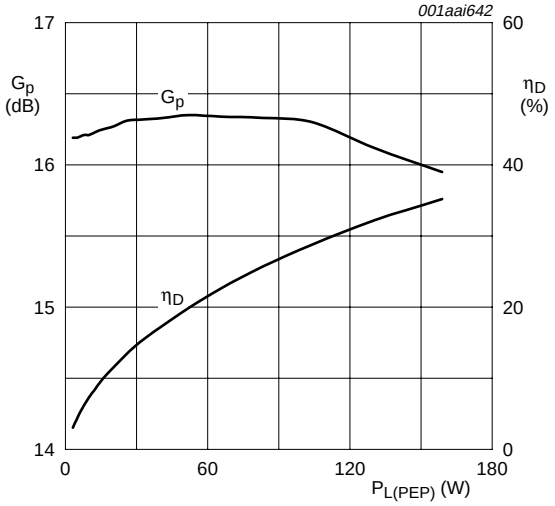
7.2 One-tone CW



V_{DS} = 30 V; I_{Dq} = 1400 mA; f = 2140 MHz.

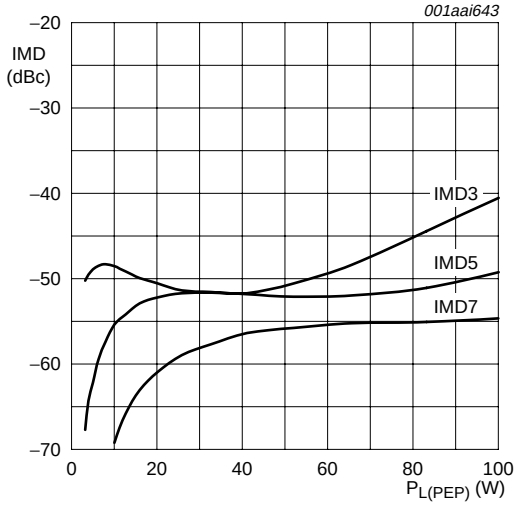
Fig 1. One-tone CW power gain and drain efficiency as function of load power; typical values

7.3 Two-tone CW



V_{DS} = 30 V; I_{Dq} = 1400 mA; f = 2140 MHz.

Fig 2. Two-tone CW power gain and drain efficiency as function of peak envelope load power; typical values



V_{DS} = 30 V; I_{Dq} = 1400 mA; f = 2140 MHz.

Fig 3. Two-tone CW intermodulation distortion as a function of peak envelope load power; typical values

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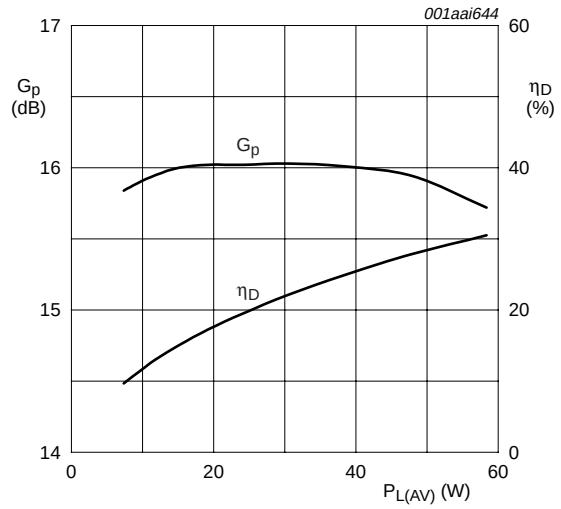
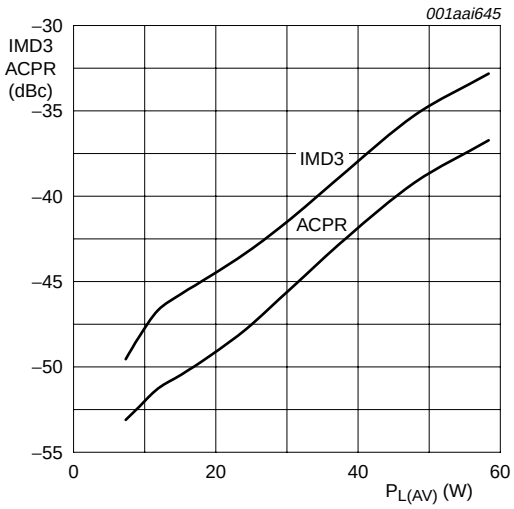
7.4 2-carrier W-CDMA



V_{DS} = 30 V; I_{Dq} = 1400 mA; f = 2140 MHz (±5 MHz); carrier spacing 10 MHz.

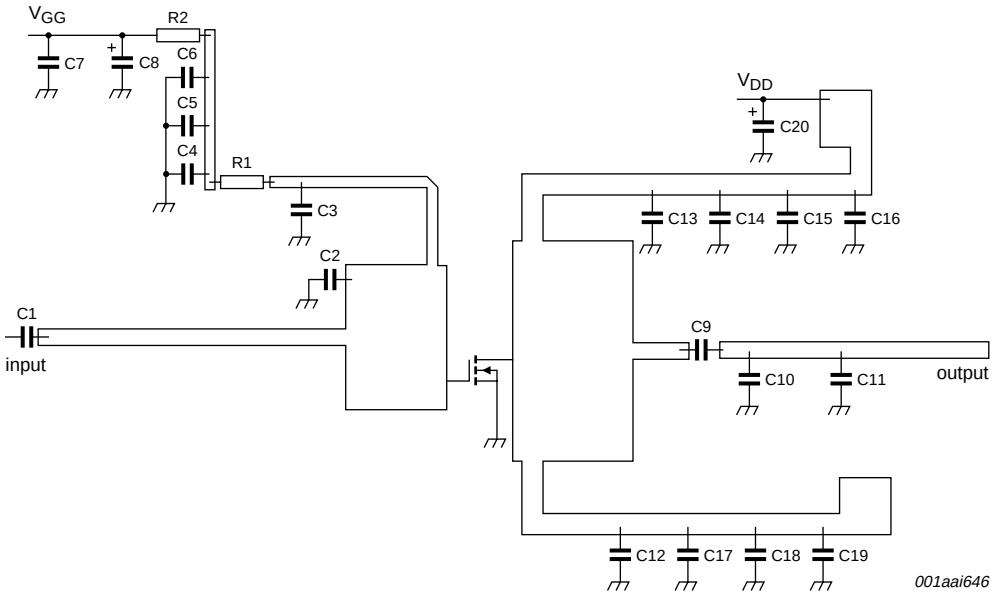
Fig 4. 2-carrier W-CDMA power gain and drain efficiency as function of average load power; typical values



V_{DS} = 30 V; I_{Dq} = 1400 mA; f = 2140 MHz (±5 MHz); carrier spacing 10 MHz.

Fig 5. 2-carrier W-CDMA adjacent channel power ratio and third order intermodulation distortion as function of average load power; typical values

8. Test information



The drawing is not to scale.

Fig 6. Test circuit for operation at 2200 MHz

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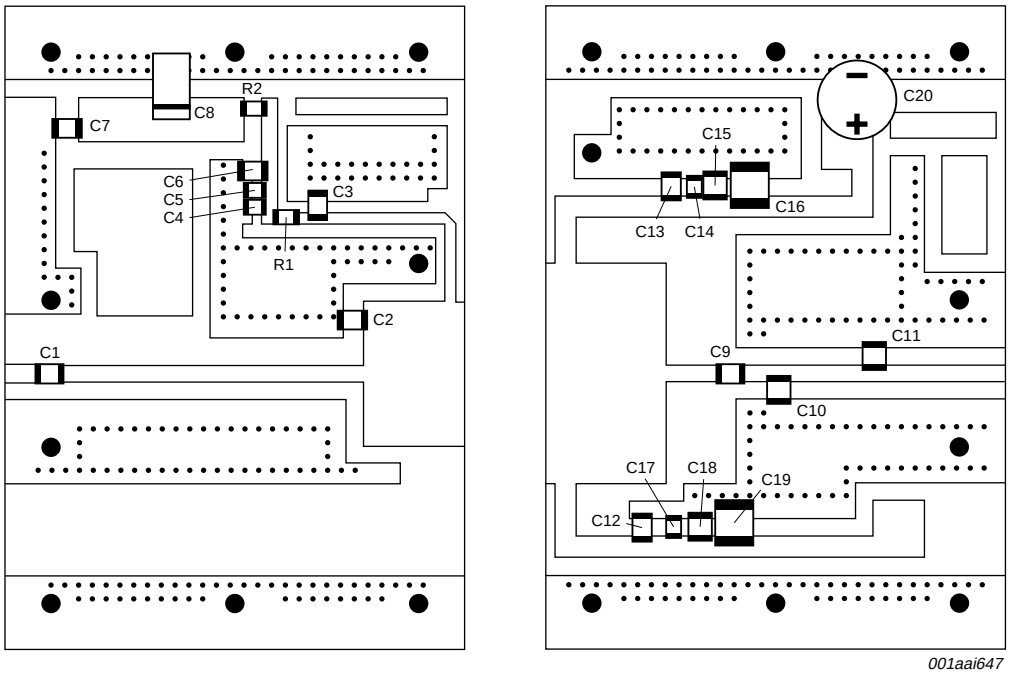

The striplines are on a double copper-clad Taconic RF35 Printed-Circuit Board (PCB) with ε_r = 3.5 and thickness = 0.76 mm.

See Table 8 for list of components.

The drawing is not to scale.

Fig 7. Component layout

Table 8. List of components (see Figure 6 and Figure 7)

The Printed-Circuit Board (PCB) used is a double copper-clad Taconic RF35 with ε_r = 3.5 and thickness = 0.76 mm.

Component	Description	Value		Remarks
C1, C3, C12, C13	multilayer ceramic chip capacitor	13 pF	[1]	ATC 100B or capacitor of same quality
C2	multilayer ceramic chip capacitor	1.4 pF	[1]	ATC 100B or capacitor of same quality
C4, C5, C14, C17	multilayer ceramic chip capacitor	220 nF		Vishay or capacitor of same quality
C6, C7	multilayer ceramic chip capacitor	100 nF		Vishay or capacitor of same quality
C8	multilayer ceramic chip capacitor	10 µF		
C9	multilayer ceramic chip capacitor	12 pF	[1]	ATC 100B or capacitor of same quality
C10	multilayer ceramic chip capacitor	1.1 pF	[1]	ATC 100B or capacitor of same quality
C11	multilayer ceramic chip capacitor	0.7 pF	[1]	ATC 100B or capacitor of same quality
C15, C18	multilayer ceramic chip capacitor	1.5 µF		
C16, C19	multilayer ceramic chip capacitor	10 µF; 50 V		TDK or capacitor of same quality
C20	electrolytic capacitor	220 µF; 63 V		
L1	ferrite SMD bead	-		Ferroxcube BDS 3/3/4.6-4S2 or equivalent
R1	SMD resistor	2.7 Ω		
R2, R3	SMD resistor	6.8 Ω		

[1] Solder vertically.

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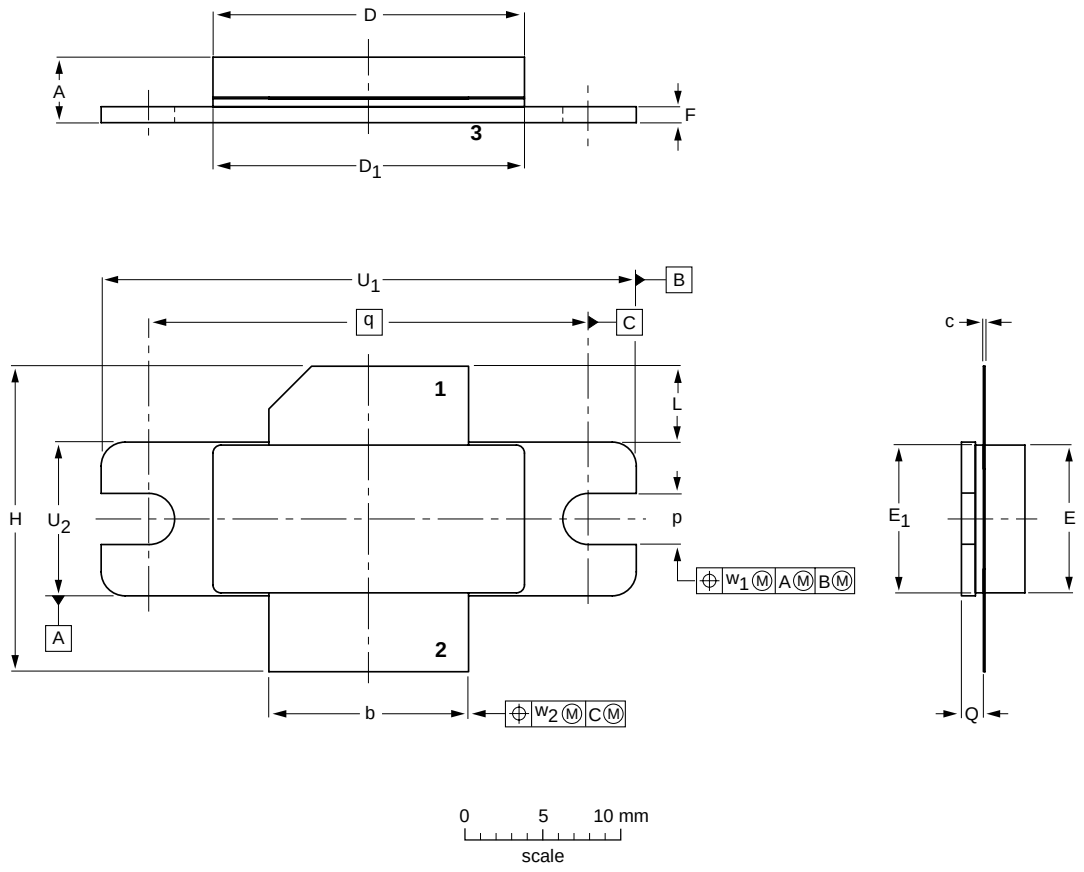
9. Package outline

Flanged LDMOST ceramic package; 2 mounting holes; 2 leads **SOT502A**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	L	p	Q	q	U_1	U_2	w_1	w_2
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	3.38 3.12	1.70 1.45	27.94	34.16 33.91	9.91 9.65	0.25	0.51
inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.133 0.123	0.067 0.057	1.100	1.345 1.335	0.390 0.380	0.01	0.02

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT502A						~~99-12-28~~ 03-01-10

Fig 8. Package outline SOT502A

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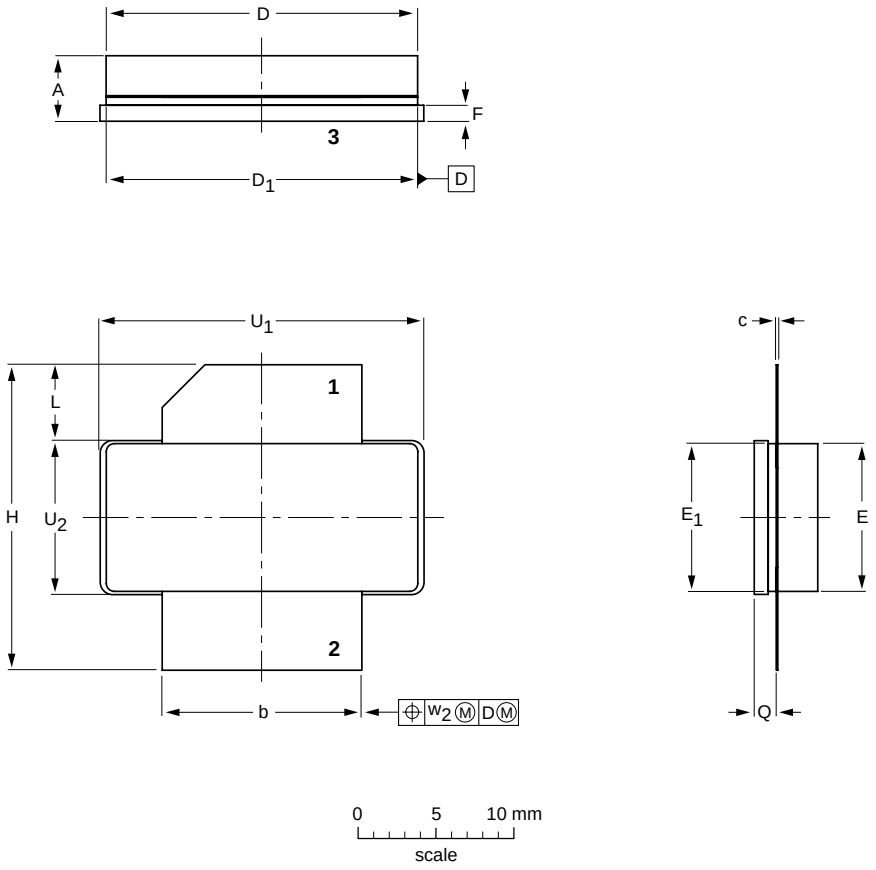
Earless flanged LDMOST ceramic package; 2 leads **SOT502B**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	L	Q	U_1	U_2	w_2
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	1.70 1.45	20.70 20.45	9.91 9.65	0.25
inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.067 0.057	0.815 0.805	0.390 0.380	0.010

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT502B						~~03-01-10~~ 07-05-09

Fig 9. Package outline SOT502B

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10. Abbreviations

Table 9. Abbreviations

Acronym	Description
3GPP	Third Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CDMA	Code Division Multiple Access
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
EDGE	Enhanced Data rates for GSM Evolution
GSM	Global System for Mobile communications
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
LDMOST	Laterally Diffused Metal-Oxide Semiconductor Transistor
PAR	Peak-to-Average power Ratio
PDPCH	transmission Power of the Dedicated Physical CHannel
RF	Radio Frequency
VSWR	Voltage Standing-Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF6G22-180RN_22LS-180RN_1	20081120	Product data sheet	-	-

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12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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