3 V/5 V, CMOS, Low Cost, Low Power, Signal Conditioning ADC

AD7714*

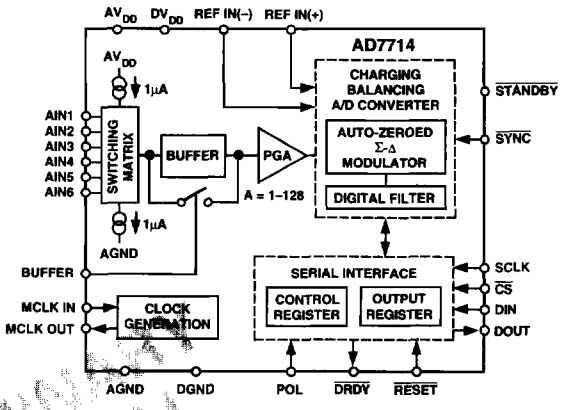
FEATURES

Charge Balancing ADC
24 Bits No Missing Codes
0.0015% Nonlinearity
Five-Channel Programmable Gain Front End
Gains from 1 to 128
Can be Configured as Three Fully Differential Inputs or Five Pseudo-Differential Inputs
Three-Wire Serial Interface
3 V (AD7714-3) or 5 V (AD7714-5) Operation
Low Power (750 μW typ) with Power-Down (50 μW typ)
Low-Pass Filter with Programmable Filter Cutoffs
Ability to Read/Write Calibration Coefficients

APPLICATIONS

Portable Industrial Instruments
Portable Weigh Scales
Loop-Powered Systems
Smart Transmitters

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7714 is a complete analog front end for low frequency measurement applications. The device accepts low level signals directly from a transducer and outputs a serial digital word. It employs a sigma-delta conversion technique to realize up to 24 bits of no missing codes performance. The input signal is applied to a proprietary programmable gain front end based around an analog modulator. The modulator output is processed by an on-chip digital filter. The first notch of this digital filter can be programmed via the on-chip control register allowing adjustment of the filter cutoff and settling time.

The part features three differential analog inputs (which can also be configured as five pseudo-differential analog inputs) as well as a differential reference input. It operates from a single supply (+3 V or +5 V). The AD7714 thus performs all signal conditioning and conversion for a system consisting of up to five channels.

The AD7714 is ideal for use in smart, microcontroller- or DSP-based systems. It features a serial interface that can be configured for three-wire operation. Gain settings, signal polarity and channel selection can be configured in software using the input serial port. The AD7714 contains self-calibration, system calibration and background calibration options and also allows the user to read and write the on-chip calibration registers.

CMOS construction ensures very low power dissipation, and the power-down mode reduces the standby power consumption to 50 μW typ. The part is available in a 24-pin, 0.3 inch-wide, plastic and hermetic dual-in-line package (DIP); a 24 lead small outline (SOIC) package and a 28-lead shrink small outline package (SSOP).

PRODUCT HIGHLIGHTS

1. The AD7714 consumes less than 500 μA ($f_{CLK\ IN}$ = 1 MHz) or 1 mA ($f_{CLK\ IN}$ = 2.5 MHz) in total supply current, making it ideal for use in loop-powered systems.
2. The programmable gain channels allow the AD7714 to accept input signals directly from a strain gage or transducer removing a considerable amount of signal conditioning.
3. The AD7714 is ideal for microcontroller or DSP processor applications with a three-wire serial interface reducing the number of interconnect lines and reducing the number of opto-couplers required in isolated systems. The part contains on-chip registers that allow control over filter cutoff, input gain, channel selection, signal polarity and calibration modes.
4. The part features excellent static performance specifications with 24-bit no missing codes, ±0.0015% accuracy and low rms noise (<300 mV). End-point errors and the effects of temperature drift are eliminated by on-chip self-calibration, which removes zero-scale and full-scale errors.

*Protected by U.S. Patent No. 5,134,401.

This is a preliminary data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD7714-5—SPECIFICATIONS (AV_{DD} = +5 V, DV_{DD} = +3 V or +5 V, REF IN(+) = +2.5 V; REF IN(–) = AGND; $f_{CLK\ IN}$ = 2.4576 MHz unless otherwise stated. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	A, S Versions[1]	Units	Conditions/Comments
STATIC PERFORMANCE			
No Missing Codes	24	Bits min	Guaranteed by Design. For Filter Notches ≤ 60 Hz
	22	Bits min	For Filter Notch = 100 Hz
	18	Bits min	For Filter Notch = 250 Hz
	15	Bits min	For Filter Notch = 500 Hz
	12	Bits min	For Filter Notch = 1 kHz
Output Noise	See Tables I & II		Depends on Filter Cutoffs and Selected Gain
Integral Nonlinearity	±0.0015	% of FSR max	Filter Notches ≤ 60 Hz
Unipolar Offset Error[2]	See Note 3		
Unipolar Offset Drift[4]	2.5/GAIN	μV/°C typ	For Gains of 1, 2, 4, 8
	0.3	μV/°C typ	For Gains of 16, 32, 64, 128
Bipolar Zero Error[2]	See Note 3		
Bipolar Zero Drift[4]	2.5/GAIN	μV/°C typ	For Gains of 1, 2, 4, 8
	0.3	μV/°C typ	For Gains of 16, 32, 64, 128
Positive Full-Scale Error[2, 5]	See Note 3		
Full Scale Drift[4, 6]	3/GAIN	μV/°C typ	For Gains of 1, 2, 4, 8
	0.35	μV/°C typ	For Gains of 16, 32, 64, 128
Gain Error[2, 7]	See Note 3		
Gain Drift[4, 8]	2	ppm of FSR/°C typ	
Bipolar Negative Full-Scale Error[2]	±0.0015	% of FSR max	Typically ±0.0004%
Bipolar Negative Full-Scale Drift[4]	4/GAIN	μV/°C typ	For Gains of 1, 2, 4, 8
	0.5	μV/°C typ	For Gains of 16, 32, 64, 128
ANALOG INPUTS/REFERENCE INPUTS			
Common-Mode Rejection (CMR)	100	dB min	At DC. See Table VI
Absolute/Common-Mode Range[9]	AGND to AV_{DD}	V min to V max	
Absolute/Common-Mode Range[9]	AGND + 50 mV to AV_{DD} – 1.5 V	V min to V max	Analog Input with BUFFER = 1
Normal-Mode 50 Hz Rejection[10]	100	dB min	For Filter Notches of 10, 25, 50 Hz, ±0.02 × f_{NOTCH}
Normal-Mode 60 Hz Rejection[10]	100	dB min	For Filter Notches of 10, 30, 60 Hz, ±0.02 × f_{NOTCH}
Common-Mode 50 Hz Rejection[10]	150	dB min	For Filter Notches of 10, 25, 50 Hz, ±0.02 × f_{NOTCH}
Common-Mode 60 Hz Rejection[10]	150	dB min	For Filter Notches of 10, 30, 60 Hz, ±0.02 × f_{NOTCH}
Input Current[10]	1	nA max	BUFFER = 1
DC Input Leakage Current[10]			BUFFER = 0
@ +25°C	10	pA max	
T_{MIN} to T_{MAX}	1	nA max	
Sampling Capacitance[10]	10	pF max	
Analog Inputs[11]			
Input Voltage Range[12]	0 to +V_{REF}/GAIN[13]	nom	Unipolar Input Range (B/U Bit of Filter High Register = 1)
	±V_{REF}/GAIN	nom	Bipolar Input Range (B/U Bit of Filter High Register = 0)
Input Sampling Rate, f_S	GAIN × $f_{CLK\ IN}$/128		For Gains of 1, 2, 4
	$f_{CLK\ IN}$/16		For Gains of 8, 16, 32, 64, 128
Reference Inputs			
REF IN(+) – REF IN(–) Voltage	+2.5	V nom	±5% for Specified Performance. Part Functions with Lower V_{REF} Voltages
Input Sampling Rate, f_S	$f_{CLK\ IN}$/128		
LOGIC INPUTS			
Input Current	±10	μA max	
All Inputs except MCLK IN			
V_{INL}, Input Low Voltage	0.8	V max	
V_{INH}, Input High Voltage	2.0	V min	
MCLK IN Only			
V_{INL}, Input Low Voltage	0.8	V max	DV_{DD} = +5 V
V_{INL}, Input Low Voltage	0.4	V max	DV_{DD} = +3 V
V_{INH}, Input High Voltage	3.5	V min	DV_{DD} = +5 V
V_{INH}, Input High Voltage	2.5	V min	DV_{DD} = +3 V
LOGIC OUTPUTS			
V_{OL}, Output Low Voltage	0.4	V max	I_{SINK} = 800 μA.
V_{OH}, Output High Voltage	4.0	V min	I_{SOURCE} = 200 μA. DV_{DD} = +5 V
V_{OH}, Output High Voltage	DV_{DD} – 0.4	V min	I_{SOURCE} = 200 μA. DV_{DD} = +3 V
Floating State Leakage Current	±10	μA max	
Floating State Output Capacitance[14]	9	pF typ	

AD7714-3—SPECIFICATIONS (AV_{DD} = +3 V, DV_{DD} = +3 V, REF IN(+) = +1.25 V; REF IN(–) = AGND; $f_{CLK\ IN}$ = 2.4576 MHz unless otherwise stated. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	A, S Versions[1]	Units	Conditions/Comments
STATIC PERFORMANCE			
No Missing Codes	24	Bits min	Guaranteed by Design. For Filter Notches ≤ 60 Hz
	22	Bits min	For Filter Notch = 100 Hz
	18	Bits min	For Filter Notch = 250 Hz
	15	Bits min	For Filter Notch = 500 Hz
	12	Bits min	For Filter Notch = 1 kHz
Output Noise	See Tables III & IV		Depends on Filter Cutoffs and Selected Gain
Integral Nonlinearity	±0.003	% of FSR max	Filter Notches ≤ 60 Hz
Unipolar Offset Error[2]	See Note 3		
Unipolar Offset Drift[4]	2.5/GAIN	μV/°C typ	For Gains of 1, 2, 4, 8
	0.3	μV/°C typ	For Gains of 16, 32, 64, 128
Bipolar Zero Error[2]	See Note 3		
Bipolar Zero Drift[4]	2.5/GAIN	μV/°C typ	For Gains of 1, 2, 4, 8
	0.3	μV/°C typ	For Gains of 16, 32, 64, 128
Positive Full-Scale Error[2, 5]	See Note 3		
Full-Scale Drift[4, 6]	3/GAIN	μV/°C typ	For Gains of 1, 2, 4, 8
	0.35	μV/°C typ	For Gains of 16, 32, 64, 128
Gain Error[2, 7]	See Note 3		
Gain Drift[4, 8]	2	ppm of FSR/°C typ	
Bipolar Negative Full-Scale Error[2]	±0.003	% of FSR max	Typically ±0.0004%
Bipolar Negative Full-Scale Drift[4]	4/GAIN	μV/°C typ	For Gains of 1, 2, 4, 8
	0.5	μV/°C typ	For Gains of 16, 32, 64, 128
ANALOG INPUTS/REFERENCE INPUTS			
Common-Mode Rejection (CMR)	94	dB min	At DC. See Table VI
Absolute Common-Mode Range[6]	AGND to AV_{DD}	V min to V max	
Absolute Common-Mode Range[6]	AGND + 50 mV to AV_{DD} – 1.5 V	V min to V max	Analog Input with BUFFER = 1
Normal-Mode 50 Hz Rejection[7]	100	dB min	For Filter Notches of 10, 25, 50 Hz, ±0.02 × f_{NOTCH}
Normal-Mode 60 Hz Rejection[7]	100	dB min	For Filter Notches of 10, 30, 60 Hz, ±0.02 × f_{NOTCH}
Common-Mode 50 Hz Rejection[7]	150	dB min	For Filter Notches of 10, 25, 50 Hz, ±0.02 × f_{NOTCH}
Common-Mode 60 Hz Rejection[7]	150	dB min	For Filter Notches of 10, 30, 60 Hz, ±0.02 × f_{NOTCH}
Input Current[7]	1	nA max	BUFFER = 1
DC Input Leakage Current[7]			BUFFER = 0
@ +25°C	10	pA max	
T_{MIN} to T_{MAX}	1	nA max	
Sampling Capacitance[7]	10	pF max	
Analog Inputs[8]			
Input Voltage Range[9]	0 to $+V_{REF}$/GAIN[13]	nom	Unipolar Input Range (B/U Bit of Filter High Register = 1)
	$\pm V_{REF}$/GAIN	nom	Bipolar Input Range (B/U Bit of Filter High Register = 0)
Input Sampling Rate, f_S	GAIN × $f_{CLK\ IN}$/128		For Gains of 1, 2, 4
	$f_{CLK\ IN}$/16		For Gains of 8, 16, 32, 64, 128
Reference Inputs			
REF IN(+) – REF IN(–) Voltage	+1.25	V nom	±5% for Specified Performance. Part Functions with Lower V_{REF} Voltages
Input Sampling Rate, f_S	$f_{CLK\ IN}$/128		
LOGIC INPUTS			
Input Current	±10	μA max	
All Inputs except MCLK IN			
V_{INL}, Input Low Voltage	0.8	V max	
V_{INH}, Input High Voltage	2.0	V min	
MCLK IN Only			
V_{INL}, Input Low Voltage	0.4	V max	
V_{INH}, Input High Voltage	2.5	V min	
LOGIC OUTPUTS			
V_{OL}, Output Low Voltage	0.2	V max	I_{SINK} = 800 μA
V_{OH}, Output High Voltage	DV_{DD} – 0.4	V min	I_{SOURCE} = 200 μA
Floating State Leakage Current	±10	μA max	
Floating State Output Capacitance[11]	9	pF typ	

AD7714–SPECIFICATIONS

(AV_{DD} = +3 V to +5 V, DV_{DD} = +3 V to +5 V, REF IN(+) = +1.25 V (AD7714-3) or +2.5 V (AD7714-5); REF IN(–) = AGND; MCLK IN = 1 MHz to 2.4576 MHz unless otherwise stated. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	A, S Versions	Units	Conditions/Comments
SYSTEM CALIBRATION			
Positive Full-Scale Calibration Limit[15]	$(1.05 \times V_{REF})/GAIN$	V max	GAIN Is the Selected PGA Gain (Between 1 and 128)
Negative Full-Scale Calibration Limit[15]	$-(1.05 \times V_{REF})/GAIN$	V max	GAIN Is the Selected PGA Gain (Between 1 and 128)
Offset Calibration Limit[16]	$-(1.05 \times V_{REF})/GAIN$	V max	GAIN Is the Selected PGA Gain (Between 1 and 128)
Input Span[16]	$0.8 \times V_{REF}/GAIN$	V min	GAIN Is the Selected PGA Gain (Between 1 and 128)
	$(2.1 \times V_{REF})/GAIN$	V max	GAIN Is the Selected PGA Gain (Between 1 and 128)
POWER REQUIREMENTS			
Power Supply Voltages			
AV_{DD} Voltage (AD7714-3)	+2.7 to +3.6	V nom	For Specified Performance
AV_{DD} Voltage (AD7714-5)	+5	V nom	±5% for Specified Performance
DV_{DD} Voltage	+2.7 to +5.25	V nom	For Specified Performance
Power Supply Currents			
AV_{DD} Current			AV_{DD} = 3 V or 5 V. BST Bit of Filter High Register = 0[17]
	0.3	mA max	Typically 0.2 mA. BUFFER = 0 V. $f_{CLK\,IN}$ = 1 MHz or 2.4576 MHz
	0.6	mA max	Typically 0.4 mA. BUFFER = +5 V. $f_{CLK\,IN}$ = 1 MHz or 2.4576 MHz
			AV_{DD} = 3 V or 5 V. BST Bit of Filter High Register = 1[17]
	0.5	mA max	Typically 0.3 mA. BUFFER = 0 V. $f_{CLK\,IN}$ = 2.4576 MHz
	1	mA max	Typically 0.8 mA. BUFFER = +5 V. $f_{CLK\,IN}$ = 2.4576 MHz
DV_{DD} Current			Digital I/Ps = 0 V or DV_{DD}
	0.2	mA max	Typically 0.15 mA. DV_{DD} = 3 V. $f_{CLK\,IN}$ = 1 MHz
	0.4	mA max	Typically 0.3 mA. DV_{DD} = 5 V. $f_{CLK\,IN}$ = 1 MHz
	0.5	mA max	Typically 0.4 mA. DV_{DD} = 3 V. $f_{CLK\,IN}$ = 2.4576 MHz
	1	mA max	Typically 0.8 mA. DV_{DD} = 5 V. $f_{CLK\,IN}$ = 2.4576 MHz
Power Supply Rejection[18] (AVDD)	See Note 19	dB typ	
Normal Mode Power Dissipation			AV_{DD} = DV_{DD} = +3 V. Digital I/Ps = 0 V or DV_{DD}. BST Bit = 0
	1.5	mW max	Typically 1 mW. BUFFER = 0 V. $f_{CLK\,IN}$ = 1 MHz
	2.4	mW max	Typically 1.6 mW. BUFFER = +5 V. $f_{CLK\,IN}$ = 1 MHz
	3	mW max	Typically 2.1 mW. BUFFER = 0 V. $f_{CLK\,IN}$ = 2.4576 MHz
	4.5	mW max	Typically 3.6 mW. BUFFER = +5 V. $f_{CLK\,IN}$ = 2.4576 MHz
Normal Mode Power Dissipation			AV_{DD} = DV_{DD} = +5 V. Digital I/Ps = 0 V or DV_{DD}. BST Bit = 0
	3.5	mW max	Typically 2.5 mW. BUFFER = 0 V. $f_{CLK\,IN}$ = 1 MHz
	5	mW max	Typically 3.5 mW. BUFFER = +5 V. $f_{CLK\,IN}$ = 1 MHz
	7.5	mW max	Typically 5.5 mW. BUFFER = 0 V. $f_{CLK\,IN}$ = 2.4576 MHz
	10	mW max	Typically 8 mW. BUFFER = +5 V. $f_{CLK\,IN}$ = 2.4576 MHz
Standby (Power-Down) Dissipation	100	μW max	Typically 50 μW

NOTES

[1]Temperature ranges are as follows: A Version: –40°C to +85°C; S Version: –55°C to +125°C.

[2]Applies after calibration at the temperature of interest.

[3]These errors will be of the order of the output noise of the part as shown in Tables I to IV.

[4]Recalibration at any temperature will remove these drift errors.

[5]Positive Full-Scale Error includes Zero-Scale Errors (Unipolar Offset Error or Bipolar Zero Error) and applies to both unipolar and bipolar input ranges.

[6]Full-Scale Drift includes Zero-Scale Drift (Unipolar Offset Drift or Bipolar Zero Drift) and applies to both unipolar and bipolar input ranges.

[7]Gain Error does not include Zero-Scale Errors. It is calculated as Full-Scale Error—Unipolar Offset Error for unipolar ranges and Full-Scale Error—Bipolar Zero Error for bipolar ranges.

[8]Gain Drift does not include Unipolar Offset Drift/Bipolar Zero Drift. It is effectively the drift of the part if zero-scale calibrations only were performed as is the case with background calibration for gains of 64 and 128.

[9]This Common-Mode voltage range is allowed provided that the input voltage on the differential inputs does not go more positive than AV_{DD} + 30 mV or go more negative than AGND – 30 mV. The common-mode mode voltage applies to those inputs which form differential pairs (see Table VI).

[10]These numbers are guaranteed by design and/or characterization.

[11]The analog inputs present a very high impedance dynamic load which varies with clock frequency and input sample rate. The maximum recommended source resistance depends on the selected gain.

[12]The analog input voltage range on the analog inputs is given here with respect to the voltage on the respective negative input of its differential or pseudo-differential pair (see Table V). The absolute voltage on the analog inputs should not go more positive than AV_{DD} + 30 mV or go more negative than AGND – 30 mV.

[13]V_{REF} = REF IN(+) – REF IN(–).

[14]Sample tested at +25°C to ensure compliance.

[15]After calibration, if the analog input exceeds positive full scale, the converter will output all 1s. If the analog input is less than negative full scale, then the device will output all 0s.

[16]These calibration and span limits apply provided the absolute voltage on the analog inputs does not exceed AV_{DD} + 30 mV or go more negative than AGND – 30 mV. The offset calibration limit applies to both the unipolar zero point and the bipolar zero point.

[17]For higher gains (≥8) at $f_{CLK\,IN}$ = 2.4576 MHz, the BST bit of the Filter High Register must be set to 1. For other conditions, it can be set to 0.

[18]Measured at dc and applies in the selected passband. PSRR at 50 Hz will exceed 120 dB with filter notches of 5, 10, 25 or 50 Hz. PSRR at 60 Hz will exceed 120 dB with filter notches of 6, 10, 30 or 60 Hz.

[19]PSRR depends on gain: Gain of 1: 70 dB typ; Gain of 2: 75 dB typ; Gain of 4: 80 dB typ; Gains of 8 to 128: 85 dB typ.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1, 2] (DV_{DD} = +3 V to +5 V, ± 5%; AV_{DD} = +3 V or +5 V, ± 5%; AGND = DGND = 0 V; f_{CLKIN} = 2.5 MHz; Input Logic 0 = 0 V, Logic 1 = DV_{DD} unless otherwise noted.)

Parameter	Limit at T_{MIN}, T_{MAX} (A, S Versions)	Units	Conditions/Comments
f_{CLKIN}[3, 4]	400	kHz min	Master Clock Frequency: Crystal Oscillator or Externally Supplied
	2.5	MHz max	For Specified Performance
$t_{CLK\ IN\ LO}$	0.4 × $t_{CLK\ IN}$	ns min	Master Clock Input Low Time. $t_{CLK\ IN}$ = 1/$f_{CLK\ IN}$
$t_{CLK\ IN\ HI}$	0.4 × $t_{CLK\ IN}$	ns min	Master Clock Input High Time
t_r[5]	50	ns max	Digital Output Rise Time. Typically 20 ns
t_f[5]	50	ns max	Digital Output Fall Time. Typically 20 ns
t_{DRDY}	500 × $t_{CLK\ IN}$	ns nom	$\overline{DRDY}$ High Time
t_1	1000	ns min	$\overline{SYNC}$ Pulse Width
t_2	1000	ns min	$\overline{RESET}$ Pulse Width
Read Operation			
t_3	0	ns min	$\overline{DRDY}$ to $\overline{CS}$ Setup Time
t_4	20	ns min	$\overline{CS}$ Falling Edge to SCLK Falling Edge (POL = 1) or SCLK Rising Edge (POL = 0) Setup Time
t_5[6]	0	ns min	SCLK Active Edge to Data Valid Delay[7]
	20	ns max	DV_{DD} = +5 V
	40	ns max	DV_{DD} = +3 V
t_6	200	ns min	SCLK High Pulse Width
t_7	200	ns min	SCLK Low Pulse Width
t_8	20	ns min	$\overline{CS}$ Rising Edge to SCLK Rising Edge (POL = 1) or SCLK Falling Edge (POL = 0) Hold Time
t_9[8]	10	ns min	Bus Relinquish Time after SCLK Rising Edge (POL = 1) or
	50	ns max	SCLK Falling Edge (POL = 0). DV_{DD} = +5 V
	100	ns max	SCLK Falling Edge (POL = 0). DV_{DD} = +3 V
t_{10}	50	ns max	SCLK Rising Edge (POL = 1) or SCLK Falling Edge (POL = 0) to $\overline{DRDY}$ High[9]
Write Operation			
t_{11}	20	ns min	$\overline{CS}$ Falling Edge to SCLK Falling Edge (POL = 1) or SCLK Rising Edge (POL = 0) Setup Time
t_{12}	30	ns min	Data Valid to SCLK Active Edge Setup Time[6]
t_{13}	20	ns min	Data Valid to SCLK Active Edge Hold Time[6]
t_{14}	200	ns min	SCLK High Pulse Width
t_{15}	200	ns min	SCLK Low Pulse Width
t_{16}	20	ns min	$\overline{CS}$ Rising Edge to SCLK Rising Edge (POL = 1) or SCLK Falling Edge (POL = 0) Hold Time

NOTES

[1]Sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of DV_{DD}) and timed from a voltage level of 1.6 V.

[2]See Figures 2 and 3.

[3]CLKIN Duty Cycle range is 45% to 55%. CLKIN must be supplied whenever the AD7714 is not in standby mode. If no clock is present in this case, the device can draw higher current than specified and possibly become uncalibrated.

[4]The AD7714 is production tested with f_{CLKIN} at 2.5 MHz (1 MHz for some I_{DD} tests). It is guaranteed by characterization to operate at 400 kHz.

[5]Specified using 10% and 90% points on waveform of interest.

[6]These numbers are measured with the load circuit of Figure 1 and defined as the time required for the output to cross the V_{OL} or V_{OH} limits.

[7]SCLK active edge is falling edge of SCLK with POL = 1; SCLK active edge is rising edge of SCLK with POL = 0.

[8]These numbers are derived from the measured time taken by the data output to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove effects of charging or discharging the 100 pF capacitor. This means that the times quoted in the timing characteristics are the true bus relinquish times of the part and as such are independent of external bus loading capacitances.

[9]$\overline{DRDY}$ returns high after the first read from the device after an output update. The same data can be read again, if required, while $\overline{DRDY}$ is high although care should be taken that subsequent reads do not occur close to the next output update.

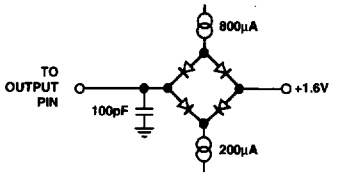


Figure 1. Load Circuit for Access Time and Bus Relinquish Time

ORDERING GUIDE

Model	AV_{DD} Supply	Temperature Range	Package Option*
AD7714AN-5	5 V	–40°C to +85°C	N-24
AD7714AR-5	5 V	–40°C to +85°C	R-24
AD7714ARS-5	5 V	–40°C to +85°C	RS-28
AD7714SQ-5	5 V	–55°C to +125°C	Q-24
AD7714AN-3	3 V	–40°C to +85°C	N-24
AD7714AR-3	3 V	–40°C to +85°C	R-24
AD7714ARS-3	3 V	–40°C to +85°C	RS-28
AD7714SQ	3 V & 5 V	–55°C to +125°C	Q-24

*N = Plastic DIP; R = SOIC; RS = SSOP; Q = Cerdip. For outline information see Package Information section.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

AV_{DD} to AGND ..... –0.3 V to +7 V
AV_{DD} to DGND ..... –0.3 V to +7 V
DV_{DD} to AGND ..... –0.3 V to +7 V
DV_{DD} to DGND ..... –0.3 V to +7 V
Analog Input Voltage to AGND ..... –0.3 V to AV_{DD} + 0.3 V
Reference Input Voltage to AGND ... –0.3 V to AV_{DD} + 0.3 V
Digital Input Voltage to DGND ..... –0.3 V to DV_{DD} + 0.3 V
Digital Output Voltage to DGND .... –0.3 V to DV_{DD} + 0.3 V
Operating Temperature Range
  Commercial (A Version) ..... –40°C to +85°C
  Extended (S Version) ..... –55°C to +125°C
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature ..... +150°C
Plastic DIP Package, Power Dissipation ..... 450 mW
  θ_{JA} Thermal Impedance ..... 105°C/W
  Lead Temperature (Soldering, 10 sec) ..... +260°C
Cerdip Package, Power Dissipation ..... 450 mW
  θ_{JA} Thermal Impedance ..... 70°C/W
  Lead Temperature (Soldering, 10 sec) ..... +300°C
SOIC Package, Power Dissipation ..... 450 mW
  θ_{JA} Thermal Impedance ..... 75°C/W
  Lead Temperature, Soldering
    Vapor Phase (60 sec) ..... +215°C
    Infrared (15 sec) ..... +220°C
Power Dissipation (Any Package) to +75°C ..... 450 mW

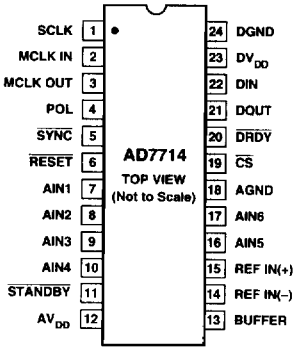
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

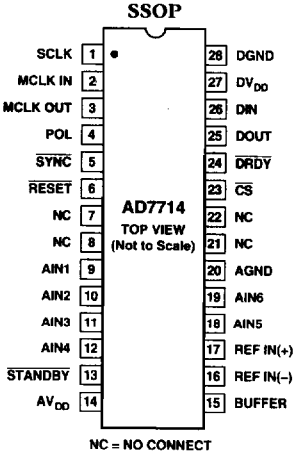
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7714 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS

DIP & SOIC



SSOP



NC = NO CONNECT

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

PIN FUNCTION DESCRIPTION

DIP/SOIC PIN NUMBERS

Pin No.	Mnemonic	Function
1	SCLK	Serial Clock. Logic Input. An external serial clock is applied to this input to access serial data from the AD7714. This serial clock can be a continuous clock with all data transmitted in a continuous train of pulses. Alternatively, it can be a noncontinuous clock with the information being transmitted to the AD7714 in smaller batches of data.
2	MCLK IN	Master Clock signal for the device. This can be provided in the form of a crystal or external clock. A crystal can be tied across the MCLK IN and MCLK OUT pins. Alternatively, the MCLK IN pin can be driven with a CMOS-compatible clock and MCLK OUT left unconnected. The clock input frequency is nominally either 2.5 MHz or 1 MHz.
3	MCLK OUT	When the master clock for the device is a crystal, the crystal is connected between MCLK IN and MCLK OUT.
4	POL	Clock Polarity. Logic Input. With this input low, the first transition of the serial clock in a data transfer operation is from a low to a high. In microcontroller applications this means that the serial clock should idle low between data transfers. With this input high, the first transition of the serial clock in a data transfer operation is from a high to a low. In microcontroller applications, this means that the serial clock should idle high between data transfers.
5	$\overline{\text{SYNC}}$	Logic Input which allows for synchronization of the digital filters and analog modulators when using a number of AD7714s. While $\overline{\text{SYNC}}$ is low, the nodes of the digital filter, the filter control logic and the calibration control logic are reset and the analog modulator is also held in its reset state.
6	$\overline{\text{RESET}}$	Logic Input. Active low input which resets the control logic, interface logic, digital filter and analog modulator of the part to power-on status.
7	AIN1	Analog Input Channel 1. Programmable-gain analog input which can be used as a pseudo-differential input when used with AIN6 or as the positive input of a differential analog input pair when used with AIN2 (see Communications Register section).
8	AIN2	Analog Input Channel 2. Programmable-gain analog input which can be used as a pseudo-differential input when used with AIN6 or as the negative input of a differential analog input pair when used with AIN1 (see Communications Register section).
9	AIN3	Analog Input Channel 3. Programmable-gain analog input which can be used as a pseudo-differential input when used with AIN6 or as the positive input of a differential analog input pair when used with AIN4 (see Communications Register section).
10	AIN4	Analog Input Channel 4. Programmable-gain analog input which can be used as a pseudo-differential input when used with AIN6 or as the negative input of a differential analog input pair when used with AIN3 (see Communications Register section).
11	$\overline{\text{STANDBY}}$	Logic Input. Taking this pin low shuts down the analog and digital circuitry, reducing power consumption to typically 50 μW.
12	AV_{DD}	Analog Positive Supply Voltage, +3 V nominal (AD7714-3) or +5 V nominal (AD7714-5).
13	BUFFER	Buffer Option Select. Logic Input. With this input low, the on-chip buffer on the analog input (after the multiplexer and before the analog modulator) is shorted out. With the buffer shorted out the current flowing in the AV_{DD} line is reduced to 300 μA ($f_{CLK\,IN}$ = 1 MHz) or 500 μA ($f_{CLK\,IN}$ = 2.5 MHz). With this input high, the on-chip buffer is in series with the analog input allowing the inputs to handle higher source impedances.
14	REF IN(–)	Reference Input. Negative input of the differential reference input to the AD7714. The REF IN(–) can lie anywhere between AV_{DD} and AGND provided REF IN(+) is greater than REF IN(–).
15	REF IN(+)	Reference Input. Positive input of the differential reference input to the AD7714. The reference input is differential with the provision that REF IN(+) must be greater than REF IN(–). REF IN(+) can lie anywhere between AV_{DD} and AGND.
16	AIN5	Analog Input Channel 5. Programmable-gain analog input which is the positive input of a differential analog input pair when used with AIN6 (see Communications Register section).
17	AIN6	Analog Input Channel 6. Reference point for AIN1 through AIN4 in pseudo-differential mode or as the negative input of a differential analog input pair when used with AIN5 (see Communications Register section).
18	AGND	Ground reference point for analog circuitry.

Pin No.	Mnemonic	Function
19	$\overline{CS}$	Chip Select. Active low Logic Input used to select the AD7714. With this input hard-wired low, the AD7714 can operate in its three-wire interface mode with SCLK, DIN and DOUT used to interface to the device. $\overline{CS}$ can be used to select the device in systems with more than one device on the serial bus or as a frame synchronization signal in communicating with the AD7714.
20	$\overline{DRDY}$	Logic output. A logic low on this output indicates that a new output word is available from the AD7714 data register. The $\overline{DRDY}$ pin will return high upon completion of a read operation of a full output word. If no data read has taken place, after an output update, the $\overline{DRDY}$ line will return high for 500 × $t_{CLK\ IN}$ cycles prior to he next output update. This gives an indication of when a read operation should not be attempted to avoid reading from the data register as it is being updated. $\overline{DRDY}$ is also used to indicate when the AD7714 has completed its on-chip calibration sequence.
21	DOUT	Serial Data Output with serial data being read from the output shift register on the part. This output shift register can contain information from the calibration registers, mode register, communications register, filter selection registers or data register depending on the register selection bits of the Communications Register.
22	DIN	Serial Data Input with serial data being written to the input shift register on the part. Data from this input shift register is transferred to the calibration registers, mode register, communications register or filter selection registers depending on the register selection bits of the Communications Register.
23	DV_{DD}	Digital Supply Voltage, +3 V or +5 V nominal.
24	DGND	Ground reference point for digital circuitry.

TERMINOLOGY*

INTEGRAL NONLINEARITY

This is the maximum deviation of any code from a straight line passing through the endpoints of the transfer function. The endpoints of the transfer function are zero-scale (not to be confused with bipolar zero), a point 0.5 LSB below the first code transition (000 . . . 000 to 000 . . . 001) and Full-Scale, a point 0.5 LSB above the last code transition (111 . . . 110 to 111 . . . 111). The error is expressed as a percentage of full scale.

POSITIVE FULL-SCALE ERROR

Positive Full-Scale Error is the deviation of the last code transition (111 . . . 110 to 111 . . . 111) from the ideal AIN(+) voltage (AIN(–) + V_{REF}/GAIN – 3/2 LSBs). It applies to both unipolar and bipolar analog input ranges.

UNIPOLAR OFFSET ERROR

Unipolar Offset Error is the deviation of the first code transition from the ideal AIN(+) voltage (AIN(–) + 0.5 LSB) when operating in the unipolar mode.

BIPOLAR ZERO ERROR

This is the deviation of the midscale transition (0111 . . . 111 to 1000 . . . 000) from the ideal AIN(+) voltage (AIN(–) – 0.5 LSB) when operating in the bipolar mode.

GAIN ERROR

This is a measure of the span error of the ADC. It includes full-scale errors but not zero-scale errors. For unipolar input ranges it is defined as (full-scale error–unipolar offset error) while for bipolar input ranges it is defined as (full-scale error–bipolar zero error).

BIPOLAR NEGATIVE FULL-SCALE ERROR

This is the deviation of the first code transition from the ideal AIN(+) voltage (AIN(–) – V_{REF}/GAIN + 0.5 LSB), when operating in the bipolar mode.

POSITIVE FULL-SCALE OVERRANGE

Positive Full-Scale Overrange is the amount of overhead available to handle input voltages on AIN(+) input greater than AIN(–) + V_{REF}/GAIN (for example, noise peaks or excess voltages due to system gain errors in system calibration routines) without introducing errors due to overloading the analog modulator or overflowing the digital filter.

NEGATIVE FULL-SCALE OVERRANGE

This is the amount of overhead available to handle voltages on AIN(+) below AIN(–) – V_{REF}/GAIN without overloading the analog modulator or overflowing the digital filter. Note that the analog input will accept negative voltage peaks even in the unipolar mode provided that AIN(+) is greater than AIN(–) and greater than AGND – 30 mV.

OFFSET CALIBRATION RANGE

In the system calibration modes, the AD7714 calibrates its offset with respect to the analog input. The Offset Calibration Range specification defines the range of voltages that the AD7714 can accept and still calibrate offset accurately.

FULL-SCALE CALIBRATION RANGE

This is the range of voltages that the AD7714 can accept in the system calibration mode and still calibrate full-scale correctly.

INPUT SPAN

In system calibration schemes, two voltages applied in sequence to the AD7714's analog input define the analog input range. The input span specification defines the minimum and maximum input voltages from zero to full-scale that the AD7714 can accept and still calibrate gain accurately.

*AIN(–) refers to the negative input of the differential input pairs or to AIN6 when referring to the pseudo-differential input configurations

AD7714-5 Output Noise

Table I shows the output rms noise and effective resolution for some typical notch and –3 dB frequencies for the AD7714-5 with $f_{CLK\ IN}$ = 2.4576 MHz while Table II gives the information for $f_{CLK\ IN}$ = 1 MHz. The numbers given are for the bipolar input ranges with a V_{REF} of +2.5 V and with BUFFER = 0. These numbers are typical and are generated at an analog input voltage of 0 V. The numbers in brackets in each table are for the effective resolution of the part (rounded to the nearest 0.5 LSB). The effective resolution of the device is defined as the ratio of the output rms noise to the input full-scale (i.e., $2 \times V_{REF}$/GAIN). It should be noted that it is not calculated using peak-to-peak output noise numbers. Peak-to-peak noise numbers can be up to 6.6 times the rms numbers while effective resolution numbers based on peak-to-peak noise can be 2.5 bits below the effective resolution based on rms noise as quoted in the tables.

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The output noise from the part comes from two sources. The first is the electrical noise in the semiconductor devices used in the implementation of the modulator (device noise). Secondly, when the analog input signal is converted into the digital domain, quantization noise is added. The device noise is at a low level and is largely independent of frequency. The quantization noise starts at an even lower level but rises rapidly with increasing frequency to become the dominant noise source. Consequently, lower filter notch settings (below 100 Hz approximately for $f_{CLK\ IN}$ = 2.4576 MHz and below 40 Hz approximately for $f_{CLK\ IN}$ = 1 MHz) tend to be device noise dominated while higher notch settings are dominated by quantization noise. Changing the filter notch and cutoff frequency in the quantization-noise dominated region results in a more dramatic improvement in noise performance than it does in the device-noise dominated region as shown in Tables I and II. Furthermore, quantization noise is added after the PGA, so effective resolution is largely independent of gain for the higher filter notch frequencies. Meanwhile, device noise is added in the PGA and, therefore, effective resolution reduces at high gains for lower notch frequencies. Additionally, in the device-noise dominated region, the output noise is largely independent of reference voltage while in the quantization-noise dominated region, the noise is proportional to the value of the reference. Noise numbers in the device noise dominated region will be higher than those in the Table I for BUFFER = 1 (at a gain of 128, 10 Hz notch rms noise will be 500 nV). It is possible to do post-filtering on the device to improve the output data rate for a given –3 dB frequency and also to further reduce the output noise.

At the lower filter notch settings (below 60 Hz for $f_{CLK\ IN}$ = 2.4576 MHz and below 25 Hz for $f_{CLK\ IN}$ = 1 MHz), the no missing codes performance of the device is at the 24-bit level. At the higher settings, more codes will be missed until at 1 kHz notch setting for $f_{CLK\ IN}$ = 2.4576 MHz (400 Hz for $f_{CLK\ IN}$ = 1 MHz), no missing codes performance is only guaranteed to the 12-bit level.

Table I. Output Noise/Effective Resolution vs. Gain and First Notch Frequency for $f_{CLK\ IN}$ = 2.4576 MHz, BUFFER = 0

Filter First Notch & O/P Data Rate	–3 dB Frequency	Typical Output RMS Noise in nV (Effective Resolution in Bits)															
		Gain of 1		Gain of 2		Gain of 4		Gain of 8		Gain of 16		Gain of 32		Gain of 64		Gain of 128	
5 Hz	1.31 Hz	1.2	(22)	0.7	(22)	0.4	(21.5)	0.3	(21)	0.3	(20)	0.3	(19)	0.3	(18)	0.3	(17)
10 Hz	2.62 Hz	1.7	(21.5)	1.0	(21.5)	0.5	(21.5)	0.36	(20.5)	0.33	(20)	0.33	(19)	0.33	(18)	0.33	(17)
25 Hz	6.55 Hz	4.9	(20)	2.2	(20)	1.2	(20)	0.60	(20)	0.36	(19.5)	0.36	(18.5)	0.36	(17.5)	0.36	(16.5)
30 Hz	7.86 Hz	6.1	(19.5)	2.4	(20)	1.2	(20)	0.84	(19.5)	0.5	(19.5)	0.4	(18.5)	0.4	(17.5)	0.4	(16.5)
50 Hz	13.1 Hz	7.5	(19.5)	3.8	(19.5)	2.0	(19.5)	1.0	(19.5)	0.6	(19)	0.5	(18.5)	0.5	(17.5)	0.45	(16.5)
60 Hz	15.72 Hz	8.5	(19)	4.1	(19)	2.1	(19)	1.1	(19)	0.6	(19)	0.5	(18.5)	0.5	(17.5)	0.45	(16.5)
100 Hz	26.2 Hz	13	(18.5)	6.4	(18.5)	3.7	(18.5)	1.8	(18.5)	1.1	(18)	0.9	(17.5)	0.65	(17)	0.65	(16.5)
250 Hz	65.5 Hz	130	(15)	75	(15)	25	(15.5)	12	(15.5)	7.5	(15.5)	4.0	(15.5)	2.7	(15)	1.7	(14.5)
500 Hz	131 Hz	600	(13)	260	(13)	140	(13)	70	(13)	35	(13)	25	(12.5)	15	(12.5)	8	(12.5)
1 kHz	262 Hz	2,850	(11)	1,430	(11)	700	(11)	290	(11)	180	(11)	120	(11)	63	(10.5)	35	(10)

Table II. Output Noise/Effective Resolution vs. Gain and First Notch Frequency for $f_{CLK\ IN}$ = 1 MHz, BUFFER = 0

Filter First Notch & O/P Data Rate	–3 dB Frequency	Typical Output RMS Noise in μV (Effective Resolution in Bits)															
		Gain of 1		Gain of 2		Gain of 4		Gain of 8		Gain of 16		Gain of 32		Gain of 64		Gain of 128	
2 Hz	0.52 Hz	1.2	(22)	0.7	(22)	0.4	(21.5)	0.3	(21)	0.3	(20)	0.3	(19)	0.3	(18)	0.3	(17)
4 Hz	1.05 Hz	1.7	(21.5)	1.0	(21.5)	0.5	(21.5)	0.36	(20.5)	0.33	(20)	0.33	(19)	0.33	(18)	0.33	(17)
10 Hz	2.62 Hz	4.9	(20)	2.2	(20)	1.2	(20)	0.60	(20)	0.36	(19.5)	0.36	(18.5)	0.36	(17.5)	0.36	(16.5)
25 Hz	6.55 Hz	8.5	(19)	4.1	(19)	2.1	(19)	1.1	(19)	0.6	(19)	0.5	(18.5)	0.5	(17.5)	0.45	(16.5)
30 Hz	7.86 Hz	10.2	(19)	4.9	(19)	2.6	(19)	1.3	(19)	0.8	(18.5)	0.65	(18)	0.65	(17)	0.5	(16)
50 Hz	13.1 Hz	22.5	(18)	11.2	(18)	5.6	(18)	2.7	(18)	1.7	(17.5)	1.2	(17)	0.85	(16.5)	0.75	(15.5)
60 Hz	15.72 Hz	31	(17.5)	16	(17.5)	7.6	(17.5)	3.7	(17.5)	2.3	(17)	1.5	(16.5)	1.0	(16)	0.85	(15.5)
100 Hz	26.2 Hz	130	(15)	75	(15)	25	(15.5)	12	(15.5)	7.5	(15.5)	4.0	(15.5)	2.7	(15)	1.7	(14.5)
200 Hz	52.4 Hz	600	(13)	260	(13)	140	(13)	70	(13)	35	(13)	25	(12.5)	15	(12.5)	8	(12.5)
400 Hz	104.8 Hz	2,850	(11)	1,430	(11)	700	(11)	290	(11)	180	(11)	120	(11)	63	(10.5)	35	(10)

AD7714-3 Output Noise

Table III shows the output rms noise and effective resolution for some typical notch and –3 dB frequencies for the AD7714-3 with $f_{CLK\ IN}$ = 2.4576 MHz while Table IV gives the information for $f_{CLK\ IN}$ = 1 MHz. The numbers given are for the bipolar input ranges with a V_{REF} of +1.25 V and BUFFER = 0. These numbers are typical and are generated at an analog input voltage of 0 V. The numbers in brackets in each table are for the effective resolution of the part (rounded to the nearest 0.5 LSB). The effective resolution of the device is defined as the ratio of the output rms noise to the input full-scale (i.e., $2 \times V_{REF}$/GAIN). It should be noted that it is not calculated using peak-to-peak output noise numbers. Peak-to-peak noise numbers can be up to 6.6 times the rms numbers while effective resolution numbers based on peak-to-peak noise can be 2.5 bits below the effective resolution based on rms noise as quoted in the tables.

The output noise from the part comes from two sources. The first is the electrical noise in the semiconductor devices used in the implementation of the modulator (device noise). Secondly, when the analog input signal is converted into the digital domain, quantization noise is added. The device noise is at a low level and is largely independent of frequency. The quantization noise starts at an even lower level but rises rapidly with increasing frequency to become the dominant noise source. Consequently, lower filter notch settings (below 100 Hz approximately for $f_{CLK\ IN}$ = 2.4576 MHz and below 40 Hz approximately for $f_{CLK\ IN}$ = 1 MHz) tend to be device noise dominated while higher notch settings are dominated by quantization noise. Changing the filter notch and cutoff frequency in the quantization noise dominated region results in a more dramatic improvement in noise performance than it does in the device-noise dominated region as shown in Tables III and IV. Furthermore, quantization noise is added after the PGA, so effective resolution is largely independent of gain for the higher filter notch frequencies. Meanwhile, device noise is added in the PGA and, therefore, effective resolution suffers a little at high gains for lower notch frequencies. Additionally, in the device-noise dominated region, the output noise is largely independent of reference voltage while in the quantization-noise dominated region, the noise is proportional to the value of the reference. Noise numbers in the device noise dominated region will be higher than those in the Table III for BUFFER = 1 (at a gain of 128, 10 Hz notch rms noise will be 500 nV). It is possible to do post-filtering on the device to improve the output data rate for a given –3 dB frequency and also to further reduce the output noise (see Digital Filtering section).

At the lower filter notch settings (below 60 Hz for $f_{CLK\ IN}$ = 2.4576 MHz and below 25 Hz for $f_{CLK\ IN}$ = 1 MHz), the no missing codes performance of the device is at the 24-bit level. At the higher settings, more codes will be missed until at 1 kHz notch setting for $f_{CLK\ IN}$ = 2.4576 MHz (400 Hz for $f_{CLK\ IN}$ = 1 MHz), no missing codes performance is only guaranteed to the 12-bit level.

Table III. Output Noise/Effective Resolution vs. Gain and First Notch Frequency for $f_{CLK\ IN}$ = 2.4576 MHz, BUFFER = 0

Filter First Notch & O/P Data Rate	–3 dB Frequency	Typical Output RMS Noise in μV (Effective Resolution in Bits)															
		Gain of 1		Gain of 2		Gain of 4		Gain of 8		Gain of 16		Gain of 32		Gain of 64		Gain of 128	
5 Hz	1.31 Hz	1.2	(21)	0.7	(21)	0.4	(20.5)	0.3	(20)	0.3	(19)	0.3	(18)	0.3	(17)	0.3	(16)
10 Hz	2.62 Hz	1.7	(20.5)	1.0	(20.5)	0.5	(20.5)	0.36	(19.5)	0.33	(19)	0.33	(18)	0.33	(17)	0.33	(16)
25 Hz	6.55 Hz	4.9	(19)	2.2	(19)	1.2	(19)	0.60	(19)	0.36	(18.5)	0.36	(17.5)	0.36	(16.5)	0.36	(15.5)
30 Hz	7.86 Hz	5.6	(19)	2.4	(19)	1.2	(19)	0.84	(18.5)	0.5	(18.5)	0.4	(17.5)	0.4	(16.5)	0.4	(15.5)
50 Hz	13.1 Hz	7.5	(18.5)	3.8	(18.5)	2.0	(18.5)	1.0	(18.5)	0.6	(18)	0.5	(17.5)	0.5	(16.5)	0.45	(15.5)
60 Hz	15.72 Hz	8.5	(18)	4.1	(18)	2.1	(18)	1.1	(18)	0.6	(18)	0.5	(17.5)	0.5	(16.5)	0.45	(15.5)
100 Hz	26.2 Hz	13	(17.5)	6.4	(17.5)	2.9	(17.5)	1.5	(17.5)	1.1	(17)	0.7	(17)	0.65	(16)	0.65	(15)
250 Hz	65.5 Hz	53	(15.5)	28	(15.5)	12	(15.5)	8.6	(15)	3.9	(15)	3.7	(14)	1.9	(14)	1.4	(14)
500 Hz	131 Hz	240	(13.5)	150	(13)	80	(13)	35	(13)	22	(13)	14	(12.5)	8.7	(12)	8	(11.5)
1 kHz	262 Hz	1400	(11)	610	(11)	370	(10.5)	230	(10.5)	125	(10.5)	70	(10)	40	(10)	22	(10)

Table IV. Output Noise/Effective Resolution vs. Gain and First Notch Frequency for $f_{CLK\ IN}$ = 1 MHz, BUFFER = 0

Filter First Notch & O/P Data Rate	–3 dB Frequency	Typical Output RMS Noise in μV (Effective Resolution in Bits)															
		Gain of 1		Gain of 2		Gain of 4		Gain of 8		Gain of 16		Gain of 32		Gain of 64		Gain of 128	
2 Hz	0.52 Hz	1.2	(21)	0.7	(21)	0.4	(20.5)	0.3	(20)	0.3	(19)	0.3	(18)	0.3	(17)	0.3	(16)
4 Hz	1.05 Hz	1.7	(20.5)	1.0	(20.5)	0.5	(20.5)	0.36	(19.5)	0.33	(19)	0.33	(18)	0.33	(17)	0.33	(16)
10 Hz	2.62 Hz	4.9	(19)	2.2	(19)	1.2	(19)	0.60	(19)	0.36	(18.5)	0.36	(17.5)	0.36	(16.5)	0.36	(15.5)
25 Hz	6.55 Hz	7.8	(18.5)	4.1	(18)	2.1	(18)	1.1	(18)	0.6	(18)	0.5	(17.5)	0.5	(16.5)	0.45	(15.5)
30 Hz	7.86 Hz	10.2	(18)	4.9	(18)	2.1	(18)	1.1	(18)	0.8	(17.5)	0.65	(17)	0.65	(16)	0.5	(15)
50 Hz	13.1 Hz	22.5	(17)	11.2	(17)	4.4	(17)	2.3	(17)	1.7	(16.5)	1.2	(16)	0.85	(15.5)	0.75	(14.5)
60 Hz	15.72 Hz	31	(16.5)	16	(16.5)	6.0	(16.5)	3.2	(16.5)	2.3	(16)	1.5	(15.5)	1.0	(15)	0.85	(14.5)
100 Hz	26.2 Hz	53	(15.5)	28	(15.5)	12	(15.5)	8.6	(15)	3.9	(15)	3.7	(14)	1.9	(14)	1.4	(14)
200 Hz	52.4 Hz	240	(13.5)	150	(13)	80	(13)	35	(13)	22	(13)	14	(12.5)	8.7	(12)	8	(11.5)
400 Hz	104.8 Hz	1400	(11)	610	(11)	370	(10.5)	230	(10.5)	125	(10.5)	70	(10)	40	(10)	22	(10)

On-Chip Registers

The AD7714 contains eight on-chip registers which can be accessed via the serial port of the part. The first of these is a Communications Register which controls the channel selection, decides whether the next operation is a read or write operation and also decides which register the next read or write operation accesses. The $\overline{DRDY}$ status is also available by reading from the Communications Register. The second register is a Mode Register which determines calibration mode and gain setting. The third register is labelled the Filter High Register and this determines the word length, bipolar/unipolar operation and contains the upper 4 bits of the filter selection word. The fourth register is labelled the Filter Low Register and contains the lower 8 bits of the filter selection word. The fifth register is a Test Register which is accessed when testing the device. The sixth register is the Data Register from which the output data from the part is accessed. The final two registers are calibration registers; one is the Calibration Zero-Scale Register and the other is the Calibration Full-Scale Register. The registers are discussed in more detail in the following sections.

Communications Register (RS2–RS0 = 0, 0, 0)

The Communications Register is an eight bit register from which data can either be read or to which data can be written. On power-up or after a $\overline{RESET}$, the AD7714 is waiting for a write operation to the Communications Register. This is the default state of the interface, and in situations where the interface sequence is lost, if enough writes to the device (at least four bytes) take place with DIN high, the AD7714 returns to its default state. Table V outlines the bit designations for the Communications Register.

Table V. Communications Register

0/$\overline{DRDY}$	RS2	RS1	RS0	R/$\overline{W}$	CH2	CH1	CH0

0/$\overline{DRDY}$

For a read operation, this bit provides the status of the $\overline{DRDY}$ flag from the part. The status of this bit is the same as the $\overline{DRDY}$ output pin. For a write operation, a 0 must be written to this bit so that the write operation will be recognized by the register. If a 1 is written to this bit, the part will not clock on to subsequent bits in the register.

RS2–RS0

Register Selection Bits. RS2 is the MSB of the three selection bits. The three bits select to which one of eight on-chip registers the next read or write operation takes place as follows:

RS2	RS1	RS0	Register	Register Size
0	0	0	Communications Register	8 Bits
0	0	1	Mode Register	8 Bits
0	1	0	Filter High Register	8 Bits
0	1	1	Filter Low Register	8 Bits
1	0	0	Test Register	8 Bits
1	0	1	Data Register	16 Bits or 24 Bits
1	1	0	Calibration Zero-Scale Register	24 Bits
1	1	1	Calibration Full-Scale Register	24 Bits

R/$\overline{W}$

Read/Write Select. This bit selects whether the next operation is a read or write operation to the selected register. A 0 indicates a write cycle for the next operation to the appropriate register, while a 1 indicates a read operation from the appropriate register.

CH2–CH0

Channel Select. These three bits select a channel for either conversion or for access to calibration coefficients as outlined in Table VI. There are three pairs of calibration registers on the part with some of the input channel combinations sharing calibration registers. With CH2, CH1 and CH0 at a logic 1, the part internally looks at shorted AIN6 inputs. This can be used as a test method to evaluate the noise performance of the part. The power-on or RESET status of these bits is 1, 0, 0 selecting the differential pair AIN1 and AIN2.

Table VI. Channel Selection

CH2	CH1	CH0	AIN(+)	AIN(–)	Type	Calibration Register Pair
0	0	0	AIN1	AIN6	Pseudo Differential	Register Pair 0
0	0	1	AIN2	AIN6	Pseudo Differential	Register Pair 1
0	1	0	AIN3	AIN6	Pseudo Differential	Register Pair 2
0	1	1	AIN4	AIN6	Pseudo Differential	Register Pair 2
1	0	0	AIN1	AIN2	Fully Differential	Register Pair 0
1	0	1	AIN3	AIN4	Fully Differential	Register Pair 1
1	1	0	AIN5	AIN6	Fully Differential	Register Pair 2
1	1	1	AIN6	AIN6	Test Mode	Register Pair 2

Mode Register (RS2-RS0 = 0, 0, 1); Power On/Reset Status: 00 Hex

The Mode Register is an eight bit register from which data can either be read or to which data can be written. Table VII outlines the bit designations for the Mode Register.

Table VII. Mode Register

MD2	MD1	MD0	G2	G1	G0	BO	FSYNC

MD2	MD1	MD0	Operating Mode
0	0	0	Normal Mode; this is the normal mode of operation of the device whereby the device is performing normal conversions. This is the default condition of these bits after Power-On or RESET.
0	0	1	Self-Calibration; this activates self-calibration on the channel selected by CH2, CH1 and CH0 of the Communications Register. This is a one step calibration sequence and when complete the part returns to Normal Mode. The $\overline{DRDY}$ output or bit indicates when this self-calibration is complete and when a new valid word is available in the data register. For this calibration type, the zero-scale calibration is done internally on shorted (zeroed) inputs and the full-scale calibration is done internally on V_{REF}.
0	1	0	Zero-Scale System Calibration; this activates zero-scale system calibration on the channel selected by CH2, CH1 and CH0 of the Communications Register. Calibration is performed on the analog input voltage provided at the analog input during this calibration sequence. The $\overline{DRDY}$ output or bit indicates when this zero-scale calibration is complete and the part returns to Normal Mode.
0	1	1	Full-Scale System Calibration; this activates full-scale system calibration on the selected input channel. Calibration is performed on the analog input voltage provided at the analog input during this calibration sequence. Once again, $\overline{DRDY}$ indicates when this full-scale calibration is complete. When this calibration is complete, the part returns to Normal Mode.
1	0	0	System-Offset Calibration; this activates system offset calibration on the channel selected by CH2, CH1 and CH0 of the Communications Register. This is a one step calibration sequence and when complete the part returns to Normal Mode with $\overline{DRDY}$ indicating when this system offset calibration is complete. For this calibration type, the zero-scale calibration is done on the selected input channel and the full-scale calibration is done internally on V_{REF}.
1	0	1	Background Calibration; this activates background calibration on the channel selected by CH2, CH1 and CH0 of the Communications Register. If the background calibration mode is on, the AD7714 provides continuous self-calibration of the shorted (zeroed) inputs. This calibration takes place as part of the conversion sequence, extending the conversion time and reducing the word rate by a factor of six. Its major advantage is that the user does not have to worry about recalibrating the offset of the device when there is a change in the ambient temperature or supplies. In this mode, the shorted (zeroed) inputs, as well as the analog input voltage, are continuously monitored and the calibration registers of the device are automatically updated. Because the background calibration does not perform full-scale calibrations, a full-scale self-calibration should be performed before placing the part in background calibration mode.
1	1	0	Zero-Scale Self-Calibration; this activates zero-scale self-calibration on the channel selected by CH2, CH1 and CH0 of the Communications Register. This zero-scale calibration is done internally on shorted (zeroed) inputs. This is a one step calibration sequence and when complete the part returns to Normal Mode. The $\overline{DRDY}$ output or bit indicates when this zero-scale self-calibration is complete.
1	1	1	Full-Scale Self-Calibration; this activates full-scale self-calibration on the channel selected by CH2, CH1 and CH0 of the Communications Register. This full-scale calibration is done internally on V_{REF}. This is a one step calibration sequence and when complete the part returns to Normal Mode. The $\overline{DRDY}$ output indicates when this full-scale self-calibration is complete.
G2	G1	G0	Gain Setting
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128
BO			Burn Out Current. A 0 in this bit turns off the on-chip burn out currents. This is the default (Power-On or RESET) status of this bit. A 1 in this bit activates the burn out currents.
FSYNC			Filter Synchronization. When this bit is high, the nodes of the digital filter, the filter control logic and the calibration control logic are reset, and the analog modulator is also held in its reset state. When this bit goes low, valid data is available in 3 × 1/(output update rate), i.e., the settling time of the filter.

Filter Registers. Power On/Reset Status: Filter High Register: 01 Hex. Filter Low Register: 40 Hex

There are two 8-bit Filter Registers on the AD7714 from which data can either be read or to which data can be written. Tables VIII and IX outline the bit designations for the Filter Registers.

Table VIII. Filter High Register (RS2–RS0 = 0, 1, 0)

$\overline{B}$/U	WL	BST	0	FS11	FS10	FS9	FS8

Table IX. Filter Low Register (RS2–RS0 = 0, 1, 1)

FS7	FS6	FS5	FS4	FS3	FS2	FS1	FS0

$\overline{B}$/U	Bipolar/Unipolar Operation. A 0 in this bit selects Bipolar Operation. This is the default (Power-On or $\overline{RESET}$) status of this bit. A 1 in this bit selects unipolar operation.
WL	Word Length. A 0 in this bit selects 16-bit word length when reading from the data register (i.e., $\overline{DRDY}$ returns high after 16 serial clock cycles). This is the default (Power-On or RESET) status of this bit. A 1 in this bit selects 24-bit word length.
BST	Current Boost. A 0 in this bit reduces the current taken by the analog front-end. When the part is operated with $f_{CLK\ IN}$ = 1 MHz, this bit should be 0 to reduce the current drawn from AV_{DD}. When the AD7714 is operated from $f_{CLK\ IN}$ = 2.4576 MHz with gains of 8 to 128, this bit needs to be 1 to ensure correct operation of the device. The Power-On or $\overline{RESET}$ status of this bit is 0.
0	To ensure correct operation of the part, a 0 must be written to this bit.
FS11–FS0	Filter Selection. The on-chip digital filter provides a $Sinc^3$ (or $(Sinx/x)^3$) filter response. The 12-bits of data programmed into these bits determine the filter cut-off frequency, the position of the first notch of the filter and the data rate for the part. In association with the gain selection, it also determines the output noise (and hence the effective resolution) of the device. The first notch of the filter occurs at a frequency determined by the relationship: *filter first notch frequency* = $(f_{CLK\ IN}/128)/code$ where *code* is the decimal equivalent of the code in bits FS0 to FS11 and is in the range 19 to 4,000. With the nominal $f_{CLK\ IN}$ of 2.4576 MHz, this results in a first notch frequency range from 4.8 Hz to 1.01 kHz. To ensure correct operation of the AD7714, the value of the code loaded to these bits must be within this range. Failure to do this will result in unspecified operation of the device. Changing the filter notch frequency, as well as the selected gain, impacts resolution. Tables I through IV show the effect of the filter notch frequency and gain on the effective resolution of the AD7714. The output data rate (or effective conversion time) for the device is equal to the frequency selected for the first notch of the filter. For example, if the first notch of the filter is selected at 50 Hz, then a new word is available at a 50 Hz rate or every 20 ms. If the first notch is at 1 kHz, a new word is available every 1 ms. The settling-time of the filter to a full-scale step input change is worst case 4 × 1/(output data rate). For example, with the first filter notch at 50 Hz, the settling time of the filter to a full-scale step input change is 80 ms max. If the first notch is at 1 kHz, the settling time of the filter to a full-scale input step is 4 ms max. This settling-time can be reduced to 3 × 1/(output data rate) by synchronizing the step input change to a reset of the digital filter. In other words, if the step input takes place with the $\overline{SYNC}$ input low or the FSYNC bit high, the settling-time time will be 3 × 1/(output data rate) from when $\overline{SYNC}$ returns high or FSYNC returns low. If a change of channel takes place, the settling-time is 3 × 1/(output data rate) regardless of the $\overline{SYNC}$ or FSYNC status as the part issues an internal SYNC command when requested to change channels. The –3 dB frequency is determined by the programmed first notch frequency according to the relationship: filter –3 dB frequency = 0.262 × first notch frequency.

Test Register (RS2–RS0 = 1, 0, 0)

The part contains a Test Register which is used in testing the device. The user is advised not to change the status of any of the bits in this register from the default (Power-On or RESET) status of all 0s as the part will be placed in one of its test modes and will not operate correctly. If the part enters one of its test modes, exercising $\overline{RESET}$ will exit the part from the mode.

Data Register (RS2–RS0 = 1, 0, 1)
The Data Register on the part is a read-only register which contains the most up-to-date conversion result from the AD7714. The register can be programmed to be either 16 bits or 24 bits wide, determined by the status of the WL bit of the Mode Register. If an attempt is made to write to this register, the 16 or 24 bits of data will not actually be written to any location of the AD7714.

Calibration Zero-Scale Register (RS2–RS0 = 1, 1, 0)
The AD7714 contains 3 zero-scale calibration registers, labelled Register 0 to Register 2. Each of these registers is a 24-bit read/write register and 24 bits must be written; otherwise no data will be transferred to the register. The register is used in conjunction with the associated full-scale calibration register to form a register pair. These register pairs are associated with input channel pairs as outlined in Table VI.

There is a possibility that after accessing the calibration registers (either read or write operation), the first output data read from the part contain incorrect data. In addition, a read or write operation to the calibration register should not be attempted while a calibration is in progress. These eventualities can be avoided by taking either the $\overline{\text{SYNC}}$ input low or the FSYNC bit of the Mode Register high before the calibration register operation and taking them either high or low respectively after the operation is complete.

Calibration Full-Scale Register (RS2–RS0 = 1, 1, 1)
The AD7714 contains 3 full-scale calibration registers, labelled Register 0 to Register 2. Each of these registers is a 24-bit read/write register and 24 bits must be written, otherwise no data will be transferred to the register. The register is used in conjunction with the associated zero scale calibration register to form a register pair. These register pairs are associated with input channel pairs as outlined in Table VI.

There is a possibility that after accessing the calibration registers (either read or write operation), the first output data read from the part will contain incorrect data. In addition, a read or write operation to the calibration register should not be attempted while a calibration is in progress. These eventualities can be avoided by taking either the $\overline{\text{SYNC}}$ input low or the FSYNC bit of the Mode Register high before the calibration register operation and taking them either high or low respectively after the operation is complete.

CIRCUIT DESCRIPTION

The AD7714 is a sigma-delta A/D converter with on-chip digital filtering, intended for the measurement of wide dynamic range, low frequency signals such as those in weigh-scale, industrial control or process control applications. It contains a sigma-delta (or charge-balancing) ADC, a calibration microcontroller with on-chip static RAM, a clock oscillator, a digital filter and a bidirectional serial communications port. The part consumes only 500 μA of power supply current, making it ideal for battery-powered or loop-powered instruments. The part comes in two versions, the AD7714-5 which is specified for operation from a +5 V analog supply (AV_{DD}) and the AD7714-3 which is specified for operation from a +3 V analog supply. The AD7714-5 can be operated with a digital supply (DV_{DD}) voltage of +3 V or +5 V.

The part contains three programmable-gain fully differential analog input channels which can be reconfigured as five pseudo-differential inputs. The gain range on all channels is from 1 to 128 allowing the part to accept unipolar signals of between 0 mV to +20 mV and 0 V to +2.5 V or bipolar signals in the range from ±20 mV to ±2.5 V when the reference input voltage equals +2.5 V. With a reference voltage of +1.25 V, the input ranges are from 0 mV to +10 mV to 0 V to +1.25 V in unipolar mode and from ±10 mV to ±1.25 V in bipolar mode.

The input signal to the selected analog input channel is continuously sampled at a rate determined by the frequency of the master clock, MCLK IN, and the selected gain. A charge-balancing A/D converter (Sigma-Delta Modulator) converts the sampled signal into a digital pulse train whose duty cycle contains the digital information. The programmable gain function on the analog input is also incorporated in this sigma delta modulator with the input sampling frequency being modified to give the higher gains. A $Sinc^3$ digital low-pass filter processes the output of the sigma-delta modulator and updates the output register at a rate determined by the first notch frequency of this filter. The output data can be read from the serial port randomly or periodically at any rate up to the output register update rate. The first notch of this digital filter (and hence its –3 dB frequency) can be programmed via the filter high and filter low registers. With a master clock frequency of 2.4576 MHz, the programmable range for this first notch frequency is from 4.8 Hz to 1.01 kHz giving a programmable range for the –3 dB frequency of 1.26 Hz to 265 Hz.

The basic connection diagram for the part is shown in Figure 2. This shows both the AV_{DD} and DV_{DD} pins of the AD7714 being driven from the analog +3 V or +5 V supply. Some applications will have AV_{DD} and DV_{DD} driven from separate supplies. In the connection diagram shown, the AD7714's analog inputs are configured as three fully differential inputs. The part is set up for unbuffered mode on the these analog inputs. An AD780, precision +2.5 V reference, provides the reference source for the part. On the digital side, the part is configured for three-wire operation with $\overline{\text{CS}}$ tied to DGND. A quartz crystal or ceramic resonator provides the master clock source for the part.

The AD7714 provides a number of calibration options which can be programmed via the MD2, MD1 and MD0 bits of the Mode Register. A calibration cycle may be initiated at any time by writing to these bits of the Mode Register. The part can perform self-calibration using the on-chip calibration microcontroller and SRAM to store calibration parameters. Other system components may also be included in the calibration loop to remove offset and gain errors in the input channel using the system calibration mode. Another option is a background calibration mode where the part continuously performs internal zero-scale calibrations and updates the calibration coefficients. Using the part in this mode, the user does not have to worry

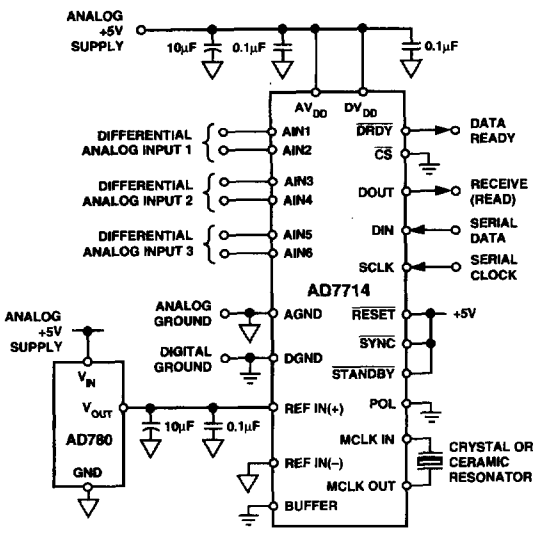

Figure 2. Basic Connection Diagram

about issuing periodic calibration commands to the device or ask the device to recalibrate when there is a change in the ambient temperature or power supply voltage. This automatic removal of offset errors is achieved at the expense of output update rate which is reduced by a factor of six. Using the part in background calibration mode automatically removes offset errors but not full-scale errors. A full-scale self-calibration should be performed before entering the background calibration mode. The residual gain drift in background calibration mode is 2 ppm/°C.

The AD7714 gives the user access to the on-chip calibration registers allowing the microprocessor to read the device's calibration coefficients and also to write its own calibration coefficients to the part from prestored values in E^{2}PROM. This gives the microprocessor much greater control over the AD7714's calibration procedure. It also means that the user can verify that the device has performed its calibration correctly by comparing the coefficients after calibration with prestored values in E^{2}PROM. Table X details the calibration options and sequences available on the AD7714. For the table, Sel Gain refers to the selected operating gain.

DIGITAL INTERFACE

The AD7714's serial interface consists of five signals, $\overline{CS}$, SCLK, DIN, DOUT and $\overline{DRDY}$. The DIN line is used for

Table X. Calibration Sequences

Calibration Type	MD2, MD1, MD0	Calibration Sequence	Duration
Self Calibration	0, 0, 1	Internal ZS Cal @ Sel Gain + Internal FS Cal @ Sel Gain	9 × 1/Output Rate
ZS System Calibration	0, 1, 0	ZS Cal on AIN @ Sel Gain	3 × 1/Output Rate
FS System Calibration	0, 1, 1	FS Cal on AIN @ Sel Gain	3 × 1/Output Rate
System-Offset Calibration	1, 0, 0	ZS Cal on AIN @ Sel Gain + Internal FS Cal @ Sel Gain	9 × 1/Output Rate
Background Calibration	1, 0, 1	Internal ZS Cal @ Sel Gain	6 × 1/Output Rate
ZS Self Calibration	1, 1, 0	Internal ZS Cal @ Sel Gain	3 × 1/Output Rate
FS Self Calibration	1, 1, 1	Internal FS Cal @ Sel Gain	3 × 1/Output Rate

transferring data into the on-chip registers while the DOUT line is used for accessing data from the on-chip registers. SCLK is the serial clock input for the device and all data transfers (either on DIN or DOUT) take place with respect to this SCLK signal. The $\overline{DRDY}$ line is used as a status signal to indicate when data is ready to be read from the AD7714's data register. $\overline{DRDY}$ goes low when a new data word is available in the output register. It is reset high when a read operation from the data register is complete. It also goes high prior to the updating of the output register to indicate when not to read from the device to ensure that a data read is not attempted while the register is being updated. $\overline{CS}$ is used to select the device. It can be used to decode the AD7714 in systems where a number of parts are connected to the serial bus.

The AD7714 serial interface can operate in three-wire mode by tying the $\overline{CS}$ input low. In this case, the SCLK, DIN and DOUT lines are used to communicate with the AD7714 and the status of $\overline{DRDY}$ can be obtained by interrogating the MSB of the Communications Register.

Figures 3 and 4 show timing diagrams for interfacing to the AD7714 with $\overline{CS}$ used to decode the part. Figure 3 is for a read operation from the AD7714's output shift register while Figure 4 shows a write operation to the input shift register. Both diagrams are for the POL input at a logic high; for operation with the POL input at a logic high simply invert the SCLK waveform shown in the diagrams. It is possible to read the same data twice from the output register even though the $\overline{DRDY}$ line returns high after the first read operation. Care must be taken, however, to ensure that the read operations have been completed before the next output update is about to take place.

The serial interface can be reset by exercising the $\overline{RESET}$ input on the part. It can also be reset by writing a series of 1s on the DIN input. If a logic 1 is written to the AD7714 DIN line for at least 32 serial clock cycles, the serial interface is reset. This ensures that in three-wire systems that if the interface gets lost either via a software error or by some glitch in the system, it can be reset back into a known state. This known state (which is also where the interface returns to after a $\overline{RESET}$) is that the part is expecting a write operation to the Communications Register.

Figure 3. Read Cycle Timing Diagram (POL = 1)

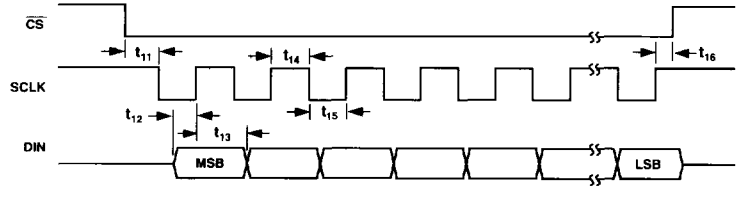

Figure 4. Write Cycle Timing Diagram (POL = 1)