1024-/256-Position, 1% Resistor Tolerance Error, SPI Interface and 50-TP Memory Digital Rheostat

AD5270/AD5271

FEATURES

Single-channel, 1024-/256-position resolution
20 kΩ, 50 kΩ, 100 kΩ nominal resistance
Maximum ±1% nominal resistor tolerance error
50-times programmable (50-TP) wiper memory
Rheostat mode temperature coefficient: 5 ppm/°C
2.7 V to 5.5 V single-supply operation
±2.5 V to ±2.75 V dual-supply operation for ac or bipolar operations
SPI-compatible interface
Wiper setting readback
Power on refreshed from 50-TP memory
Thin LFCSP, 10-lead, 3 mm × 3 mm × 0.8 mm package
Compact MSOP, 10-lead, 3 mm × 4.9 mm × 1.1 mm package

APPLICATIONS

Mechanical rheostat replacements
Op-amp: variable gain control
Instrumentation: gain, offset adjustment
Programmable voltage to current conversions
Programmable filters, delays, time constants
Programmable power supply
Sensor calibration

FUNCTIONAL BLOCK DIAGRAM

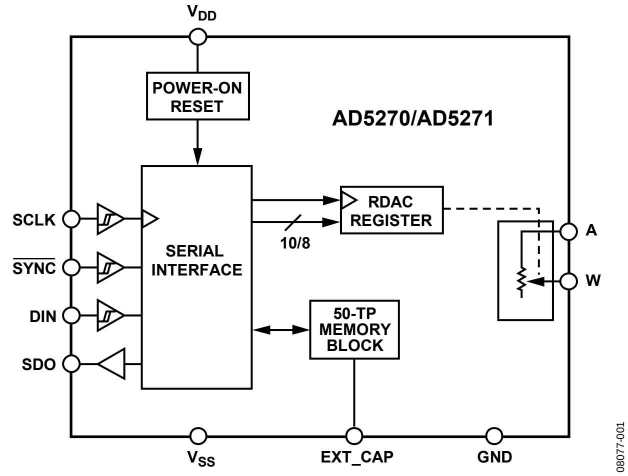

Figure 1.

GENERAL DESCRIPTION

The AD5270/AD5271[1] are single-channel, 1024-/256-position digital rheostats that combine industry leading variable resistor performance with nonvolatile memory (NVM) in a compact package.

The AD5270/AD5271 ensure less than 1% end-to-end resistor tolerance error and offer 50-times programmable (50-TP) memory.

The guaranteed industry leading low resistor tolerance error feature simplifies open-loop applications as well as precision calibration and tolerance matching applications.

The AD5270/AD5271 device wiper settings are controllable through the SPI digital interface. Unlimited adjustments are allowed before programming the resistance value into the 50-TP memory. The AD5270/AD5271 do not require any external voltage supply to facilitate fuse blow and there are 50 opportunities for permanent programming. During 50-TP activation, a permanent blow fuse command freezes the resistance position (analogous to placing epoxy on a mechanical trimmer).

The AD5270/AD5271 are available in a 3 mm × 3 mm, 10-lead LFCSP package and in a 10-lead MSOP package. The parts are guaranteed to operate over the extended industrial temperature range of −40°C to +125°C.

[1] Protected by U.S.Patent Number 7688240

Rev. E

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REVISION HISTORY

12/10—Rev. D to Rev. E

Changes to SDO Pin Description ... 10
Changes to SDO Pin and Daisy-Chain Operation Section ... 21

11/10—Rev. C to Rev. D

Changes to Figure 25 ... 14

9/10—Rev. B to Rev. C

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Deleted Daisy-Chain Operation Section, Added SDO Pin and Daisy-Chain Operation Section ... 21

5/10—Rev. A to Rev. B

Added LFCSP Throughout ... 1
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Changes to Product Title, Features, and General Description ... 1
Changes to Table 1 ... 3
Added Table 3; Renumbered Sequentially ... 4
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Added Figure 6 and changes to Table 10 ... 10
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Updated Outline Dimensions ... 23
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3/10—Rev. 0 to Rev. A

Changes to Product Title and General Description ... 1

Changes to Theory of Operation Section ... 14

10/09—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—AD5270

V_{DD} = 2.7 V to 5.5 V, V_{SS} = 0 V; V_{DD} = 2.5 V to 2.75 V, V_{SS} = −2.5 V to −2.75 V; −40°C < T_A < +125°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS—RHEOSTAT MODE						
Resolution			10			Bits
Resistor Integral Nonlinearity[2, 3]	R-INL	R_{AW} = 20 kΩ, |V_{DD} − V_{SS}| = 3.0 V to 5.5 V	−1		+1	LSB
		R_{AW} = 20 kΩ, |V_{DD} − V_{SS}| = 2.7 V to 3.0 V	−1		+1.5	LSB
		R_{AW} = 50 kΩ, 100 kΩ	−1		+1	LSB
Resistor Differential Nonlinearity[2]	R-DNL		−1		+1	LSB
Nominal Resistor Tolerance						
R-Perf Mode[4]		See Table 2 and Table 3	−1	±0.5	+1	%
Normal Mode				±15		%
Resistance Temperature Coefficient[5, 6]		Code = full scale		5		ppm/°C
Wiper Resistance		Code = zero scale		35	70	Ω
RESISTOR TERMINALS						
Terminal Voltage Range[5, 7]			V_{SS}		V_{DD}	V
Capacitance[5] A		f = 1 MHz, measured to GND, code = half scale		90		pF
Capacitance[5] W		f = 1 MHz, measured to GND, code = half scale		40		pF
Common-Mode Leakage Current[5]		V_A = V_W			50	nA
DIGITAL INPUTS						
Input Logic[5]						
High	V_{INH}		2.0			V
Low	V_{INL}				0.8	V
Input Current	I_{IN}			±1		µA
Input Capacitance[5]	C_{IN}			5		pF
DIGITAL OUTPUT						
Output Voltage[5]						
High	V_{OH}	R_{PULL_UP} = 2.2 kΩ to V_{DD}	V_{DD} − 0.1			V
Low	V_{OL}	R_{PULL_UP} = 2.2 kΩ to V_{DD}				
		V_{DD} = 2.7 V to 5.5 V, V_{SS} = 0 V			0.4	V
		V_{DD} = 2.5 V to 2.75 V, V_{SS} = −2.5 V to −2.75 V			0.6	V
Tristate Leakage Current			−1		+1	µA
Output Capacitance[5]				5		pF
POWER SUPPLIES						
Single-Supply Power Range		V_{SS} = 0 V	2.7		5.5	V
Dual-Supply Power Range			±2.5		±2.75	V
Supply Current						
Positive	I_{DD}				1	µA
Negative	I_{SS}		−1			µA
50-TP Store Current[5, 8]						
Positive	$I_{DD\_OTP\_STORE}$			4		mA
Negative	$I_{SS\_OTP\_STORE}$			−4		mA
OTP Read Current[5, 9]						
Positive	$I_{DD\_OTP\_READ}$				500	µA
Negative	$I_{SS\_OTP\_READ}$		−500			µA

Parameter	Symbol	Test Conditions/Comments	Min	Typ[1]	Max	Unit
Power Dissipation[10]		$V_{IH} = V_{DD}$ or V_{IL} = GND			5.5	μW
Power Supply Rejection Ratio[5]	PSRR	$\Delta V_{DD}/\Delta V_{SS}$ = ±5 V ± 10%				dB
		R_{AW} = 20 kΩ		−66	−55	
		R_{AW} = 50 kΩ		−75	−67	
		R_{AW} = 100 kΩ		−78	−70	
DYNAMIC CHARACTERISTICS[5, 11]						
Bandwidth		−3 dB, R_{AW} = 10 kΩ, Terminal W, see Figure 42				kHz
		R_{AW} = 20 kΩ		300		
		R_{AW} = 50 kΩ		120		
		R_{AW} = 100 kΩ		60		
Total Harmonic Distortion		V_A = 1 V rms, f = 1 kHz, code = half scale				dB
		R_{AW} = 20 kΩ		−90		
		R_{AW} = 50 kΩ		−88		
		R_{AW}= 100 kΩ		−85		
Resistor Noise Density		Code = half scale, T_A = 25°C				nV/√Hz
		R_{AW} = 20 kΩ		50		
		R_{AW} = 50 kΩ		25		
		R_{AW} = 100 kΩ		32		

[1] Typical specifications represent average readings at 25°C, V_{DD} = 5 V, and V_{SS} = 0 V.
[2] Resistor position nonlinearity error (R-INL) is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions.
[3] The maximum current in each code is defined by $I_{AW} = (V_{DD} - 1)/R_{AW}$.
[4] The terms resistor performance mode and R-Perf mode are used interchangeably. See the Resistor Performance Mode section.
[5] Guaranteed by design and not subject to production test.
[6] See Figure 25 for more details.
[7] Resistor Terminal A and Resistor Terminal W have no limitations on polarity with respect to each other. Dual-supply operation enables ground referenced bipolar signal adjustment.
[8] Different from operating current, the supply current for the fuse program lasts approximately 55 ms.
[9] Different from operating current, the supply current for the fuse read lasts approximately 500 ns.
[10] P_{DISS} is calculated from $(I_{DD} \times V_{DD}) + (I_{SS} \times V_{SS})$.
[11] All dynamic characteristics use V_{DD} = +2.5 V, V_{SS} = −2.5 V.

Table 2. AD5270—20 kΩ Resistor Performance Mode Code Range

Resistor Tolerance Per Code	$\lvert V_{DD} - V_{SS}\rvert$ = 4.5 V to 5.5 V	$\lvert V_{DD} - V_{SS}\rvert$ = 2.7 V to 4.5 V
R-TOLERANCE		
1% R-Tolerance	From 0x078 to 0x3FF	From 0x0BE to 0x3FF
2% R-Tolerance	From 0x037 to 0x3FF	From 0x055 to 0x3FF
3% R-Tolerance	From 0x028 to 0x3FF	From 0x037 to 0x3FF

Table 3. AD5270—50 kΩ and 100 kΩ Resistor Performance Mode Code Range

Resistor Tolerance Per Code	R_{AW} = 50 kΩ	R_{AW} = 100 kΩ
R-TOLERANCE		
1% R-Tolerance	From 0x078 to 0x3FF	From 0x04B to 0x3FF
2% R-Tolerance	From 0x055 to 0x3FF	From 0x032 to 0x3FF
3% R-Tolerance	From 0x032 to 0x3FF	From 0x019 to 0x3FF

ELECTRICAL CHARACTERISTICS—AD5271

V_{DD} = 2.7 V to 5.5 V, V_{SS} = 0 V; V_{DD} = 2.5 V to 2.75 V, V_{SS} = −2.5 V to −2.75 V; −40°C < T_A < +125°C, unless otherwise noted.

Table 4.

Parameter	Symbol	Test Conditions/Comments	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS—RHEOSTAT MODE						
Resolution			8			Bits
Resistor Integral Nonlinearity[2, 3]	R-INL		−1		+1	LSB
Resistor Differential Nonlinearity[2]	R-DNL		−1		+1	LSB
Nominal Resistor Tolerance						
R-Perf Mode[4]		See Table 5 and Table 6	−1	±0.5	+1	%
Normal Mode				±15		%
Resistance Temperature Coefficient[5, 6]		Code = full scale		5		ppm/°C
Wiper Resistance		Code = zero scale		35	70	Ω
RESISTOR TERMINALS						
Terminal Voltage Range[5, 7]			V_{SS}		V_{DD}	V
Capacitance[5] A		f = 1 MHz, measured to GND, code = half scale		90		pF
Capacitance[5] W		f = 1 MHz, measured to GND, code = half scale		40		pF
Common-Mode Leakage Current[5]		$V_A = V_W$			50	nA
DIGITAL INPUTS						
Input Logic[5]						
High	V_{INH}		2.0			V
Low[5]	V_{INL}				0.8	V
Input Current	I_{IN}			±1		μA
Input Capacitance[5]	C_{IN}			5		pF
DIGITAL OUTPUT						
Output Voltage[5]						
High	V_{OH}	R_{PULL_UP} = 2.2 kΩ to V_{DD}	V_{DD} − 0.1			V
Low	V_{OL}	R_{PULL_UP} = 2.2 kΩ to V_{DD}				
		V_{DD} = 2.7 V to 5.5 V, V_{SS} = 0 V			0.4	V
		V_{DD} = 2.5 V to 2.75 V, V_{SS} = −2.5 V to −2.75 V			0.6	V
Tristate Leakage Current			−1		+1	μA
Output Capacitance[5]				5		pF
POWER SUPPLIES						
Single-Supply Power Range		V_{SS} = 0 V	2.7		5.5	V
Dual-Supply Power Range			±2.5		±2.75	V
Supply Current						
Positive	I_{DD}				1	μA
Negative	I_{SS}		−1			μA
50-TP Store Current[5, 8]						
Positive	$I_{DD\_OTP\_STORE}$			4		mA
Negative	$I_{SS\_OTP\_STORE}$			−4		mA
OTP Read Current[5, 9]						
Positive	$I_{DD\_OTP\_READ}$				500	μA
Negative	$I_{SS\_OTP\_READ}$		−500			μA
Power Dissipation[10]		$V_{IH} = V_{DD}$ or V_{IL} = GND			5.5	μW
Power Supply Rejection Ratio[5]	PSRR	$\Delta V_{DD}/\Delta V_{SS}$ = ±5 V ± 10%				dB
		R_{AW} = 20 kΩ		−66	−55	
		R_{AW} = 50 kΩ		−75	−67	
		R_{AW} = 100 kΩ		−78	−70	

Parameter	Symbol	Test Conditions/Comments	Min	Typ[1]	Max	Unit
DYNAMIC CHARACTERISTICS[5, 11]						
Bandwidth		−3 dB, R_{AW} = 10 kΩ, Terminal W, see Figure 42				kHz
		R_{AW} = 20 kΩ		300		
		R_{AW} = 50 kΩ		120		
		R_{AW} = 100 kΩ		60		
Total Harmonic Distortion		V_A = 1 V rms, f = 1 kHz, code = half scale				dB
		R_{AW} = 20 kΩ		−90		
		R_{AW} = 50 kΩ		−88		
		R_{AW} = 100 kΩ		−85		
Resistor Noise Density		Code = half scale, T_A = 25°C				nV/√Hz
		R_{AW} = 20 kΩ		50		
		R_{AW} = 50 kΩ		25		
		R_{AW} = 100 kΩ		32		

[1] Typical specifications represent average readings at 25°C, V_{DD} = 5 V, and V_{SS} = 0 V.
[2] Resistor position nonlinearity error (R-INL) is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions.
[3] The maximum current in each code is defined by $I_{AW} = (V_{DD} - 1)/R_{AW}$.
[4] The terms resistor performance mode and R-Perf mode are used interchangeably. See the Resistor Performance Mode section.
[5] Guaranteed by design and not subject to production test.
[6] See Figure 25 for more details.
[7] Resistor Terminal A and Resistor Terminal W have no limitations on polarity with respect to each other. Dual-supply operation enables ground referenced bipolar signal adjustment.
[8] Different from operating current, the supply current for the fuse program lasts approximately 55 ms.
[9] Different from operating current, the supply current for the fuse read lasts approximately 500 ns.
[10] P_{DISS} is calculated from $(I_{DD} \times V_{DD}) + (I_{SS} \times V_{SS})$.
[11] All dynamic characteristics use V_{DD} = +2.5 V, V_{SS} = −2.5 V.

Table 5. AD5271—20 kΩ Resistor Performance Mode Code Range

Resistor Tolerance per Code	$\lvert V_{DD} - V_{SS} \rvert$ = 4.5 V to 5.5 V	$\lvert V_{DD} - V_{SS} \rvert$ = 2.7 V to 4.5 V
R-TOLERANCE		
1% R-Tolerance	From 0x1E to 0xFF	From 0x32 to 0xFF
2% R-Tolerance	From 0x0F to 0xFF	From 0x19 to 0xFF
3% R-Tolerance	From 0x06 to 0xFF	From 0x0E to 0xFF

Table 6. AD5271—50 kΩ and 100 kΩ Resistor Performance Mode Code Range

Resistor Tolerance per Code	R_{AW} = 50 kΩ	R_{AW} = 100 kΩ
R-TOLERANCE		
1% R-Tolerance	From 0x1E to 0xFF	From 0x14 to 0xFF
2% R-Tolerance	From 0x14 to 0xFF	From 0x0F to 0xFF
3% R-Tolerance	From 0x0A to 0xFF	From 0x0A to 0xFF

INTERFACE TIMING SPECIFICATIONS

V_{DD} = 2.5 V to 5.5 V, V_{SS} = 0 V; V_{DD} = 2.5 V, V_{SS} = −2.5 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 7.

Parameter	Limit[1]	Unit	Test Conditions/Comments
t_1[2]	20	ns min	SCLK cycle time
t_2	10	ns min	SCLK high time
t_3	10	ns min	SCLK low time
t_4	15	ns min	$\overline{\text{SYNC}}$ to SCLK falling edge setup time
t_5	5	ns min	Data setup time
t_6	5	ns min	Data hold time
t_7	1	ns min	SCLK falling edge to $\overline{\text{SYNC}}$ rising edge
t_8[3, 4]	500	ns min	Minimum $\overline{\text{SYNC}}$ high time
t_9	15	ns min	$\overline{\text{SYNC}}$ rising edge to next SCLK fall ignored
t_{10}[5]	450	ns max	SCLK rising edge to SDO valid
$t_{RDAC\_R\text{-}PERF}$	2	µs max	RDAC register write command execute time
t_{RDAC_NORMAL}	600	ns max	RDAC register write command execute time
t_{MEMORY_READ}	6	µs max	Memory readback execute time
$t_{MEMORY\_PROGRAM}$	350	ms max	Memory program time
t_{RESET}	0.6	ms max	Reset 50-TP restore time
$t_{POWER\text{-}UP}$[6]	2	ms max	Power-on 50-TP restore time

[1] All input signals are specified with tr = tf = 1 ns/V (10% to 90% of V_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2.
[2] Maximum SCLK frequency is 50 MHz.
[3] Refer to $t_{RDAC\_R\text{-}PER}$ and t_{RDAC_NORMAL} for RDAC register write operations.
[4] Refer to t_{MEMORY_READ} and $t_{MEMORY\_PROGRAM}$ for memory commands operations.
[5] R_{PULL_UP} = 2.2 kΩ to V_{DD} with a capacitance load of 168 pF.
[6] Maximum time after V_{DD} − V_{SS} is equal to 2.5 V.

Shift Register and Timing Diagrams

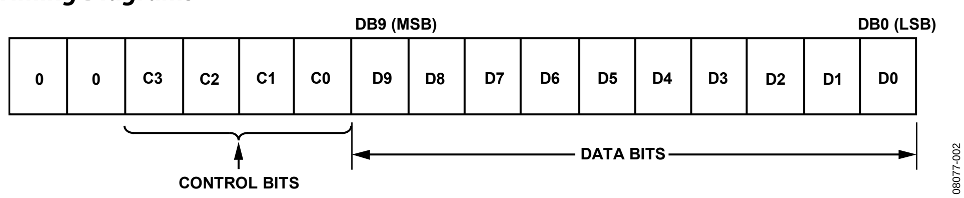


Figure 2. Shift Register Content

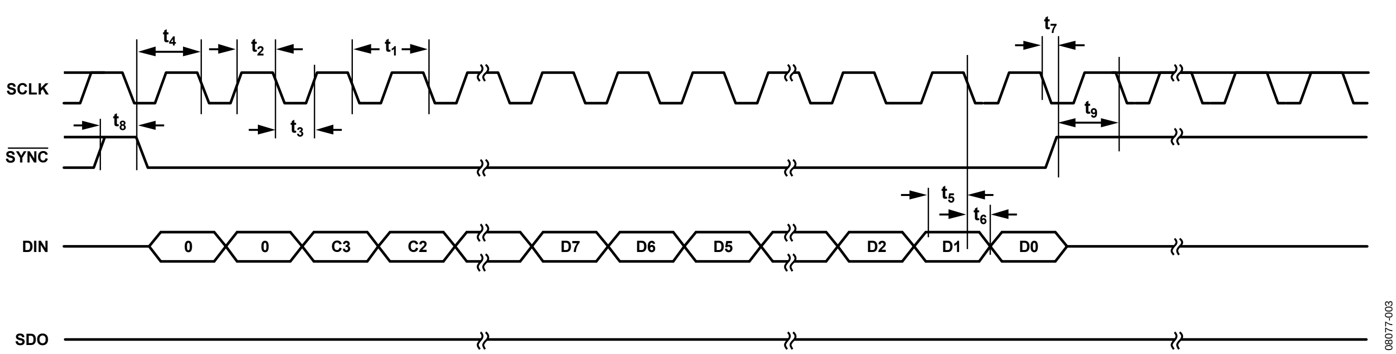


Figure 3. Write Timing Diagram (CPOL = 0, CPHA = 1)

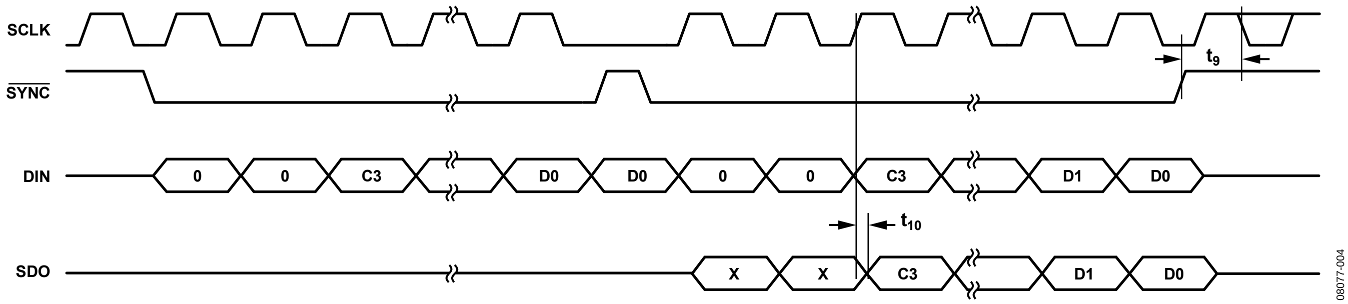


Figure 4. Read Timing Diagram (CPOL = 0, CPHA = 1)

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 8.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7.0 V
V_{SS} to GND	+0.3 V to −7.0 V
V_{DD} to V_{SS}	7 V
V_A, V_W to GND	V_{SS} − 0.3 V, V_{DD} + 0.3 V
Digital Input and Output Voltage to GND	−0.3 V to V_{DD} + 0.3 V
EXT_CAP to V_{SS}	7 V
I_A, I_W	
Continuous	
R_{AW} = 20 kΩ	±3 mA
R_{AW} = 50 kΩ, 100 kΩ	±2 mA
Pulsed[1]	
Frequency > 10 kHz	±MCC[2]/d[3]
Frequency ≤ 10 kHz	±MCC[2]/√d[3]
Operating Temperature Range[4]	−40°C to +125°C
Maximum Junction Temperature (T_J Maximum)	150°C
Storage Temperature Range	−65°C to +150°C
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	20 sec to 40 sec
Package Power Dissipation	(T_J max − T_A)/θ_{JA}

[1] Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A and W terminals at a given resistance.
[2] Maximum continuous current.
[3] Pulse duty factor.
[4] Includes programming of 50-TP memory.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

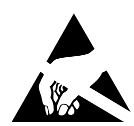
θ_{JA} is defined by JEDEC specification JESD-51 and the value is dependent on the test board and test environment.

Table 9. Thermal Resistance

Package Type	θ_{JA}[1]	θ_{JC}	Unit
10-Lead LFCSP	50	3	°C/W
10-Lead MSOP	135	N/A	°C/W

[1] JEDEC 2S2P test board, still air (0 m/s air flow).

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

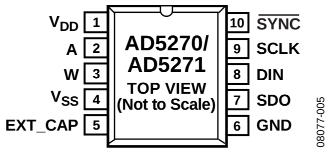


Figure 5. MSOP Pin Configuration

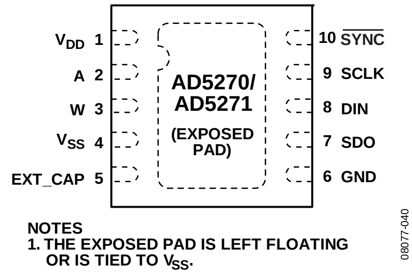


Figure 6. LFCSP Pin Configuration

Table 10. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD}	Positive Power Supply. Decouple this pin with 0.1 µF ceramic capacitors and 10 µF capacitors.
2	A	Terminal A of RDAC. $V_{SS} \leq V_A \leq V_{DD}$.
3	W	Wiper Terminal of RDAC. $V_{SS} \leq V_W \leq V_{DD}$.
4	V_{SS}	Negative Supply. Connect to 0 V for single-supply applications. Decouple this pin with 0.1 µF ceramic capacitors and 10 µF capacitors.
5	EXT_CAP	External Capacitor. Connect a 1 µF capacitor between EXT_CAP and V_{SS}. This capacitor must have a voltage rating of ≥7 V.
6	GND	Ground Pin, Logic Ground Reference.
7	SDO	Serial Data Output. This pin can be used to clock data from the shift register in daisy-chain mode or in readback mode. This open-drain output requires an external pull-up resistor even if it is not use.
8	DIN	Serial Data Line. This pin is used in conjunction with the SCLK line to clock data into or out of the 16-bit input register.
9	SCLK	Serial Clock Input. Data is clocked into the shift register on the falling edge of the serial clock input. Data can be transferred at rates up to 50 MHz.
10	$\overline{\text{SYNC}}$	Falling Edge Synchronization Signal. This is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes low, it enables the shift register and data is transferred in on the falling edges of the subsequent clocks. The selected register is updated on the rising edge of $\overline{\text{SYNC}}$ following the 16^{th} clock cycle. If $\overline{\text{SYNC}}$ is taken high before the 16^{th} clock cycle, the rising edge of $\overline{\text{SYNC}}$ acts as an interrupt, and the write sequence is ignored by the RDAC.
EPAD	Exposed Pad	Leave floating or connected to V_{SS}.

TYPICAL PERFORMANCE CHARACTERISTICS

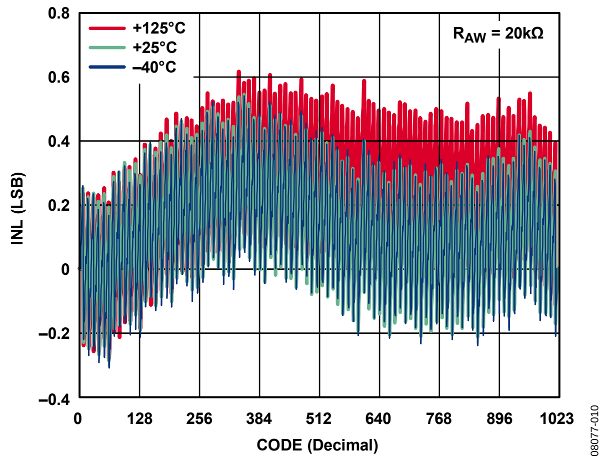


Figure 7. R-INL in R-Perf Mode vs. Code vs. Temperature (AD5270)

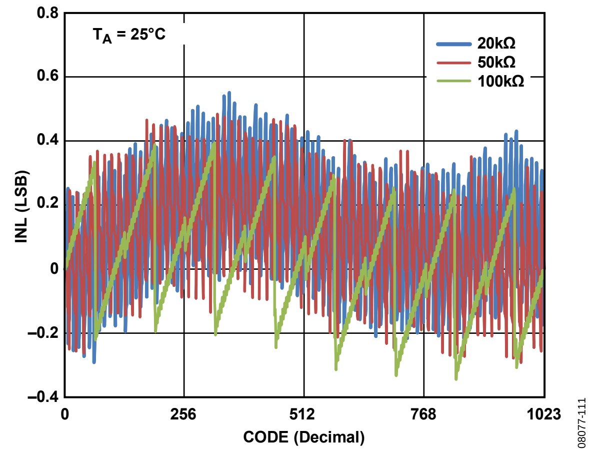


Figure 10. R-INL in R-Perf Mode vs. Code vs. Nominal Resistance (AD5270)

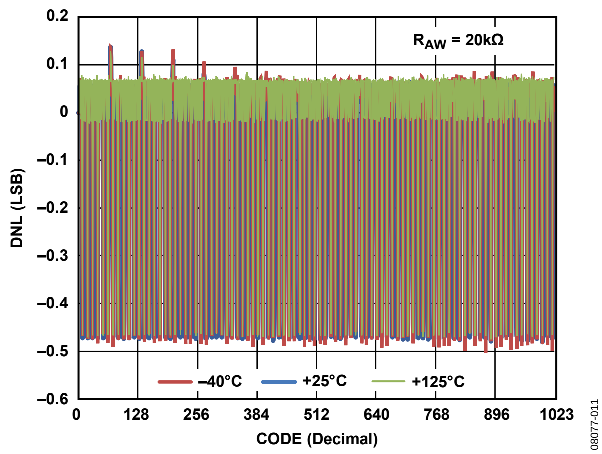


Figure 8. R-DNL in R-Perf Mode vs. Code vs. Temperature (AD5270)

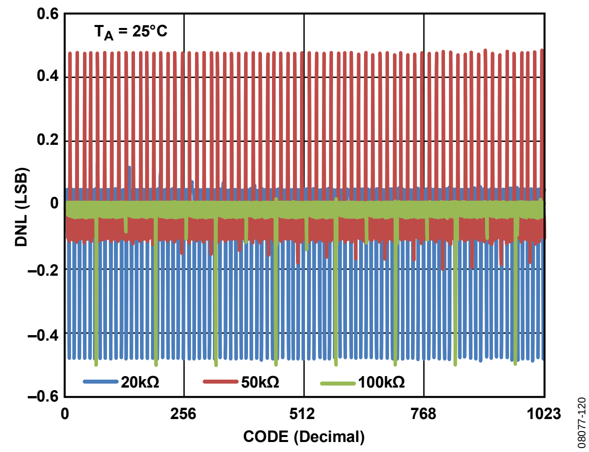


Figure 11. R-DNL in R-Perf Mode vs. Code vs. Nominal Resistance (AD5270)

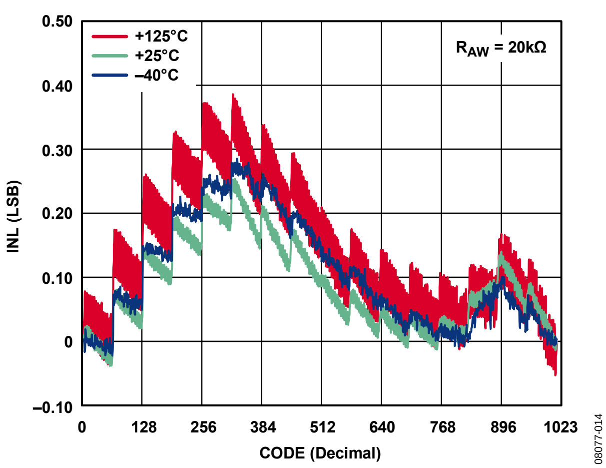


Figure 9. R-INL in Normal Mode vs. Code vs. Temperature (AD5270)

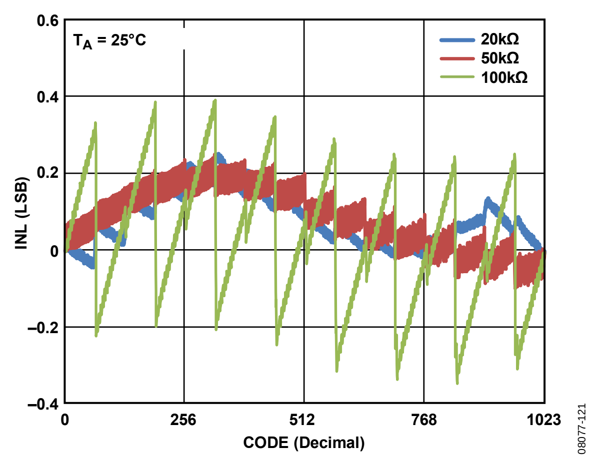


Figure 12. R-INL in Normal Mode vs. Code vs. Nominal Resistance (AD5270)

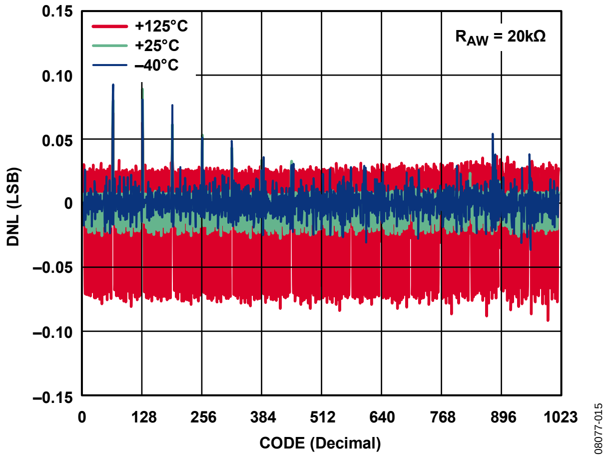


Figure 13. R-DNL in Normal Mode vs. Code vs. Temperature (AD5270)

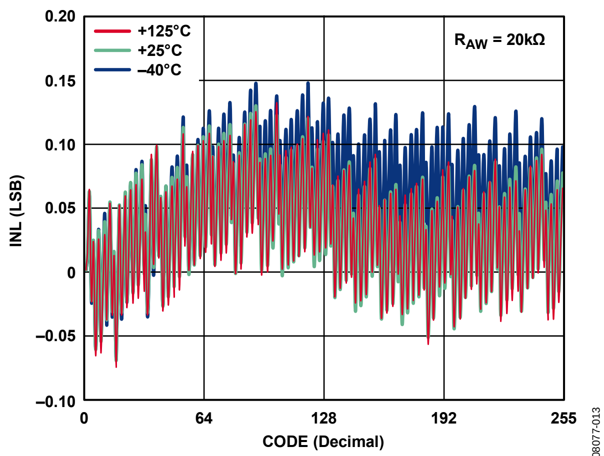


Figure 14. R-INL in R-Perf Mode vs. Code vs. Temperature (AD5271)

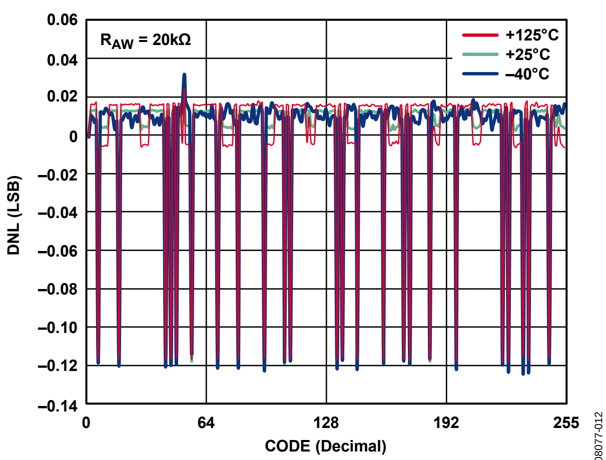


Figure 15. R-DNL in R-Perf Mode vs. Code vs. Temperature (AD5271)

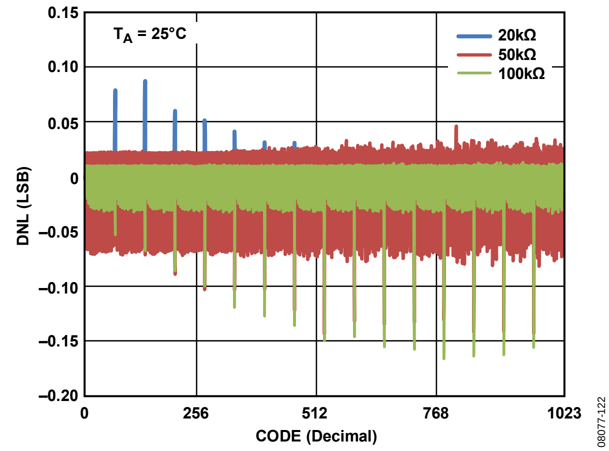


Figure 16. R-DNL in Normal Mode vs. Code vs. Nominal Resistance (AD5270)

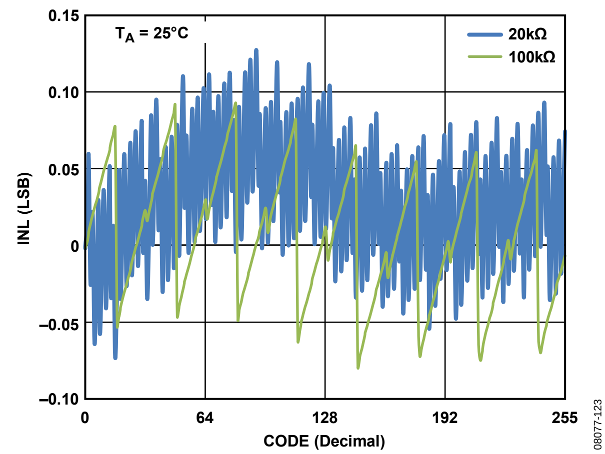


Figure 17. R-INL in R-Perf Mode vs. Code vs. Nominal Resistance (AD5271)

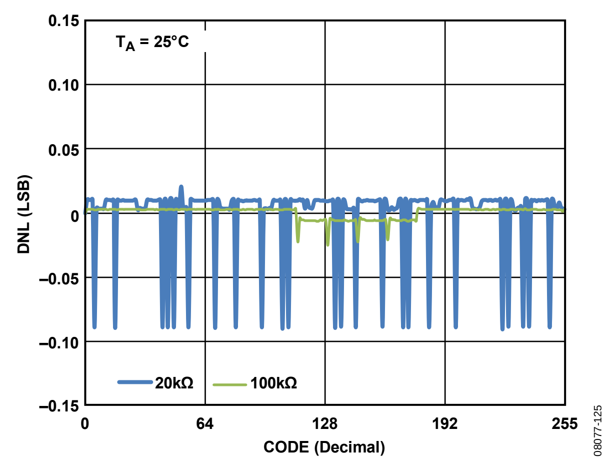


Figure 18. R-DNL in R-Perf Mode vs. Code vs. Nominal Resistance (AD5271)

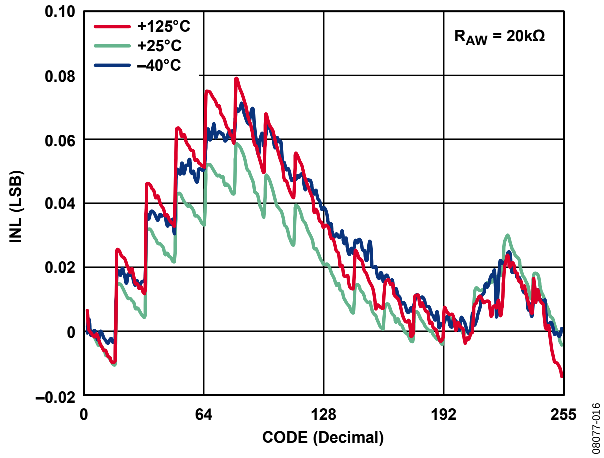


Figure 19. R-INL in Normal Mode vs. Code vs. Temperature (AD5271)

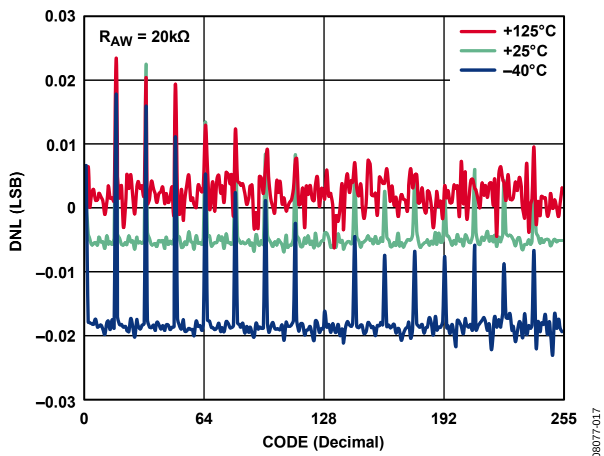


Figure 20. R-DNL in Normal Mode vs. Code vs. Temperature (AD5271)

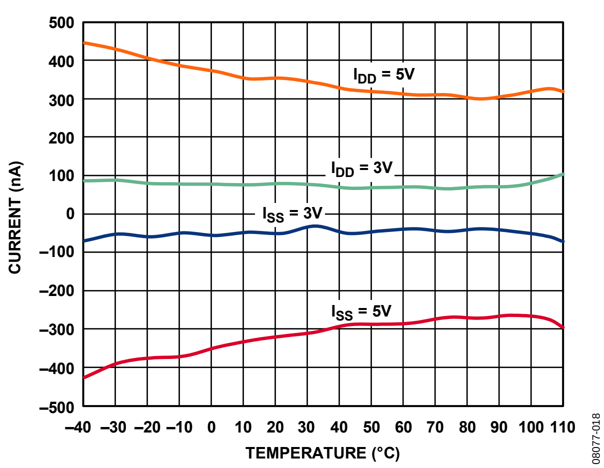


Figure 21. Supply Current (I_{DD}, I_{SS}) vs. Temperature

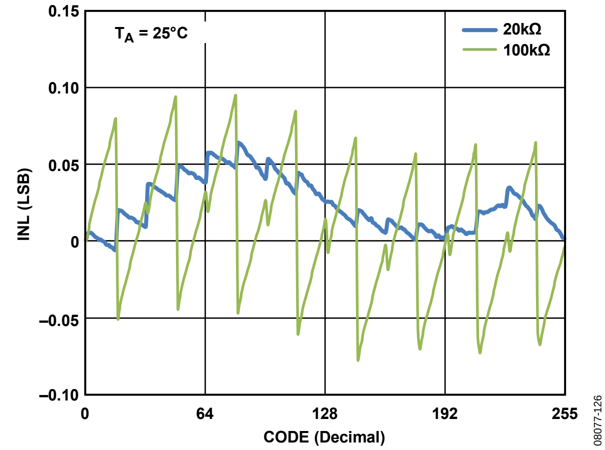


Figure 22. R-INL in Normal Mode vs. Code vs. Nominal Resistance (AD5271)

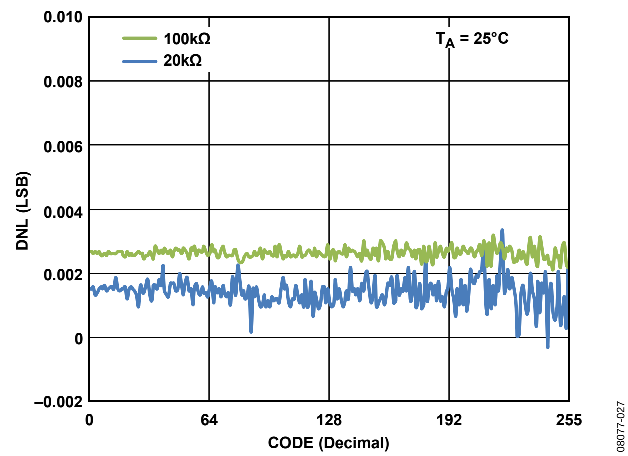


Figure 23. R-DNL in Normal Mode vs. Code vs. Nominal Resistance (AD5271)

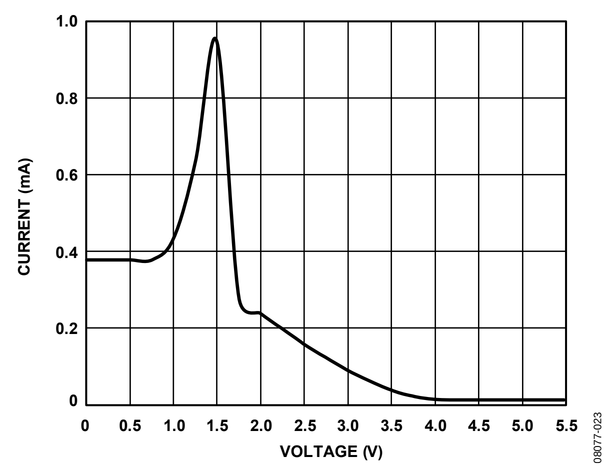


Figure 24. Supply Current I_{DD} vs. Digital Input Voltage

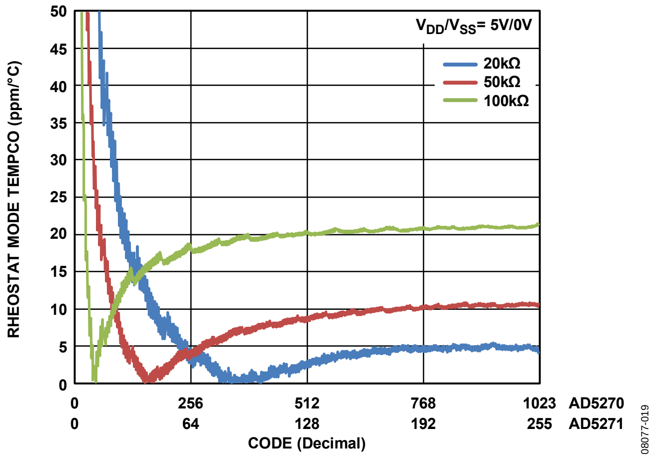


Figure 25. Tempco $\Delta R_{WA}/\Delta T$ vs. Code

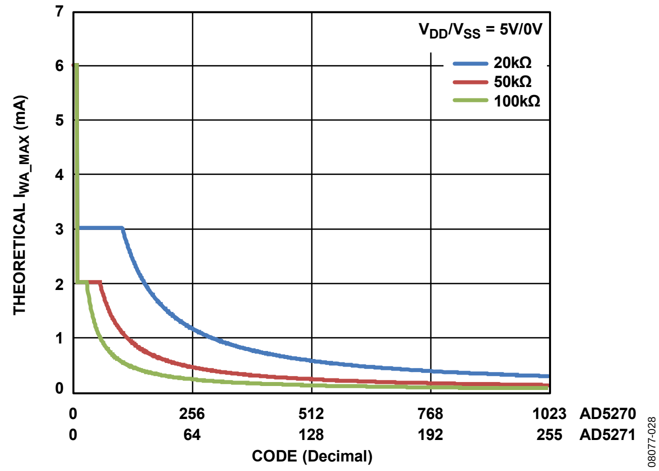


Figure 28. Theoretical Maximum Current vs. Code

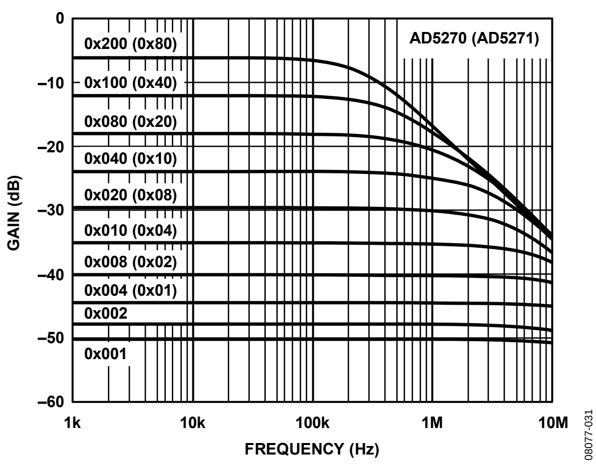


Figure 26. 20 kΩ Gain vs. Code vs. Frequency

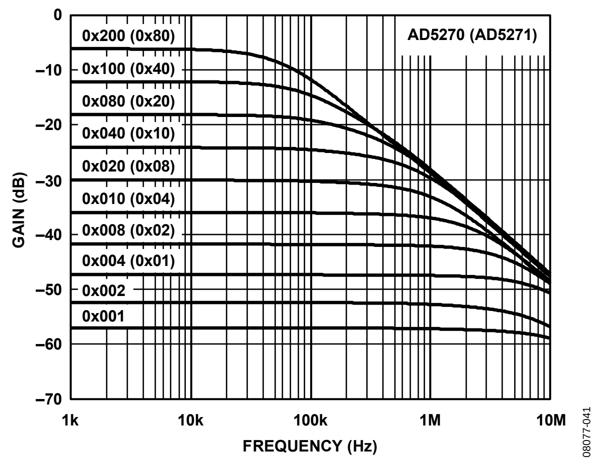


Figure 29. 100 kΩ Gain vs. Code vs. Frequency

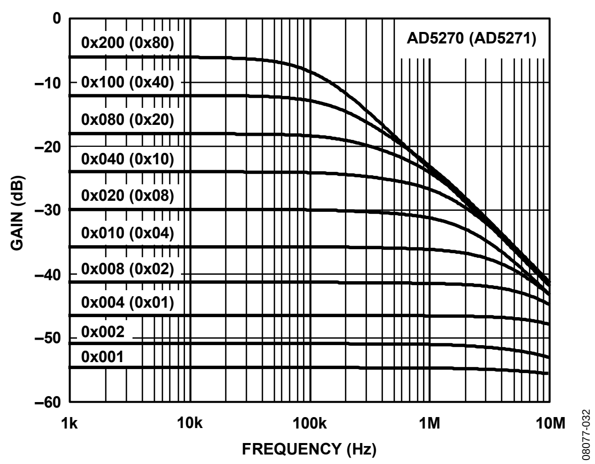


Figure 27. 50 kΩ Gain vs. Code vs. Frequency

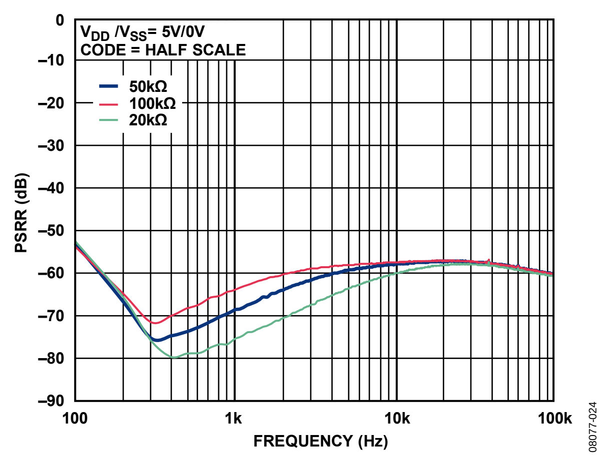


Figure 30. PSRR vs. Frequency

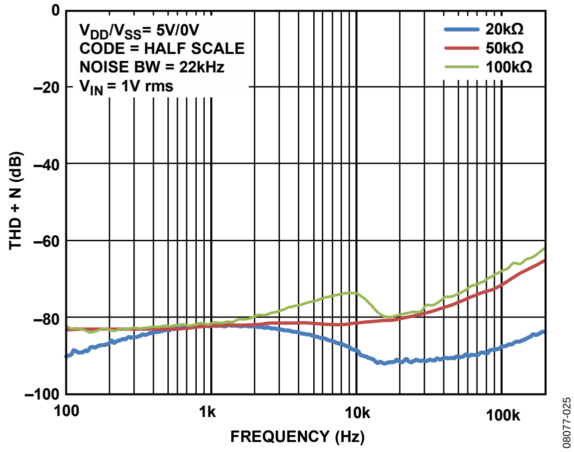


Figure 31. THD + N vs. Frequency

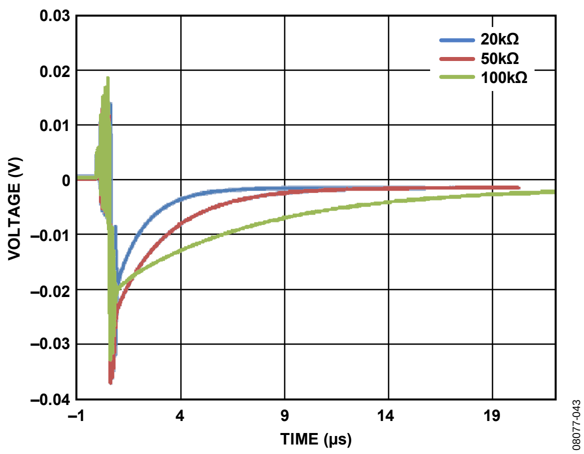


Figure 32. Maximum Glitch Energy

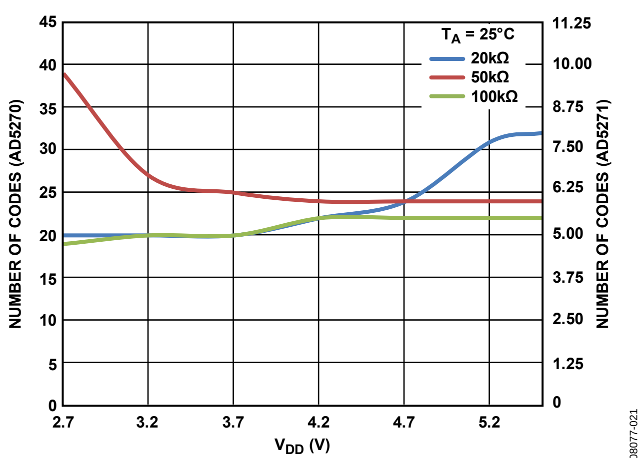


Figure 33. Maximum Code Loss vs. Voltage

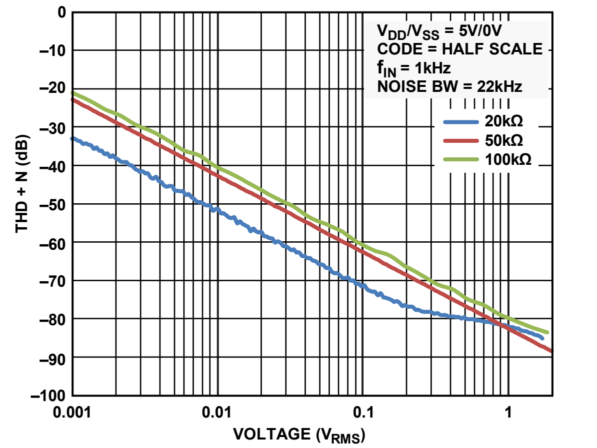


Figure 34. THD + N vs. Amplitude

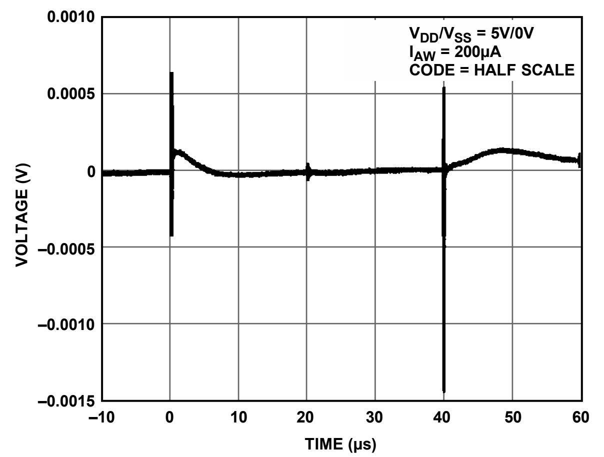


Figure 35. Digital Feedthrough

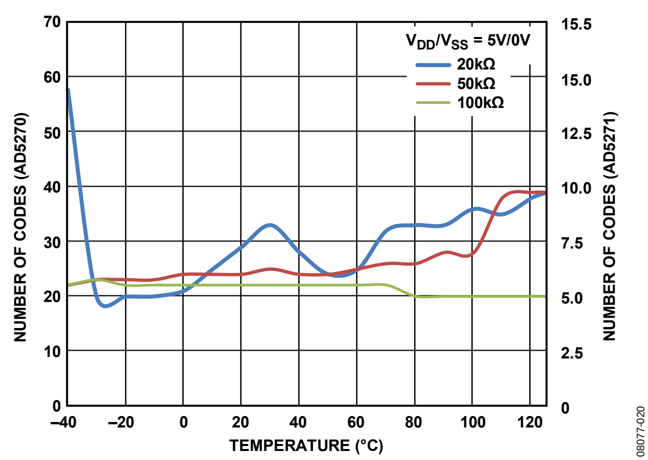


Figure 36. Maximum Code Loss vs. Temperature

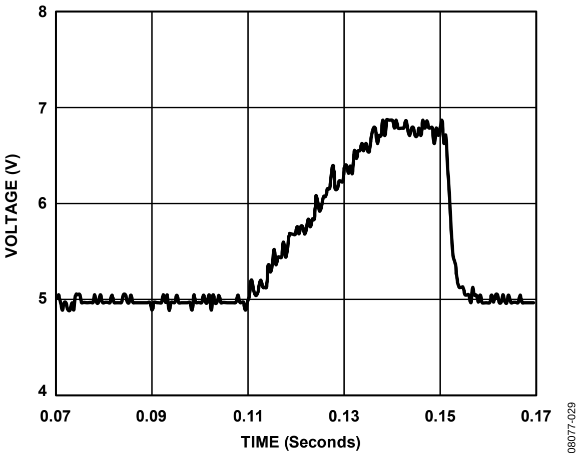


Figure 37. V_{EXT_CAP} Waveform While Writing Fuse

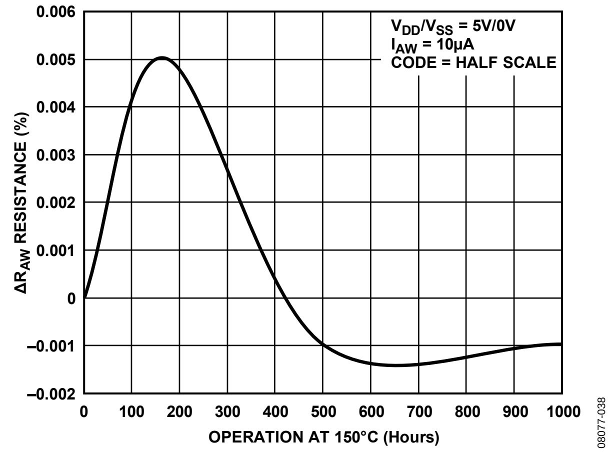


Figure 38. Long-Term Drift Accelerated Average by Burn-In

TEST CIRCUITS

Figure 39 to Figure 43 define the test conditions used in the Specifications section.

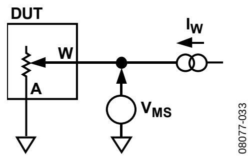


Figure 39. Resistor Position Nonlinearity Error (Rheostat Operation; R-INL, R-DNL)

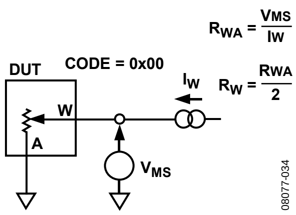


Figure 40. Wiper Resistance

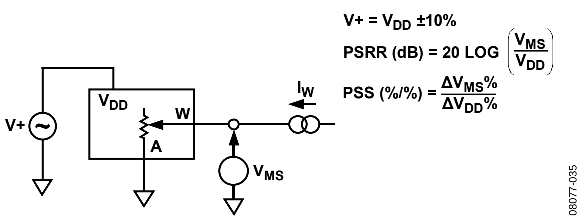


Figure 41. Power Supply Sensitivity (PSS, PSRR)

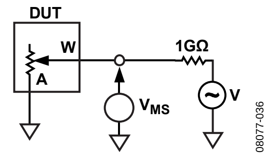


Figure 42. Gain vs. Frequency

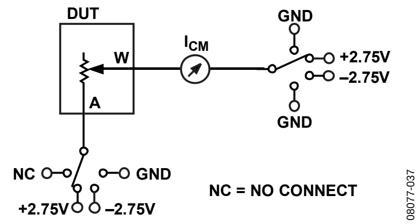


Figure 43. Common Leakage Current

THEORY OF OPERATION

The AD5270 and AD5271 are designed to operate as true variable resistors for analog signals within the terminal voltage range of $V_{SS} < V_{TERM} < V_{DD}$. The RDAC register contents determine the resistor wiper position. The RDAC register acts as a scratchpad register, which allows unlimited changes of resistance settings. The RDAC register can be programmed with any position setting using the SPI interface. When a desirable wiper position is found, this value can be stored in a 50-TP memory register. Thereafter, the wiper position is always restored to that position for subsequent power-up. The storing of 50-TP data takes approximately 350 ms; during this time, the AD5270/AD5271 lock to prevent any changes from taking place.

The AD5270/AD5271 also feature a patented 1% end-to-end resistor tolerance. This simplifies precision, rheostat mode, and open-loop applications where knowledge of absolute resistance is critical.

SERIAL DATA INTERFACE

The AD5270/AD5271 contain a serial interface ($\overline{SYNC}$, SCLK, DIN , and SDO), which is compatible with SPI interface standards, as well as most DSPs. This device allows writing of data via the serial interface to every register.

SHIFT REGISTER

For the AD5270/AD5271, the shift register is 16 bits wide, as shown in Figure 2. The 16-bit word consists of two unused bits, which should be set to zero, followed by four control bits and 10 RDAC data bits (note that for the AD5271 only, the lower two RDAC data bits are don't care if the RDAC register is read from or written to). Data is loaded MSB first (Bit 15). The four control bits determine the function of the software command as listed in Table 11. Figure 3 shows a timing diagram of a typical AD5270/AD5271 write sequence.

The write sequence begins by bringing the $\overline{SYNC}$ line low. The $\overline{SYNC}$ pin must be held low until the complete data-word is loaded from the DIN pin. When $\overline{SYNC}$ returns high, the serial data-word is decoded according to the instructions in Table 11. The command bits (Cx) control the operation of the digital potentiometer. The data bits (Dx) are the values that are loaded into the decoded register. The AD5270/AD5271 have an internal counter that counts a multiple of 16 bits (a frame) for proper operation. For example, AD5270/AD5271 each works with a 32-bit word but do not work properly with a 31-bit or 33-bit word. The AD5270/AD5271 do not require a continuous SCLK when $\overline{SYNC}$ is high. To minimize power consumption in the digital input buffers, operate all serial interface pins close to the V_{DD} supply rails.

RDAC REGISTER

The RDAC register directly controls the position of the digital rheostat wiper. For example, when the RDAC register is loaded with all zeros, the wiper is connected to Terminal A of the variable resistor. The RDAC register is a standard logic register and there is no restriction on the number of changes allowed. The basic mode of setting the variable resistor wiper position (programming the RDAC register) is accomplished by loading the serial data input register with Command 1 (see Table 11) and with the desired wiper position data.

50-TP MEMORY BLOCK

The AD5270/AD5271 contain an array of 50-TP programmable memory registers, which allow the wiper position to be programmed up to 50 times. Table 13 shows the memory map. When the desired wiper position is determined, the user can load the serial data input register with Command 3 (see Table 11) which stores the wiper position data in a 50-TP memory register. The first address to be programmed is Location 0x01 (see Table 13); the AD5270/AD5271 increments the 50-TP memory address for each subsequent program until the memory is full. Programming data to 50-TP consumes approximately 4 mA for 55 ms, and takes approximately 350 ms to complete, during which time the shift register locks to prevent any changes from occurring. Bit C3 of the control register can be polled to verify that the fuse program command was completed properly. No change in supply voltage is required to program the 50-TP memory; however, a 1 µF capacitor on the EXT_CAP pin is required (see Figure 46). Prior to 50-TP activation, the AD5270 and the AD5271 preset to midscale on power up.

WRITE PROTECTION

At power-up, the serial data input register write commands for both the RDAC register and the 50-TP memory registers are disabled. The RDAC write protect bit, C1, of the control register (see Table 13 and Table 14) is set to 0 by default. This disables any change of the RDAC register content regardless of the software commands, except that the RDAC register can be refreshed from the 50-TP memory using the software reset, Command 4. To enable programming of the RDAC register, the write protect bit (Bit C1), of the control register must first be programmed by loading the serial data input register with Command 7. To enable programming of the 50-TP memory, the program enable bit (Bit C0) of the control register, which is set to 0 by default, must first be set to 1.

RDAC AND 50-TP READ OPERATION

A serial data output SDO pin is available for readback of the internal RDAC register or 50-TP memory contents. The contents of the RDAC register can be read back through SDO by using Command 2 (see Table 11). Data from the RDAC register is clocked out of the SDO pin during the last 10 clocks of the next SPI operation.

It is possible to read back the contents of any of the 50-TP memory registers through SDO by using Command 5. The lower six LSB bits, D0 to D5 of the data byte, select which memory location is to be read back, as shown in Table 13.

Data from the selected memory location is clocked out of the SDO pin during the next SPI operation. A binary encoded version address of the most recently programmed wiper memory location can be read back using Command 6 (see Table 11). This can be used to monitor the spare memory status of the 50-TP memory block.

Table 12 provides a sample listing for the sequence of serial data input (DIN) words with the serial data output appearing at the SDO pin in hexadecimal format for a write and read to both the RDAC register and the 50-TP memory (Memory Location 20).

Table 11. Command Operation Truth Table

Command Number	Command[DB13:DB10]				Data[DB9:DB0][1]										
	C3	C2	C1	C0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Operation
0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	NOP: do nothing.
1	0	0	0	1	D9	D8	D7	D6	D5	D4	D3	D2	D1[2]	D0[2]	Write contents of serial register data to RDAC.
2	0	0	1	0	X	X	X	X	X	X	X	X	X	X	Read contents of RDAC wiper register.
3	0	0	1	1	X	X	X	X	X	X	X	X	X	X	Store wiper setting: store RDAC setting to 50-TP.
4	0	1	0	0	X	X	X	X	X	X	X	X	X	X	Software reset: refresh RDAC with last 50-TP memory stored value.
5[3]	0	1	0	1	X	X	X	X	D5	D4	D3	D2	D1	D0	Read contents of 50-TP from SDO output in the next frame.
6	0	1	1	0	X	X	X	X	X	X	X	X	X	X	Read address of last 50-TP programmed memory location.
7[4]	0	1	1	1	X	X	X	X	X	X	X	D2	D1	D0	Write contents of serial register data to control register.
8	1	0	0	0	X	X	X	X	X	X	X	X	X	X	Read contents of control register.
9	1	0	0	1	X	X	X	X	X	X	X	X	X	D0	Software shutdown. D0 = 0; normal mode. D0 = 1; device placed in shutdown mode.

[1] X is don't care.
[2] AD5271 = don't care.
[3] See Table 15 for 50-TP memory map.
[4] See Table 14 for bit details.

SHUT-DOWN MODE

The AD5270/AD5271 can be shut down by executing the software shutdown command, Command 9 (see Table 11), and setting the LSB to 1. This feature places the RDAC in a zero-power-consumption state where Terminal Ax is open circuited and the Wiper Terminal Wx remains connected. It is possible to execute any command from Table 11 while the AD5270/AD5271 are in shutdown mode. The parts can be taken out of shutdown mode by executing Command 9 and setting the LSB to 0 or by a software reset, Command 4 (see Table 11).

RESISTOR PERFORMANCE MODE

This mode activates a new, patented 1% end-to-end resistor tolerance that ensures a ±1% resistor tolerance error on each code, that is, code = half scale, R_{WA} = 10 kΩ ± 100 Ω. See Table 2, Table 3, Table 5, and Table 6 to verify which codes achieve ±1% resistor tolerance. The resistor performance mode is activated by programming Bit C2 of the control register.

RESET

The AD5270/AD5271 can be reset through software by executing Command 4 (see Table 11). The reset command loads the RDAC register with the contents of the most recently programmed 50-TP memory location. The RDAC register loads with midscale if no 50-TP memory location has been previously programmed.

Table 12. Write and Read to RDAC and 50-TP Memory

DIN	SDO[1]	Action
0x1C03	0xXXXX	Enable update of the wiper position and the 50-TP memory contents through the digital interface.
0x0500	0x1C03	Write 0x100 to the RDAC register; wiper moves to ¼ full-scale position.
0x0800	0x0500	Prepares data read from RDAC register.
0x0C00	0x100	Stores RDAC register content into the 50-TP memory. A 16-bit word appears out of SDO, where the last 10-bits contain the contents of the RDAC register (0x100).
0x1800	0x0C00	Prepares data read of last programmed 50-TP memory monitor location.
0x0000	0xXX19	NOP Instruction 0 sends a 16-bit word out of SDO, where the six LSBs last six bits contain the binary address of the last programmed 50-TP memory location, for example, 0x19 (see Table 13).
0x1419	0x0000	Prepares data read from Memory Location 0x19.
0x2000	0x0100	Prepares data read from the control register. Sends a 16-bit word out of SDO, where the last 10-bits contain the contents of Memory Location 0x19.
0x0000	0xXXXX	NOP Instruction 0 sends a 16-bit word out of SDO, where the last four bits contain the contents of the control register. If Bit C3 = 1, the fuse program command successful.

[1] X is don't care.

Table 13. Control Register Bit Map

DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	C3	C2	C1	C0

Table 14. Control Register Bit Description

Bit Name	Description
C0	50-TP program enable 0 = 50-TP program disabled (default) 1 = enable device for 50-TP program
C1	RDAC register write protect 0 = wiper position frozen to value in 50-TP memory (default)[1] 1 = allow update of wiper position through digital interface
C2	R-performance enable 0 = RDAC resistor tolerance calibration enabled (default) 1 = RDAC resistor tolerance calibration disabled
C3	50-TP memory program success bit 0 = fuse program command unsuccessful (default) 1 = fuse program command successful

[1] Wiper position frozen to the last value programmed in the 50-TP memory. The wiper is frozen to midscale if the 50-TP memory has not been previously programmed.

Table 15. Memory Map

Command Number	Data Byte[DB9:DB8][1]										Register Contents
	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
5	X	X	X	0	0	0	0	0	0	0	Reserved
	X	X	X	0	0	0	0	0	0	1	1st programmed wiper location (0x01)
	X	X	X	0	0	0	0	0	1	0	2nd programmed wiper location (0x02)
	X	X	X	0	0	0	0	0	1	1	3rd programmed wiper location (0x03)
	X	X	X	0	0	0	0	1	0	0	4th programmed wiper location (0x04)
	…	…	…	…	…	…	…	…	…	…	…
	X	X	X	0	0	0	1	0	1	0	10th programmed wiper location (0xA)
	X	X	X	0	0	1	0	1	0	0	20th programmed wiper location (0x14)
	X	X	X	0	0	1	1	1	1	0	30th programmed wiper location (0x1E)
	X	X	X	0	1	0	1	0	0	0	40th programmed wiper location (0x28)
	X	X	X	0	1	1	0	0	1	0	50th programmed wiper location (0x32)

[1] X is don't care.

SDO PIN AND DAISY-CHAIN OPERATION

The serial data output pin (SDO) serves two purposes: it can be used to read the contents of the wiper setting and 50-TP values using Command 2 and Command 5, respectively (see Table 11), or the SDO pin can be used in daisy-chain mode. Data is clocked out of SDO on the rising edge of SCLK. The SDO pin contains an open-drain N-channel FET that requires a pull-up resistor. To place the pin in high impedance and mini-mize the power dissipation when the pin is used, the 0x8001 data word followed by Command 0 should be sent to the part. Table 16 provides a sample listing for the sequence of the serial data input (DIN). Daisy chaining minimizes the number of port pins required from the controlling IC. As shown in Figure 44, the user must tie the SDO pin of one package to the DIN pin of the next package. The user may need to increase the clock period because the pull-up resistor and the capacitive loading at the SDO-to-DIN interface may require additional time delay between subsequent devices. When two AD5270/AD5271 devices are daisy-chained, 32 bits of data are required. The first 16 bits go to U2, and the second 16 bits go to U1.

Table 16. Minimize Power Dissipation at the SDO Pin

DIN	SDO[1]	Action
0xXXXX	0xXXXX	Last user command sent to the digipot.
0x8001	0xXXXX	Prepares the SDO pin to be placed in high impedance mode.
0x0000	High Impedance	The SDO pin is placed in high impedance.

[1] X is don't care.

Keep the $\overline{\text{SYNC}}$ pin low until all 32 bits are clocked to their respective serial registers. The $\overline{\text{SYNC}}$ pin is then pulled high to complete the operation.

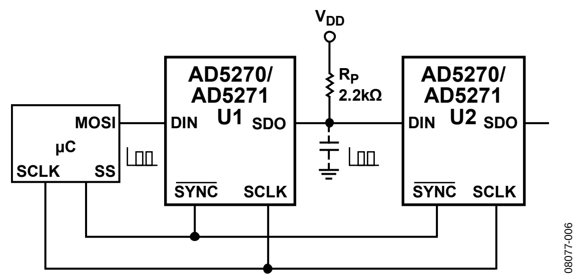


Figure 44. Daisy-Chain Configuration Using SDO

RDAC ARCHITECTURE

To achieve optimum performance, Analog Devices has patented the RDAC segmentation architecture for all the digital potentio-meters. In particular, the AD5270/AD5271 employ a three-stage segmentation approach as shown in Figure 45.The AD5270/ AD5271 wiper switch is designed with the transmission gate CMOS topology.

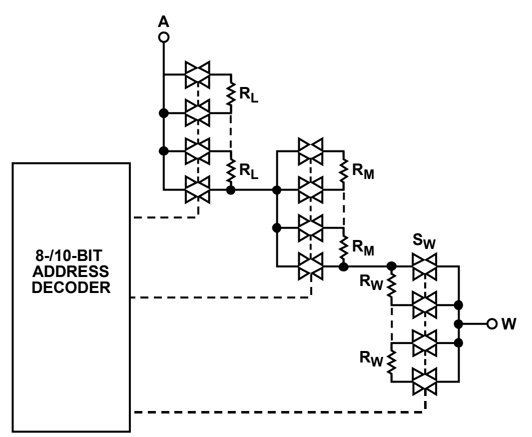


Figure 45. Simplified RDAC Circuit

PROGRAMMING THE VARIABLE RESISTOR

Rheostat Operation—1% Resistor Tolerance

The nominal resistance between Terminal W and Terminal A, R_{WA}, is 20 kΩ, 50 kΩ, or 100 kΩ and has 1024-/256-tap points accessed by the wiper terminal. The 10-/8-bit data in the RDAC latch is decoded to select one of the 1024 or 256 possible wiper settings. The AD5270 and AD5271 contain an internal ±1% resistor tolerance calibration feature that can be disabled or enabled, enabled by default, or by programming Bit C2 of the control register (see Table 13 and Table 14).

The digitally programmed output resistance between the W terminal and the A terminal, R_{WA}, is calibrated to give a maximum of ±1% absolute resistance error over both the full supply and temperature ranges. As a result, the general equations for determining the digitally programmed output resistance between the W terminal and the A terminal are the following:

For the AD5270

$$R_{WA}(D) = \frac{D}{1024} \times R_{WA} \quad (1)$$

For the AD5271

$$R_{WA}(D) = \frac{D}{256} \times R_{WA} \quad (2)$$

where:
D is the decimal equivalent of the binary code loaded in the 10-/8-bit RDAC register.
R_{WA} is the end-to-end resistance.

In the zero-scale condition, a finite total wiper resistance of 120 Ω is present. Regardless of which setting the part is operating in, take care to limit the current between Terminal A to Terminal W to the maximum continuous current of ±3 mA or a pulse current specified in Table 8. Otherwise, degradation or possible destruction of the internal switch contact can occur.

EXT_CAP CAPACITOR

A 1 µF capacitor to V_{SS} must be connected to the EXT_CAP pin, as shown in Figure 46, on power-up and throughout the operation of the AD5270/AD5271.

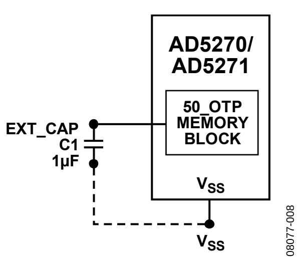


Figure 46. EXT_CAP Hardware Setup

TERMINAL VOLTAGE OPERATING RANGE

The positive V_{DD} and negative V_{SS} power supplies of the AD5270/AD5271 define the boundary conditions for proper 2-terminal digital resistor operation. Supply signals present on Terminal A and Terminal W that exceed V_{DD} or V_{SS} are clamped by the internal forward-biased diodes, see Figure 47.

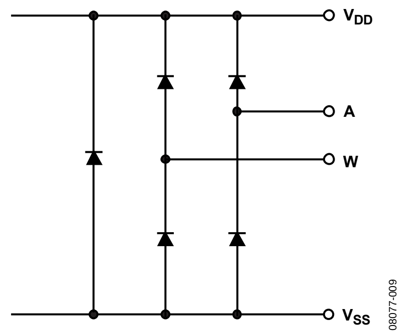


Figure 47. Maximum Terminal Voltages Set by V_{DD} and V_{SS}

The ground pins of the AD5270/AD5271 devices are primarily used as digital ground references. To minimize the digital ground bounce, join the AD5270/AD5271 ground terminal remotely to the common ground. The digital input control signals to the AD5270/AD5271 must be referenced to the device ground pin (GND), and must satisfy the logic level defined in the Specifications section. An internal level shift circuit ensures that the common-mode voltage range of the three terminals extends from V_{SS} to V_{DD}, regardless of the digital input level.

POWER-UP SEQUENCE

Because there are diodes to limit the voltage compliance at Terminal A and Terminal W (see Figure 47), it is important to power V_{DD}/V_{SS} first before applying any voltage to Terminal A and Terminal W; otherwise, the diode is forward-biased such that V_{DD}/V_{SS} are powered unintentionally. The ideal power-up sequence is V_{SS}, GND, V_{DD}, digital inputs, V_A, and V_W. The order of powering V_A, V_W, and the digital inputs is not important as long as they are powered after V_{DD}/V_{SS}.

As soon as V_{DD} is powered, the power-on preset activates which first sets the RDAC to midscale and then restores the last programmed 50-TP value to the RDAC register.

OUTLINE DIMENSIONS

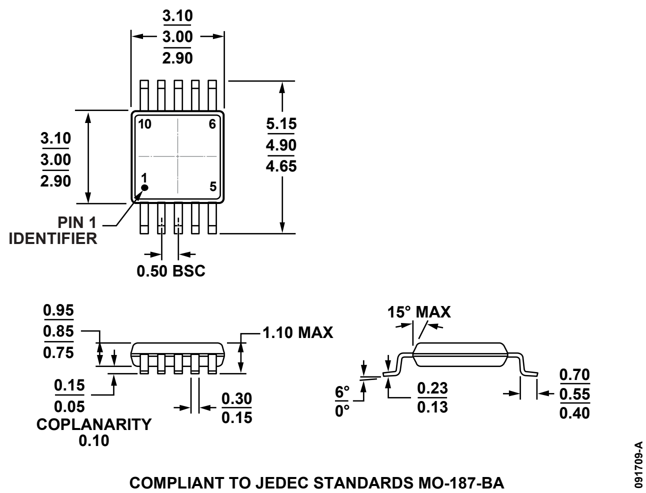


Figure 48. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

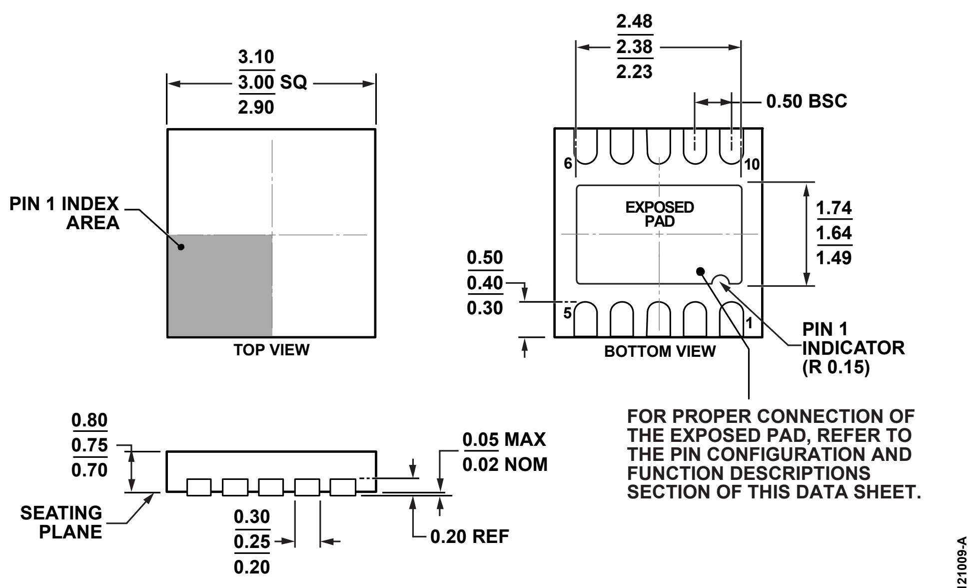


Figure 49. 10-Lead Frame Chip Scale Package [LFCSP_WD]
3 mm × 3 mm Body, Very Thin, Dual Lead
(CP-10-9)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	R_{AW} (kΩ)	Resolution	Temperature Range	Package Description	Package Option	Branding
AD5270BRMZ-20	20	1,024	−40°C to +125°C	10-Lead MSOP	RM-10	D1X
AD5270BRMZ-20-RL7	20	1,024	−40°C to +125°C	10-Lead MSOP	RM-10	D1X
AD5270BRMZ-50	50	1,024	−40°C to +125°C	10-Lead MSOP	RM-10	DDP
AD5270BRMZ-50-RL7	50	1,024	−40°C to +125°C	10-Lead MSOP	RM-10	DDP
AD5270BRMZ-100	100	1,024	−40°C to +125°C	10-Lead MSOP	RM-10	D1W
AD5270BRMZ-100-RL7	100	1,024	−40°C to +125°C	10-Lead MSOP	RM-10	D1W
AD5270BCPZ-20-RL7	20	1,024	−40°C to +125°C	10-Lead LFCSP_WD	CP-10-9	DDY
AD5270BCPZ-100-RL7	100	1,024	−40°C to +125°C	10-Lead LFCSP_WD	CP-10-9	DDX
AD5271BRMZ-20	20	256	−40°C to +125°C	10-Lead MSOP	RM-10	DE0
AD5271BRMZ-20-RL7	20	256	−40°C to +125°C	10-Lead MSOP	RM-10	DE0
AD5271BRMZ-100	100	256	−40°C to +125°C	10-Lead MSOP	RM-10	DDZ
AD5271BRMZ-100-RL7	100	256	−40°C to +125°C	10-Lead MSOP	RM-10	DDZ
AD5271BCPZ-20-RL7	20	256	−40°C to +125°C	10-Lead LFCSP_WD	CP-10-9	DE2
AD5271BCPZ-100-RL7	100	256	−40°C to +125°C	10-Lead LFCSP_WD	CP-10-9	DE1
EVAL-AD5270SDZ				Evaluation Board		

[1] Z = RoHS Compliant Part.

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