XRD64L15

3.3V CMOS 10-Bit, 20 MSPS, High Speed Analog-to-Digital Converter

March 1998-3

FEATURES

- 10-Bit Resolution
- 20MHz Sampling Rate
- Internal S/H Function
- Single 3V Power Supply
- V_{IN} DC Range: 0V to V_{DD}
- V_{REF} DC Range: 1V to V_{DD}
- Low Power: 80mW (typ)
- Three-State Digital Outputs
- Power Down: 1.0mW (typ) Power Dissipation
- ESD Protection: 2000V Minimum
- For 5V Operation Refer to XRD6415

APPLICATIONS

- Digital Camcorders
- Digital Cameras
- Precision Scanners
- Medical Imaging
- Digital Color Copiers
- IR Imaging
- Digital Communications

BENEFITS

- Complete Analog-to-Digital Converter (ADC) That Requires No External Active Components
- Small Outline Package to Reduce Board Space
- Low Power Dissipation
- Easy to Use Rugged Design

GENERAL DESCRIPTION

The XRD64L15 is a 10-bit, 20MSPS, Analog-to-Digital Converter (ADC) for applications that require high speed and high accuracy. Designed using an advanced CMOS process, this part offers excellent performance, low power consumption and latch-up free operation.

The XRD64L15 uses a subranging architecture to maintain low power consumption at high conversion rates. Our proprietary comparator design achieves a low analog input capacitance. The input circuitry of the XRD64L15 includes an on-chip S/H function that allows the product to digitize analog input signals between GND and V_{DD}. The XRD64L15 can be placed into power down (stand-by) mode, reducing the power dissipation to 1.0mW (typical) by a digitally controlled pin.

Providing external reference voltages allows easy interface to any input signal range between GND and V_{DD}. This also allows the system to calibrate out zero scale and full scale errors by adjusting V_{RT} and V_{RB}. The Reference Ladder tap (VR2) can be used to externally trim INL errors.

This device operates from a single 3.3V supply. Power consumption from a 3.3V supply is typically 80mW at F_S=15MHz. For 5V supply operation refer to XRD6415.

Part No.	Package	Operating Temperature Range
XRD64L15AIP	28 Lead 300 Mil PDIP	--40°C to +85°C
XRD64L15AID	28 Lead 300 Mil JEDEC SOIC	--40°C to +85°C
XRD64L15AIU	28 Lead SSOP (5.3 mm)	--40°C to +85°C
XRD64L15AIQ	32 Lead TQFP (7 x 7 x 1.4 mm)	--40°C to +85°C
XRD64L15AIV	48 Lead TQFP (7 x 7 x 1.0 mm)	--40°C to +85°C

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SIMPLIFIED BLOCK DIAGRAM

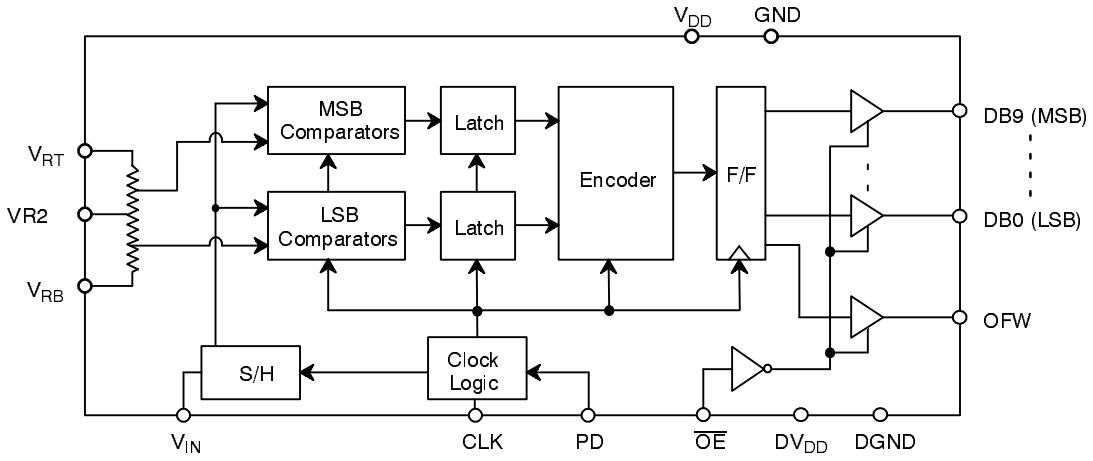
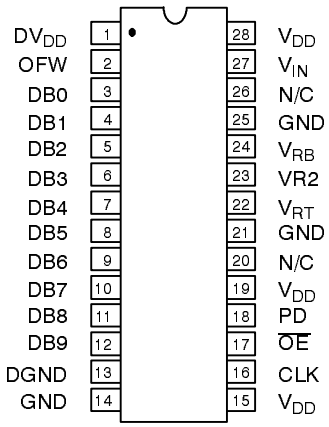
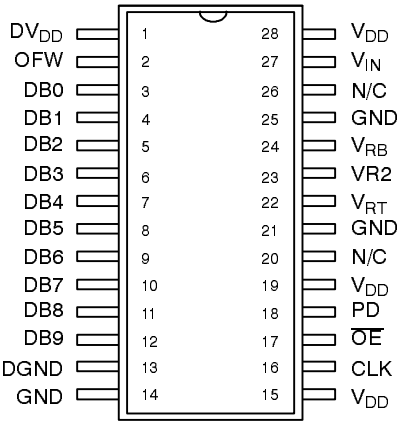


Figure 1. Block Diagram

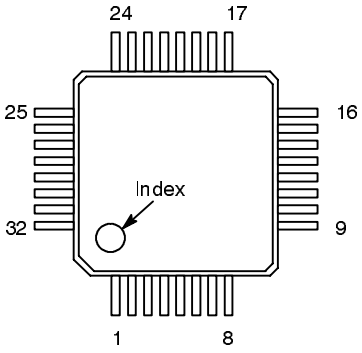
PIN CONFIGURATIONS



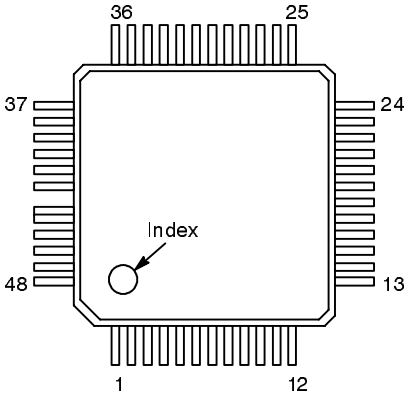
28 Lead PDIP (0.300")



28 Lead SOIC (Jedec, 0.300")
28 Lead SSOP (5.3 mm)



32 Lead TQFP (7 x 7 x 1.4 mm)



48 Lead TQFP (7 x 7 x 1.0 mm)

PIN DESCRIPTION (28 Lead PDIP, SOIC & SSOP Packages)

Pin #	Symbol	Description
1	DV_{DD}	Power Supply (Digital Outputs)
2	OFW	Overflow Output
3	DB0	Data Output Bit 0 (LSB)
4	DB1	Data Output Bit 1
5	DB2	Data Output Bit 2
6	DB3	Data Output Bit 3
7	DB4	Data Output Bit 4
8	DB5	Data Output Bit 5
9	DB6	Data Output Bit 6
10	DB7	Data Output Bit 7
11	DB8	Data Output Bit 8
12	DB9	Data Output Bit 9 (MSB)
13	DGND	Ground (Digital Outputs)
14	GND	Ground
15	V_{DD}	Power Supply
16	CLK	Sampling Clock Input
17	$\overline{OE}$	Output Enable Control
18	PD	Power Down Control
19	V_{DD}	Power Supply
20	N/C	No Connection
21	GND	Ground
22	V_{RT}	Top of Reference Ladder
23	VR2	Center of Reference Ladder
24	V_{RB}	Bottom of Reference Ladder
25	GND	Ground
26	N/C	No Connection
27	V_{IN}	Analog Input Voltage
28	V_{DD}	Power Supply

PIN DESCRIPTION (32 Lead Plastic QFP Package)

Pin #	Symbol	Description
1	DB9	Data Output Bit 9 (MSB)
2	DGND	Ground (Output)
3	GND	Ground
4	GND	Ground
5	GND	Ground
6	V_{DD}	Power Supply
7	CLK	Sampling Clock Input
8	$\overline{OE}$	Output Enable Control
9	PD	Power Down Control
10	V_{DD}	Power Supply
11	GND	Ground
12	V_{RT}	Top of Reference Ladder
13	V_{RB}	Bottom of Reference Ladder
14	GND	Ground
15	GND	Ground
16	GND	Ground
17	GND	Ground
18	GND	Ground
19	GND	Ground
20	V_{IN}	Analog Input Voltage to ADC
21	V_{DD}	Power Supply
22	DV_{DD}	Power Supply (Output)
23	OFW	Overflow Output
24	DB0	Data Output Bit 0 (LSB)
25	DB1	Data Output Bit 1
26	DB2	Data Output Bit 2
27	DB3	Data Output Bit 3
28	DB4	Data Output Bit 4
29	DB5	Data Output Bit 5
30	DB6	Data Output Bit 6
31	DB7	Data Output Bit 7
32	DB8	Data Output Bit 8

PIN DESCRIPTION (48 Lead TQFP Package)

Pin #	Symbol	Description
1	DB0	Digital Output Bit 0 (LSB)
2	DB1	Digital Output Bit 1
3	DB2	Digital Output Bit 2
4	DB3	Digital Output Bit 3
5	DB4	Digital Output Bit 4
6	N/C	No Connection
7	N/C	No Connection
8	DB5	Digital Output Bit 5
9	DB6	Digital Output Bit 6
10	DB7	Digital Output Bit 7
11	DB8	Digital Output Bit 8
12	DB9	Digital Output Bit 9 (MSB)
13	DGND	Ground (Digital Outputs)
14	N/C	No Connection
15	N/C	No Connection
16	GND	Ground
17	N/C	No Connection
18	N/C	No Connection
19	V_{DD}	Power Supply
20	N/C	No Connection
21	N/C	No Connection
22	CLK	Sample Clock
23	$\overline{OE}$	Output Enable (3-State Cntl)
24	PD	Power Down Control
25	N/C	No Connection
26	V_{DD}	Power Supply
27	N/C	No Connection
28	GND	Ground
29	N/C	No Connection
30	V_{RT}	Top of Reference Ladder
31	N/C	No Connection
32	VR2	Center of Reference Ladder
33	N/C	No Connection
34	V_{RB}	Bottom of Reference Ladder
35	N/C	No Connection
36	GND	Ground
37	N/C	No Connection
38	N/C	No Connection

PIN DESCRIPTION (48 Lead TQFP Package) (CONT'D)

Pin #	Symbol	Description
39	V_{IN}	Analog Input Voltage
40	N/C	No Connection
41	N/C	No Connection
42	V_{DD}	Power Supply
43	N/C	No Connection
44	N/C	No Connection
45	DV_{DD}	Power Supply (Digital Outputs)
46	N/C	No Connection
47	N/C	No Connection
48	N/C	No Connection

ELECTRICAL CHARACTERISTICS TABLE

Test Conditions: V_{DD} = DV_{DD} = 3.3V, F_S = 15 MHz (50% Duty Cycle), V_{RT} = 2.5V, V_{RB} = 0.5V, T_A = 25°C Unless Otherwise Specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Key Features						
n	Resolution	10			Bits	
F_S	Maximum Sample Rate	15	20		MSPS	
DC Accuracy[1]						
DNL	Differential Non-Linearity	--0.8	±0.5	1.0	LSB	
INL	Integral Non-Linearity	--2.5	1.5	2.5	LSB	Best Fit Line (Max INL -- Min INL)/2
EZS	Zero Scale Error		±20		mV	
EFS	Full Scale Error	--1.0	±0.4	1.0	% FS	
V_{INPP}	DC Input Range	GND		V_{DD}	V	V_{IN} can swing from GND to V_{DD}, actual digitized range is set by V_{RT} & V_{RB}.
Reference Voltages						
V_{RT}	Top Reference Voltage[2]	1.0	2.5	V_{DD}	V	
V_{RB}	Bottom Reference Voltage[2]	GND	0.5	V_{DD}-1	V	
V_{REF}	Differential Ref. Voltage[2]	1.0	2	V_{DD}	V	
R_L	Ladder Resistance	350	500	650	Ω	
Analog Input[3]						
	Input Voltage Range	V_{RB}		V_{RT}	V	V_{RB} Min. = GND V_{RT} Max = V_{DD}
BW	Input Bandwidth (--1 dB)[4]		50		MHz	
C_{IN}	Input Capacitance Sample[5]		20		pF	CLK = Low
C_{IN}	Input Capacitance Convert[5]		7		pF	CLK = High
Conversion Character						
t_{AP}	Aperture Delay		6		ns	
t_{AJ}	Aperture Jitter		30		ps	
Dynamic						
	Signal-to-Noise Ratio (SNR)					
	F_{IN} = 1 MHz		58		dB	F_S = 10MSPS
	SNR and Distortion (SNDR)					
	F_{IN} = 1 MHz		57		dB	F_S = 10MSPS
Digital Inputs						
V_{IH}	Digital Input High Voltage	2.5			V	
V_{IL}	Digital Input Low Voltage			0.5	V	
I_{IN}	DC Leakage Currents[6]					
	CLK, $\overline{OE}$, and PD		5		µA	CLK, $\overline{OE}$ and PD between GND and V_{DD}
	Input Capacitance		5		pF	

ELECTRICAL CHARACTERISTICS TABLE (CONT'D)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Digital Outputs						C_{OUT}=15pF
V_{OH}	Output High Voltage	2.5			V	While Sourcing 1mA
V_{OL}	Output Low Voltage			0.4	V	While Sinking 1mA
I_{OZ}	High-Z Leakage	--10		10	µA	OE = High, or PD = High
t_{DL}	Data Valid Delay[3]	10	12	13	ns	
t_{DEN}	Data Enable Delay[3]	10	12	14	ns	
t_{DHZ}	Data High-Z Delay[3]	7	8	9	ns	
	Pipeline Delay (Latency)		3		cycles	Time Delay between CLK and Data Output Constant
Power Supplies						
I_{DD}(PD)	Power Down (I_{DD})		0.3	0.5	mA	
V_{DD}	Operating Voltage[7,8]	2.7	3.3	3.6	V	
DV_{DD}	Logic Power Supply[9]	2.7	3.3	V_{DD}	V	
I_{DD}	Supply Current		24	32	mA	

Notes

1 *Tester measures code transitions by dithering the voltage of the analog input (V_{IN}). The difference between the measured and the ideal code width (V_{REF}/1024) is the DNL error. The INL error is the maximum distance (in LSBs) from the best fit line to any transition voltage. Accuracy is a function of the sampling rate (FS).*

2 *Specified values guarantee functionality. Refer to other parameters for accuracy.*

3 *Guaranteed. Not tested.*

4 *–1 dB bandwidth is a measure of performance of the A/D input stage (S/H + amplifier). Refer to other parameters for accuracy within the specified bandwidth.*

5 *See V_{IN} equivalent circuit. Switched capacitor analog input requires driver with low output resistance.*

6 *All inputs have diodes to V_{DD} and GND. Input DC currents will not exceed specified limits for any input voltage between GND and V_{DD}.*

7 *The GND pins are connected through the silicon substrate. Connect all GND pins together at the package and to the analog ground plane. DGND and GND are connected through junction diodes. See logic output interface section.*

8 *The V_{DD} pins should be tied together at the package.*

9 *See logic output interface section.*

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} to GND . . . . . +7.0V
V_{RT} & V_{RB} . . . . . V_{DD} +0.5 to GND –0.5V
V_{IN} . . . . . V_{DD} +0.5 to GND –0.5V
All Inputs . . . . . V_{DD} +0.5 to GND –0.5V
All Outputs . . . . . V_{DD} +0.5 to GND –0.5V

Storage Temperature . . . . . –65 to +150°C
Package Power Dissipation Rating to 75°C
PDIP, SOIC, TQFP, SSOP 1000mW
Derates above 75°C . . . . . 14mW/°C
Lead Temperature (Soldering 10 seconds) . . +300°C

Notes

1 *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.*

2 *Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. All inputs have protection diodes which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.*

3 *V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.*

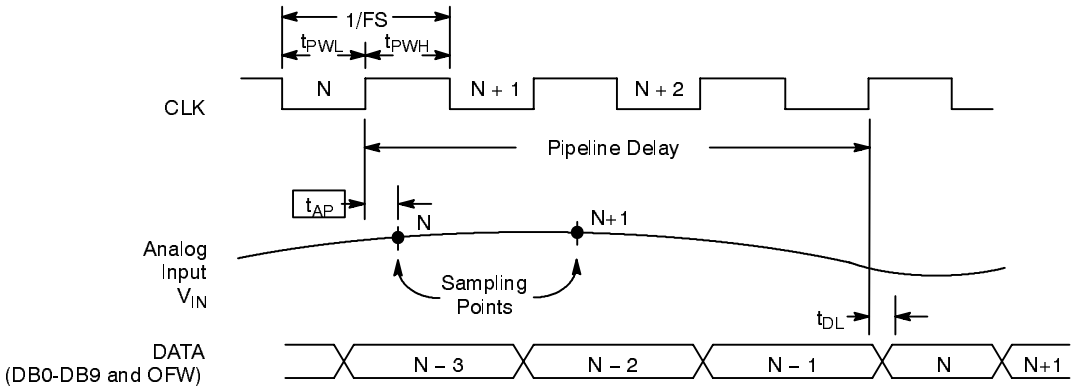


Figure 2. XRD64L15 Timing Diagram

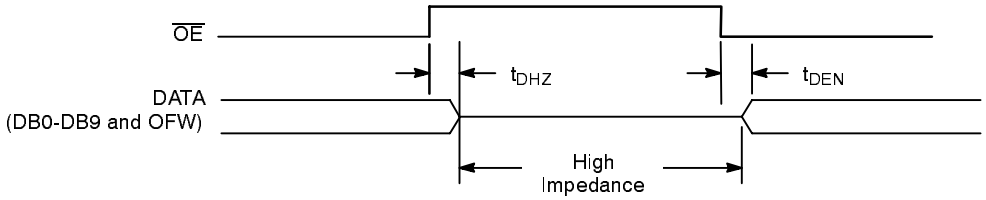


Figure 3. Three-State Timing Diagram

THEORY OF OPERATION

V_{IN} Analog Input

This part has a switched capacitor, sampling input circuit. The input impedance changes with the phase of the input clock. V_{IN} is sampled on the low to high clock transition and the digital data updates on the low to high clock transition. The diagram *Figure 4.* shows an equivalent input circuit.

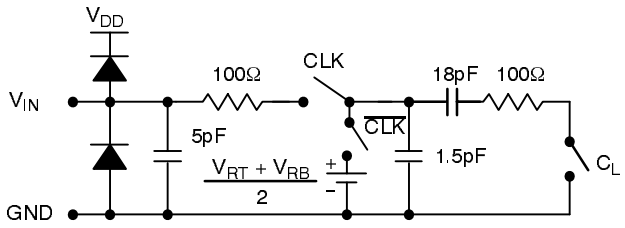


Figure 4. Equivalent Input Circuit

OFW Overflow (Output)

This signal indicates when the Analog Input (V_{IN}) goes above V_{RT}. The pin is normally at a low logic level. When $V_{IN} > V_{RT}$, OFW will go high and the data bits (DB0 – DB9) will show full scale (i.e., all 1s).

$\overline{OE}$ Output Enable (Input)

This signal controls the 3-state drivers on the digital outputs DB0 – DB9 and OFW. During normal operation, $\overline{OE}$ should be held low, so that all outputs are enabled. When $\overline{OE}$ is driven high DB0 – DB9 and OFW go into high impedance mode. This control operates asynchronous to the clock and will only control the output drivers. The internal output register will get updated if the clock is running while the outputs are in three-state mode.

$\overline{OE}$	DBO-DB9	OFW
0	Enabled	Enabled
1	High-Z	High-Z

Table 1. Output Enable

Logic Output Interface

The digital output drive circuitry of the XRD64L15 was designed to operate separately from the analog supplies. The DV_{DD} pin of the XRD64L15 is a separate power supply dedicated to the logic output drivers. DV_{DD} is not connected internally with any of the other power supplies. *Figure 5.* illustrates the power supply circuitry of the XRD64L15.

DV_{DD} and DGND connect directly to the digital logic power of the user's system isolating the analog and digital power supplies and grounds. DGND is not common to the XRD64L15 substrate. The XRD64L15 substrate is common only to the packages' GND pins.

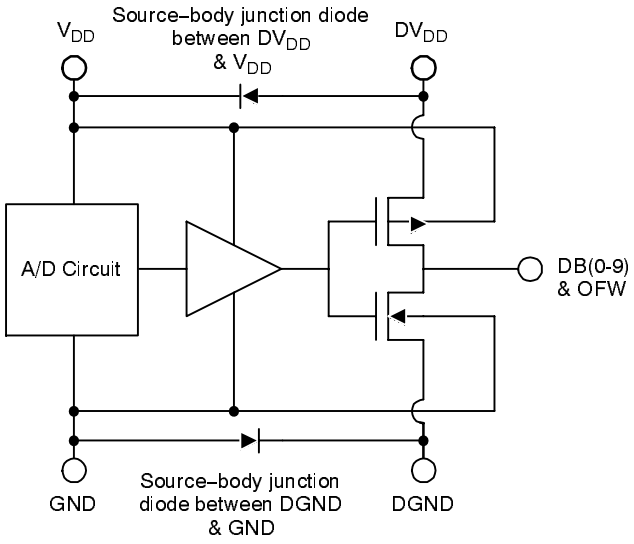


Figure 5. XRD64L15 ADC Power Supply Circuit Allows Separate V_{DD} & DV_{DD} and Separate GND & DGND

Power Supply Sequencing

There are no power supply sequencing issues if DV_{DD} and V_{DD} of the XRD64L15 are driven from the same supply. When DV_{DD} and V_{DD} are driven separately, V_{DD} must come up at the same time or before DV_{DD}, and go down at the same time or after DV_{DD}. If the power supply sequencing in this case is not followed, then damage may occur to the product due to current flow through the source-body junction diodes between DV_{DD} and V_{DD}. An external diode (5082-2235) layed out close to the converter from DV_{DD} to V_{DD} prevents damage from occurring when power is cycled incorrectly.

PD	Device Status
High	Off (Not Operating)
Low	On (Operating)

Table 2. Power Down

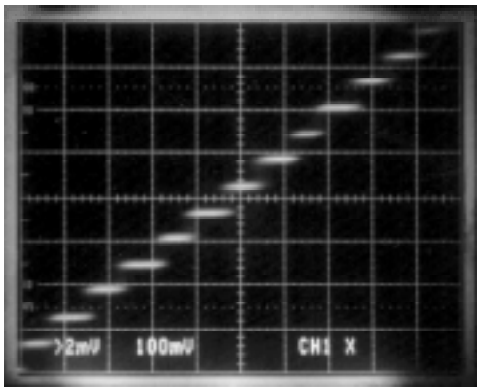


Figure 6. Crossplot Staircase Output CLK = (15MSPS, t_{rf} = 15ns), V_{DD} = 3.3V, V_{REF} = 2V

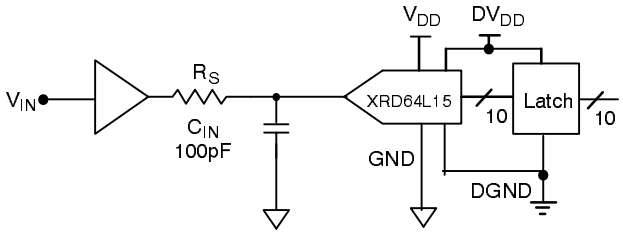


Figure 7. FFT Test Circuit (Refer to XRD64L15 Application Board Note for Details)

FINAL DESIGN CONSIDERATIONS

The XRD64L15 can be evaluated with the XRD6415AB application board. Contact your distributor or sales person for delivery. Using the XRD6415AB the following final design considerations can be made.

1. Be generous with analog and digital ground planes. Mirror the ground plane with the supply planes. Use a 5 mil power / ground plane separation if a four layer board can be used. The XRD64L15 substrate is common to the packages' GND pins only. DGND and DV_{DD} are separate supplies dedicated to the output logic drivers of the XRD64L15. Connect DGND and DV_{DD} to the power planes of the system's digital logic.
2. Keep high frequency decoupling capacitors very close to the A/D pins and minimize the loop area included so less flux will induce less noise. Use decoupling capacitors in the same locations as on the XRD6415AB.
3. Coupling between logic signals and analog circuitry can easily change a 10-bit system into an 8-bit system or worse. Completely separate them. Watch for coupling opportunities from other sources not immediately associated with the A/D. Don't use switching power supplies in adjacent locations, for example.
4. The DC performance of the XRD64L15 is optimized with rise and fall times of CLK edges limited to greater than or equal to 10ns. A resistor in series with the CLK input pin can combine with parasitic capacitance to limit rise and fall times. Select a low jitter clock with a 50% duty cycle for best spectral results.
5. Use support devices equivalent to those used on the evaluation board. Use the application board to verify these devices up front, i.e. use very linear passive components in the signal path.
6. Select a driving op amp whose noise, speed, and linearity fits the application. Use a resistor to decouple the output of the driving op amp from the switching input capacitance of the XRD64L15.
7. DNL and INL performance is optimized when the V_{RB} input of the XRD64L15 is buffered. If V_{RB} is connected to the PCB ground plane it is subject to the noise and ground bounce in that plane. For example V_{RB} could be buffered to 50mV above ground and still have a wide reference voltage range set by connecting V_{RT} to a voltage near V_{DD}.
8. Use 50 or 100Ω resistors to isolate the XRD64L15 digital output pins from a latch or bus connection. This protects the output drivers and reduces the effects of high speed switching logic signals from degrading the ADC performance. Layout the latch or digital buffers as close to the ADC as possible to minimize trace length.

PERFORMANCE CHARACTERISTICS

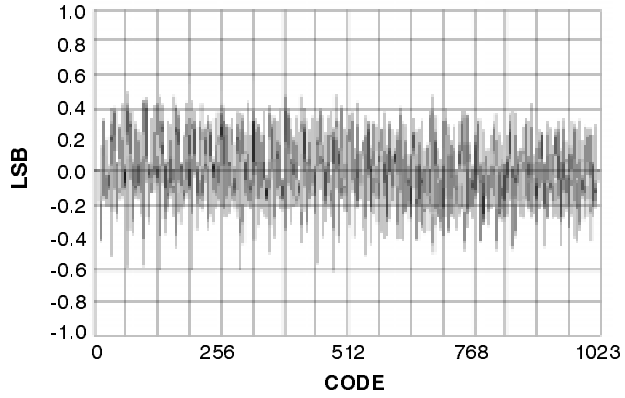


Figure 8. XRD64L15 DNL @ 15MSPS, V_{DD} = 3V, V_{RT}=2.5V, V_{RB} = 0.5V

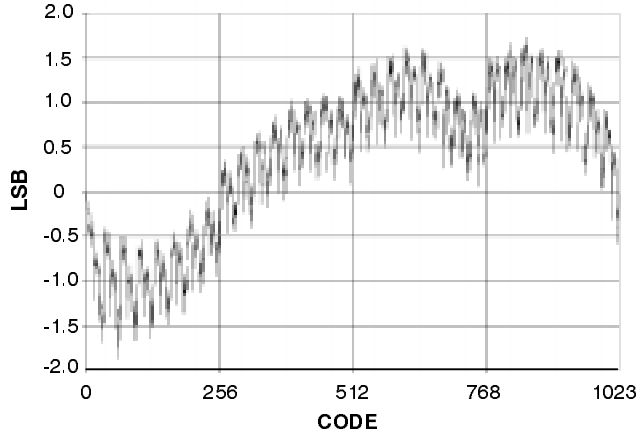


Figure 9. XRD64L15 INL @ 15MSPS, V_{DD} = 3V, V_{RT}=2.5V, V_{RB} = 0.5V

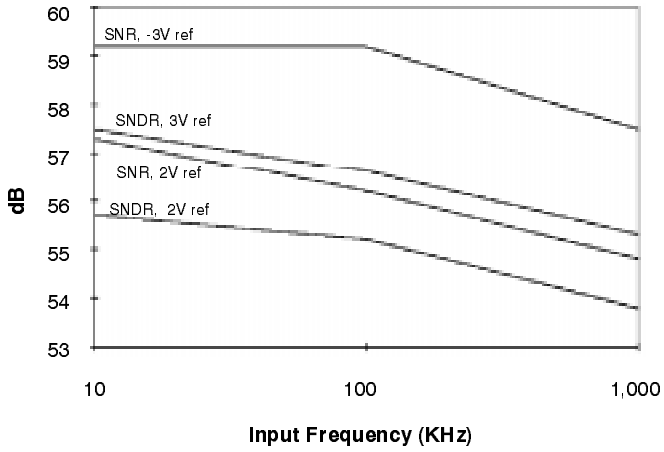


Figure 10. XRD64L15 SNR & SNDR vs. F_{IN}, V_{DD} = 3.3V, DV_{DD} = 3.3V, V_{REF} = 3V & 2V, F_S = 10MSPS, C_{IN} = 100pF

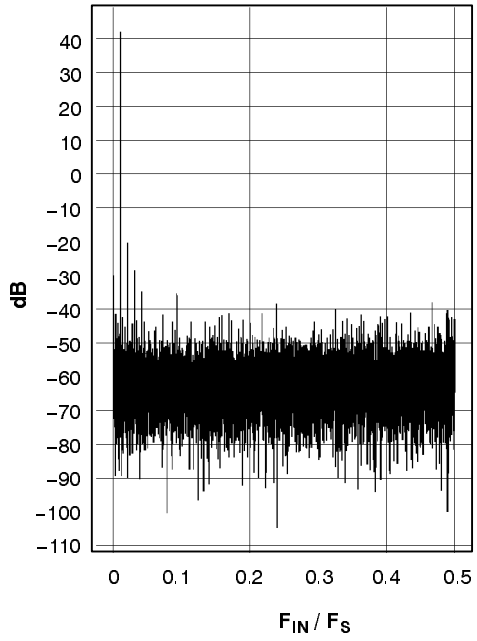


Figure 11. XRD64L15 FFT V_{REF} = V_{DD} = 3.3V, DV_{DD} = 3.3V, F_{IN} = 100kHz, F_S = 10MSPS, C_{IN} = 100pF

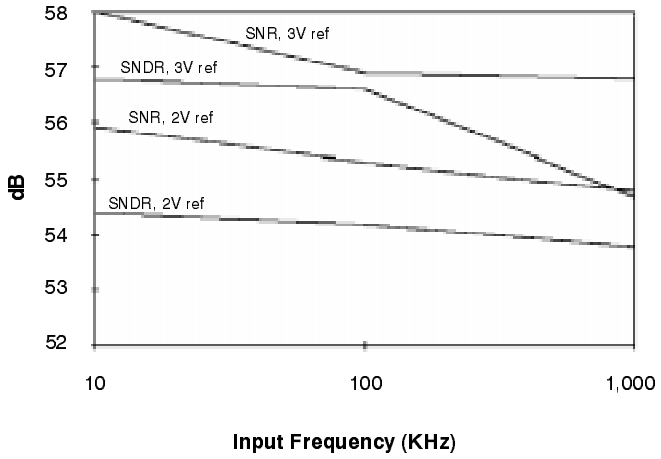


Figure 12. XRD64L15 SNR & SNDR vs. F_{IN}, V_{DD} = 3.3V, DV_{DD} = 3.3V, V_{REF} = 3V & 2V, F_S = 15MSPS, C_{IN} = 100pF

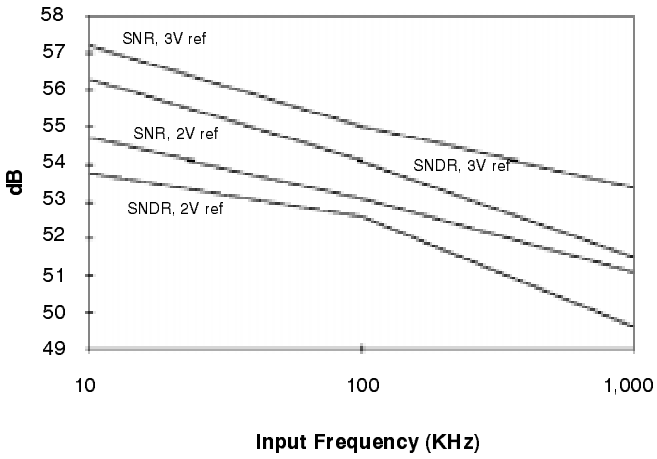
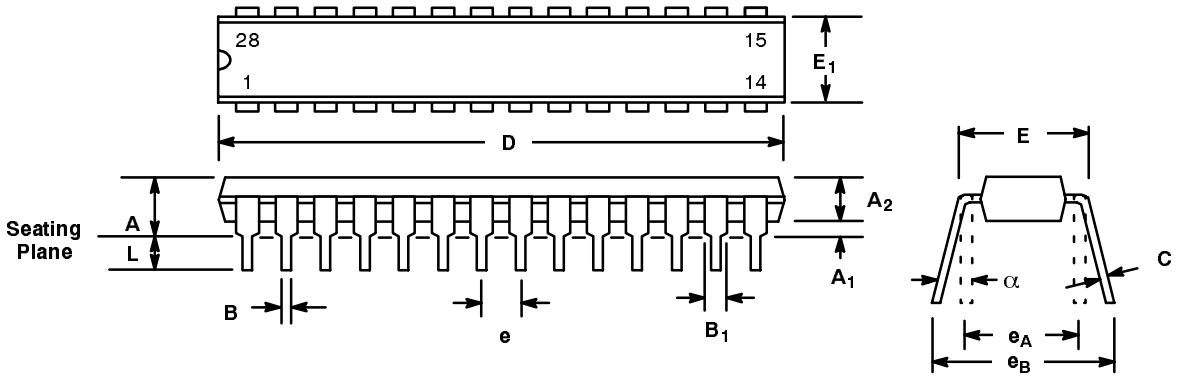


Figure 13. XRD64L15 SNR & SNDR vs. F_{IN}, V_{DD} = 3.3V, DV_{DD} = 3.3V, V_{REF} = 3V & 2V, F_S = 20MSPS, C_{IN} = 100pF

28 LEAD PLASTIC DUAL-IN-LINE (300 MIL PDIP)

Rev. 1.00

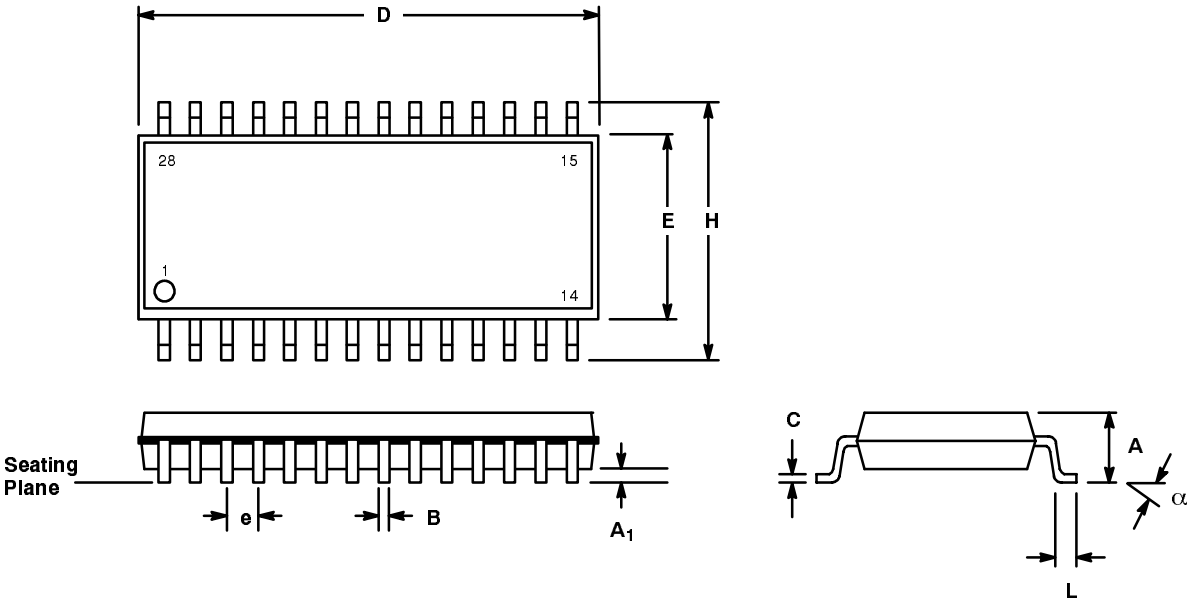


SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.145	0.210	3.68	5.33
A_1	0.015	0.070	0.51	1.78
A_2	0.115	0.195	2.92	4.95
B	0.014	0.024	0.36	0.56
B_1	0.030	0.070	0.76	1.78
C	0.008	0.014	0.20	0.38
D	1.345	1.400	34.16	35.56
E	0.300	0.325	7.62	8.26
E_1	0.265	0.310	7.11	7.49
e	0.100 BSC		2.54 BSC	
e_A	0.300 BSC		7.62 BSC	
e_B	0.310	0.430	7.87	10.92
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°

Note: The control dimension is the inch column

28 LEAD SMALL OUTLINE (300 MIL JEDEC SOIC)

Rev. 1.00

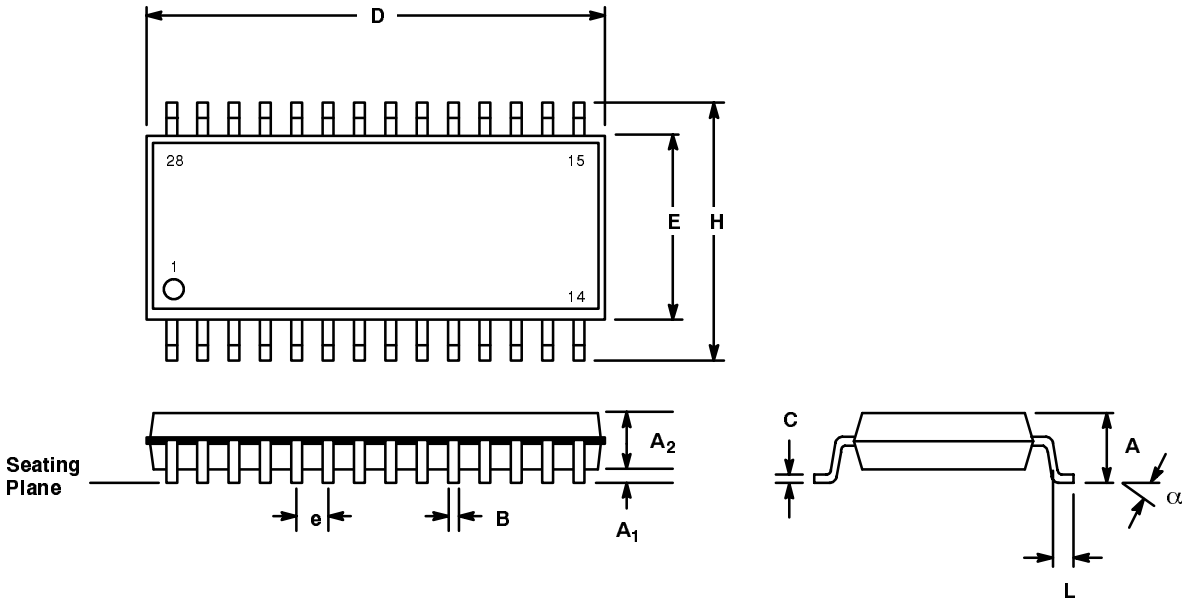


SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.013	0.020	0.33	0.51
C	0.009	0.013	0.23	0.32
D	0.697	0.713	17.70	18.10
E	0.291	0.299	7.40	7.60
e	0.050 BSC		1.27 BSC	
H	0.394	0.419	10.00	10.65
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°

Note: The control dimension is the millimeter column

28 LEAD SHRINK SMALL OUTLINE PACKAGE (5.3 mm SSOP)

Rev. 2.00

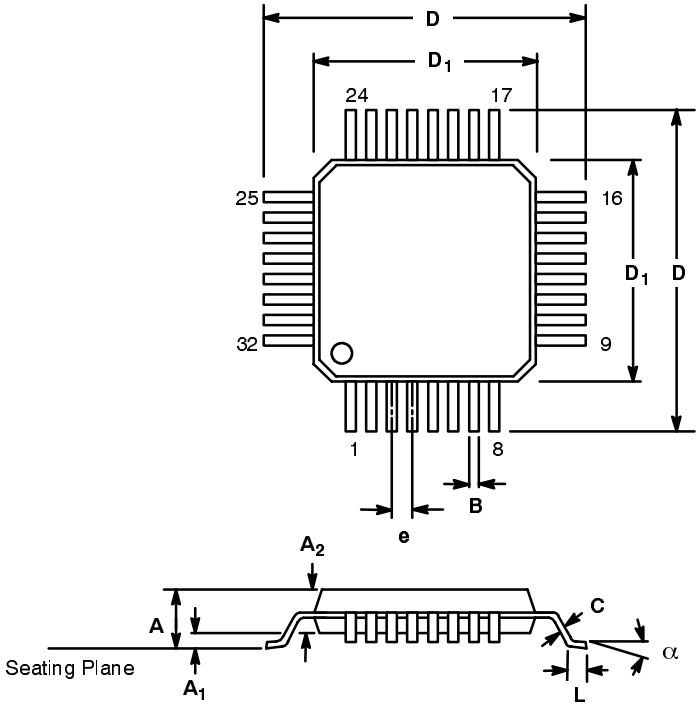


SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.067	0.079	1.70	2.00
A_1	0.002	0.006	0.05	0.15
A_2	0.065	0.073	1.65	1.85
B	0.009	0.015	0.22	0.38
C	0.004	0.010	0.09	0.25
D	0.390	0.414	9.90	10.50
E	0.197	0.221	5.00	5.60
e	0.0256 BSC		0.65 BSC	
H	0.292	0.323	7.40	8.20
L	0.022	0.037	0.55	0.95
α	0°	8°	0°	8°

Note: The control dimension is the millimeter column

32 LEAD THIN QUAD FLAT PACK (7 x 7 x 1.4 mm TQFP)

Rev. 2.00

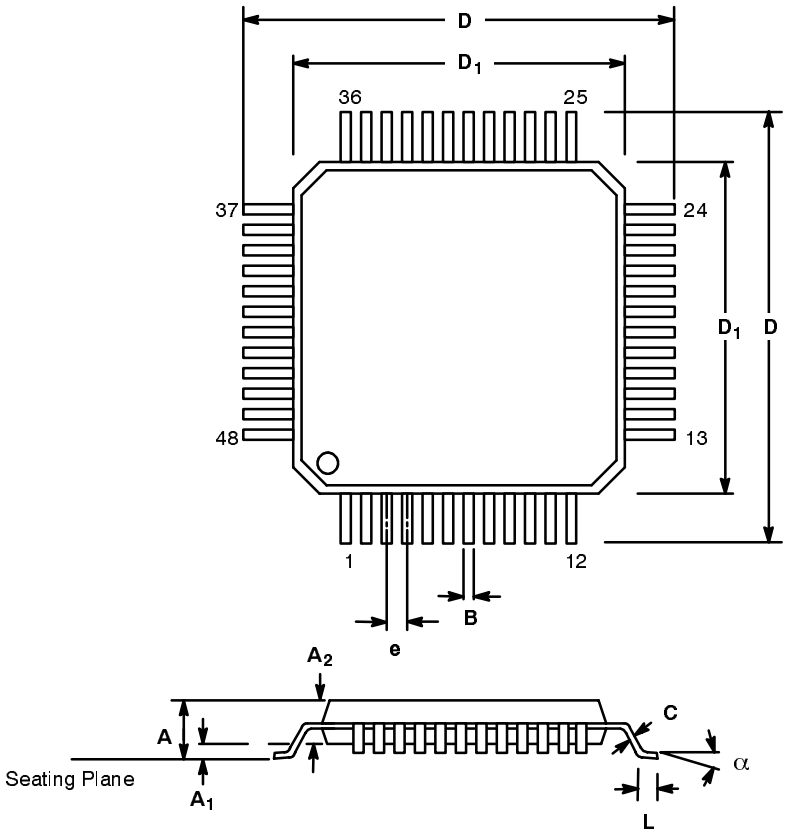


SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.055	0.063	1.40	1.60
A_1	0.002	0.006	0.05	0.15
A_2	0.053	0.057	1.35	1.45
B	0.012	0.018	0.30	0.45
C	0.004	0.008	0.09	0.20
D	0.346	0.362	8.80	9.20
D_1	0.272	0.280	6.90	7.10
e	0.0315 BSC		0.80 BSC	
L	0.018	0.030	0.45	0.75
α	0°	7°	0°	7°

Note: The control dimension is the millimeter column

48 LEAD THIN QUAD FLAT PACK
(7 x 7 x 1.0 mm, TQFP)

Rev. 1.00



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.039	0.047	1.00	1.20
A_1	0.002	0.006	0.05	0.15
A_2	0.037	0.041	0.95	1.05
B	0.007	0.011	0.17	0.27
C	0.004	0.008	0.09	0.20
D	0.346	0.362	8.80	9.20
D_1	0.272	0.280	6.90	7.10
e	0.020 BSC		0.50 BSC	
L	0.018	0.030	0.45	0.75
α	0°	7°	0°	7°

Note: The control dimension is the millimeter column

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