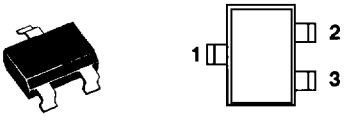
SST108 SERIES
N-Channel JFETs

Siliconix incorporated

The SST108 Series is the surface mount equivalent of our J108 device types. It features the lowest $r_{DS(ON)}$ of any SOT-23 JFET device, which makes it especially well suited for analog switching applications. Siliconix' surface mount commitment features low cost performance for a wide range of commercial applications as well as tape and reel options for automatic insertion and high-volume assembly. (See Section 7.)

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$r_{DS(ON)}$ MAX (Ω)	$I_{D(OFF)}$ TYP (pA)	t_{ON} TYP (ns)
SST108	-10	8	20	4
SST109	-6	12	20	4
SST110	-4	18	20	4

SOT-23 TOP VIEW



1 GATE
2 SOURCE
3 DRAIN

For further design information please consult the typical performance curves NIP.

SIMILAR PRODUCTS

- TO-52, See 2N5432 Series
- TO-92, See J108 Series
- Chips, See NIP Series Die

PRODUCT MARKING	
SST108	I08
SST109	I09
SST110	I10

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Gate-Drain Voltage	V_{GD}	-25	V
Gate-Source Voltage	V_{GS}	-25	
Gate Current	I_G	50	mA
Power Dissipation	P_D	350	mW
Power Derating		2.8	mW/°C
Operating Junction Temperature Range	T_J	-55 to 150	°C
Storage Temperature Range	T_{stg}	-55 to 150	
Lead Temperature ($^1/_{16}$" from case for 10 sec.)	T_L	300	

SPECIFICATIONS[a]			LIMITS							
				SST108		SST109		SST110		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-32	-25		-25		-25		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 5 V, I_D = 1 µA		-3	-10	-2	-6	-0.5	-4	
Saturation Drain Current[c]	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0 V		80		40		10		mA
Gate Reverse Current	I_{GSS}	V_{GS} = -15 V, V_{DS} = 0 V	-0.01		-3		-3		-3	nA
		T_A = 125°C	-5							
Gate Operating Current	I_G	V_{DG} = 10 V, I_D = 10 mA	-0.01							
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 5 V, V_{GS} = -10 V	0.02		3		3		3	
		T_A = 125°C	1.0							
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, $V_{DS} \leq$ 0.1 V			8		12		18	Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7							V
DYNAMIC										
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 5 V, I_D = 10 mA f = 1 kHz	17							mS
Common-Source Output Conductance	g_{os}		600							µS
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 0 V, I_D = 0 V f = 1 kHz			8		12		18	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = 0 V, V_{GS} = 0 V f = 1 MHz	60		85		85		85	pF
Common-Source Reverse Transfer Capacitance	C_{rss}	V_{DS} = 0 V, V_{GS} = -10 V f = 1 MHz	11		15		15		15	
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DG} = 5 V, I_D = 10 mA f = 1 kHz	3.5							$nV/\sqrt{Hz}$
SWITCHING										
Turn-On Time	$t_{d(ON)}$	V_{DD} = 1.5 V, $V_{GS(ON)}$ = 0 V	3							ns
	t_r	P/N $I_{D(ON)}$ $V_{GS(OFF)}$ R_L	1							
Turn-Off Time	$t_{d(OFF)}$	SST108 10mA -12V 150Ω SST109 10mA -7V 150Ω SST110 10mA -5V 150Ω	4							
	t_f		18							

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle ≤ 3%.

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