32K x 32-Bit Synchronous Pipelined Burst SRAM

FEATURES

- Synchronous Operation.
- 2 Stage Pipelined operation with 4 Burst
- On-Chip Address Counter.
- Self-Timed Write Cycle.
- On- Chip Address and Control Registers.
- Single 3.3V-5%/+10% Power Supply.
- 5V tolerant Inputs
- Byte Write Enable Control
- Asynchronous Output Enable Control.
- $\overline{ADSP}$,$\overline{ADSC}$,$\overline{ADV}$ Burst Control Pins.
- Transparent Logic Support for 1 or 2 CPU
- TTL-Level Three-State Outputs.
- TTL Compatible Inputs.
- 100-Pin QFP/TQFP Packages .

FAST ACCESS TIMES

Parameter	Symbol	-13	-15	-17	Unit
Cycle Time	tCYC	75	66	60	MHz
Clock Access Time	tCD	7	8	9	ns
Output Enable Access Time	tOE	5	5	5	ns

GENERAL DESCRIPTION

The KM732V588 is a 1,048,576-bit Synchronous Static Random Access Memory designed for high performance with advanced i486/Pentium address pipelining. When $\overline{CS1}$ is high, $\overline{ADSP}$ is blocked to control signals.

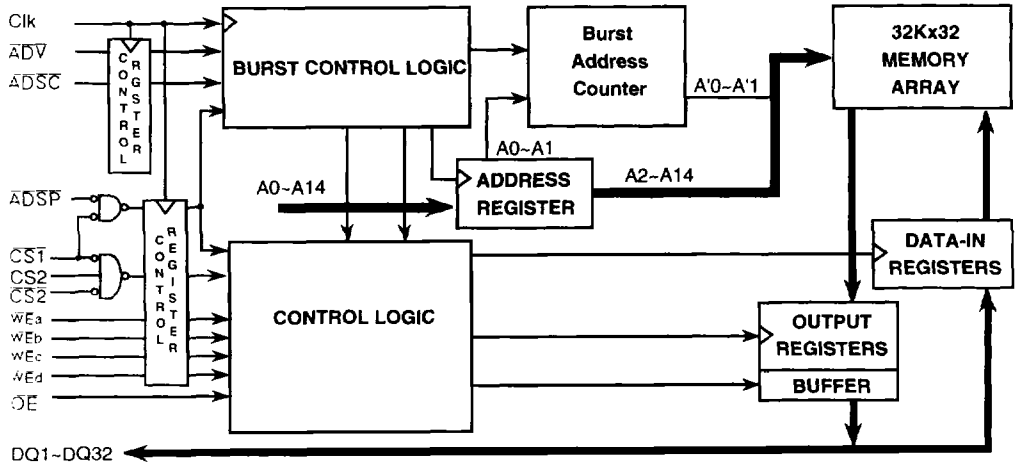
It is organized as 32,768 words of 32 bits and integrates address and control registers, a 2-bit burst address counter and high output drive circuitry onto a single integrated circuit for reduced component count implementations of high performance cache RAM applications.

Write cycles are internally self-timed and synchronous. The self-timed write feature eliminates complex off chip write pulse shaping logic, simplifying the cache design and further reducing the component count.

Bursts can be initiated with either the address status processor ($\overline{ADSP}$) or address status cache controller ($\overline{ADSC}$) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance ($\overline{ADV}$) input.

The KM732V588 is fabricated using Samsung's high performance CMOS technology and is available in a 100 pin PQFP package. Multiple power and ground pins are utilized to minimize ground bounce

LOGIC BLOCK DIAGRAM



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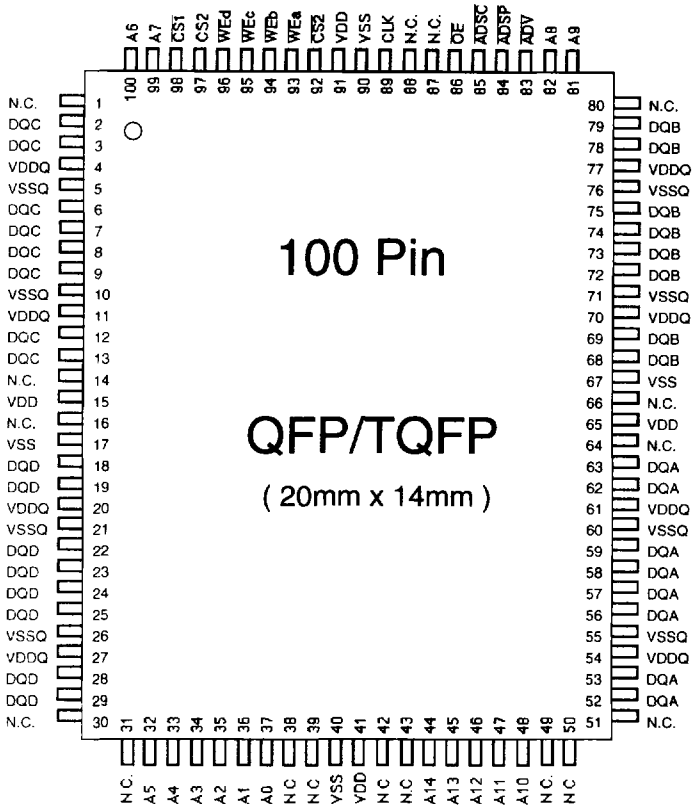
PIN CONFIGURATION (TOP VIEW)



PIN NAME

SYMBOL	PIN NAME	PIN NO.	SYMBOL	PIN NAME	PIN NO.
A0-A14	Address Inputs	32, 33, 34, 35, 36, 37, 44, 45, 46, 47, 48, 81, 82, 99, 100	NC	No Connect	1, 14, 16, 30, 31, 38, 39, 42, 43, 49 ,50, 51, 64, 66, 80, 87, 88
$\overline{ADV}$	Burst Address Advance	83			
$\overline{ADSP}$	Address Status Processor	84	DQ1~ DQ32	Data Inputs/Outputs	2, 3, 6, 7, 8, 9, 12, 13, 18, 19, 22, 23, 24, 25, 28, 29, 52, 53, 56, 57, 58, 59, 62, 63, 68, 69, 72, 73, 74, 75, 78, 79
$\overline{ADSC}$	Address Status Controller	85			
CLK	Clock	89			
$\overline{CS1}$	Chip Select	98			
CS2	Chip Select	97			
$\overline{CS2}$	Chip Select	92			
$\overline{WE}$x	Byte Write Enable	93, 94, 95, 96	VDDQ	Output Power Supply (+3.3V)	4, 11, 20, 27, 54, 61, 70, 77
$\overline{OE}$	Output Enable	86			
VDD	Power Supply (+3.3V)	15, 41, 65, 91	VSSQ	Output Ground	5, 10, 21, 26, 55,60, 71, 76
VSS	Ground	17, 40, 67, 90			

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FUNCTION DESCRIPTION

The KM732V588 is a synchronous SRAM designed to support the burst address accessing sequence of the i486/Pentium microprocessor. All inputs (with the exception of $\overline{OE}$) are sampled on rising clock edges. The start and duration of the burst access is controlled by $\overline{ADSC}$, $\overline{ADSP}$ and $\overline{ADV}$. The accesses are enabled with the chip select signals and output enable. Wait states are inserted into the access with $\overline{ADV}$.

Read cycles are initiated with $\overline{ADSP}$ (regardless of $\overline{WE}$x and $\overline{ADSC}$) using the new external address clocked into the on-chip address register whenever $\overline{ADSP}$ is sampled low, the chip selects are sampled active, and the output buffer is enabled with $\overline{OE}$. In read operation the data of cell array accessed by the current address, registered in the Data-out registers by the positive edge of Clk, are carried to the Data-out buffer by the next positive edge of Clk. The data, registered in the Data-out buffer, are projected to the output pins. $\overline{ADV}$ is ignored on the clock edge that samples $\overline{ADSP}$ asserted, but is sampled on the subsequent clock edges. The address increases internally for the next access of the burst when $\overline{WE}$x are sampled HIGH and $\overline{ADV}$ is sampled low. And $\overline{ADSP}$ is blocked to control signals by disabling $\overline{CS1}$.

Write cycles are performed by disabling the output buffers with $\overline{OE}$ and asserting $\overline{WE}$x. $\overline{WE}$x are ignored on the clock edge that samples $\overline{ADSP}$ low, but are sampled on the subsequent clock edges. The output buffers are disabled when $\overline{WE}$x are sampled low (regardless of $\overline{OE}$). Data is clocked into the data input register when $\overline{WE}$x sampled low. The address increases internally to the next address of burst if both $\overline{WE}$x and $\overline{ADV}$ are sampled low. Individual byte write cycles are performed by any one or more byte write enable signals($\overline{WE}$a, $\overline{WE}$b, $\overline{WE}$c or $\overline{WE}$d) sampled low. $\overline{WE}$a controls DQ1~DQ8, $\overline{WE}$b, controls DQ9~DQ16, $\overline{WE}$c controls DQ17~DQ24 and $\overline{WE}$d controls DQ25~DQ32. Read or write cycles (depending on $\overline{WE}$) may also be initiated with $\overline{ADSC}$, instead of $\overline{ADSP}$. The differences between cycles initiated with $\overline{ADSC}$ and $\overline{ADSP}$ are as follows;

- $\overline{ADSP}$ must be sampled high when $\overline{ADSC}$ is sampled low to initiate a cycle with $\overline{ADSC}$.
- $\overline{WE}$x are sampled on the same clock edge that samples $\overline{ADSC}$ low (and $\overline{ADSP}$ high).

Addresses are generated for the burst access as shown below. The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion.

BURST SEQUENCE TABLE

	Case 1		Case 2		Case 3		Case 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
↓	0	1	0	0	1	1	1	0
	1	0	1	1	0	0	0	1
Fourth Address	1	1	1	0	0	1	0	0

TRUTH TABLES

SYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

$\overline{CST}$	CS2	$\overline{CS2}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WEx}$	K	Address Accessed	Operation
H	X	X	X	L	X	X	↑	N/A	Not Selected
L	L	X	L	X	X	X	↑	N/A	Not Selected
L	X	H	L	X	X	X	↑	N/A	Not Selected
L	L	X	X	L	X	X	↑	N/A	Not Selected
L	X	H	X	L	X	X	↑	N/A	Not Selected
L	H	L	L	X	X	X	↑	External Address	Begin Burst Read Cycle
L	H	L	H	L	X	L	↑	External Address	Begin Burst Write Cycle
L	H	L	H	L	X	H	↑	External Address	Begin Burst Read Cycle
X	X	X	H	H	L	H	↑	Next Address	Continue Burst Read Cycle
H	X	X	X	H	L	H	↑	Next Address	Continue Burst Read Cycle
X	X	X	H	H	L	L	↑	Next Address	Continue Burst Write Cycle
H	X	X	X	H	L	L	↑	Next Address	Continue Burst Write Cycle
X	X	X	H	H	H	H	↑	Current Address	Suspend Burst Read Cycle
H	X	X	X	H	H	H	↑	Current Address	Suspend Burst Read Cycle
X	X	X	H	H	H	L	↑	Current Address	Suspend Burst Write Cycle
H	X	X	X	H	H	L	↑	Current Address	Suspend Burst Write Cycle

NOTE 1 : X means "Don't Care"

NOTE 2 : The rising edge of clock is symbolized by ↑

PASS-THROUGH TRUTH TABLE

Previous Cycle		Present Cycle				Next Cycle
Operation	$\overline{WEx}$	Operation	$\overline{CST}$	$\overline{WEx}$	$\overline{OE}$	
Write Cycle, All bytes Address=An-1, Data=Dn-1	L	Initiate Read Cycle Address=An, Data=Qn-1	L	H	L	Read Cycle Data=Qn
Write Cycle, All bytes Address=An-1, Data=Dn-1	L	No new cycle Data=Qn-1	H	H	L	No carryover from previous cycle
Write Cycle, All bytes Address=An-1, Data=Dn-1	L	No new cycle Data=High-Z	H	H	H	No carryover from previous cycle

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on V_{DD} Supply Relative to Vss	V_{DD}	-0.3 to 4.6	V
Voltage on Any Other Pin Relative to Vss	V_{IN}	-0.3 to 6.0	V
Power Dissipation	P_D	1.2	W
Storage Temperature	T_{STG}	-65 to +150	°C
Operating Temperature	T_{OPR}	0 to +70	°C
Storage Temperature Range Under Bias	T_{BIAS}	-10 to +85	°C

***NOTE** : Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V_{DD}	3.13	3.3	3.6	V
Ground	Vss	0	0	0	V

DC ELECTRICAL CHARACTERISTICS (V_{DD}=3.3V-5%/+10%, TA=0°C to +70°C)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	Iil	V_{DD}=Max; V_{IN}=Vss to V_{DD}		-2	+2	μA
Output Leakage Current	Iol	Output Disabled, V_{OUT}=Vss to V_{DD}		-2	+2	μA
Operating Current	Icc	V_{DD}=Max	75MHz	-	220	mA
		I_{OUT}=0mA	66MHz	-	200	
		Cycle Time ≥ tCYC min	60MHz	-	180	
Standby Current	Isb	Device deselected, I_{OUT}=0mA, Cycle Time ≥ tCYC min All Inputs=Fix (V_{DD}-0.2 or 0.2V)		-	40	mA
	Isb1	Device deselected, I_{OUT}=0mA, Cycle Time =0MHz All Inputs=Fix (V_{DD}-0.2 or 0.2V)		-	20	mA
Output Low Voltage	Vol	Iol=8.0mA		-	0.4	V
Output High Voltage	Voh	Ioh=-4.0mA		2.4	-	V
Input Low Voltage	Vil			-0.5*	0.8	V
Input High Voltage	Vih			2.2	5.5**	V

* Vil(min)=-3.0 (Pulse Width ≤20ns)

** In Case of I/O Pins, the Max.Vih=Vcc + 0.5V

CAPACITANCE* (T_A=25°C, f=1Mhz)

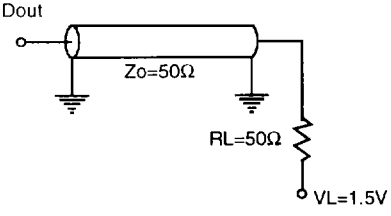
Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	5	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	-	7	pF

*NOTE : Sampled not 100% tested.

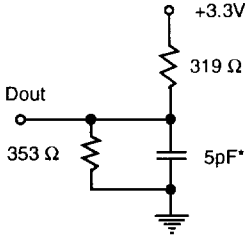
TEST CONDITIONS (T_A=0°C to 70°C, V_{DD}=3.3V-5%/+10%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time (Measured at 0.3V and 2.7V)	2ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1

Output Load (A)



Output Load (B)
(for tLZC, tLZOE, tHZOE & tHZC)



* Including Scope and Jig Capacitance

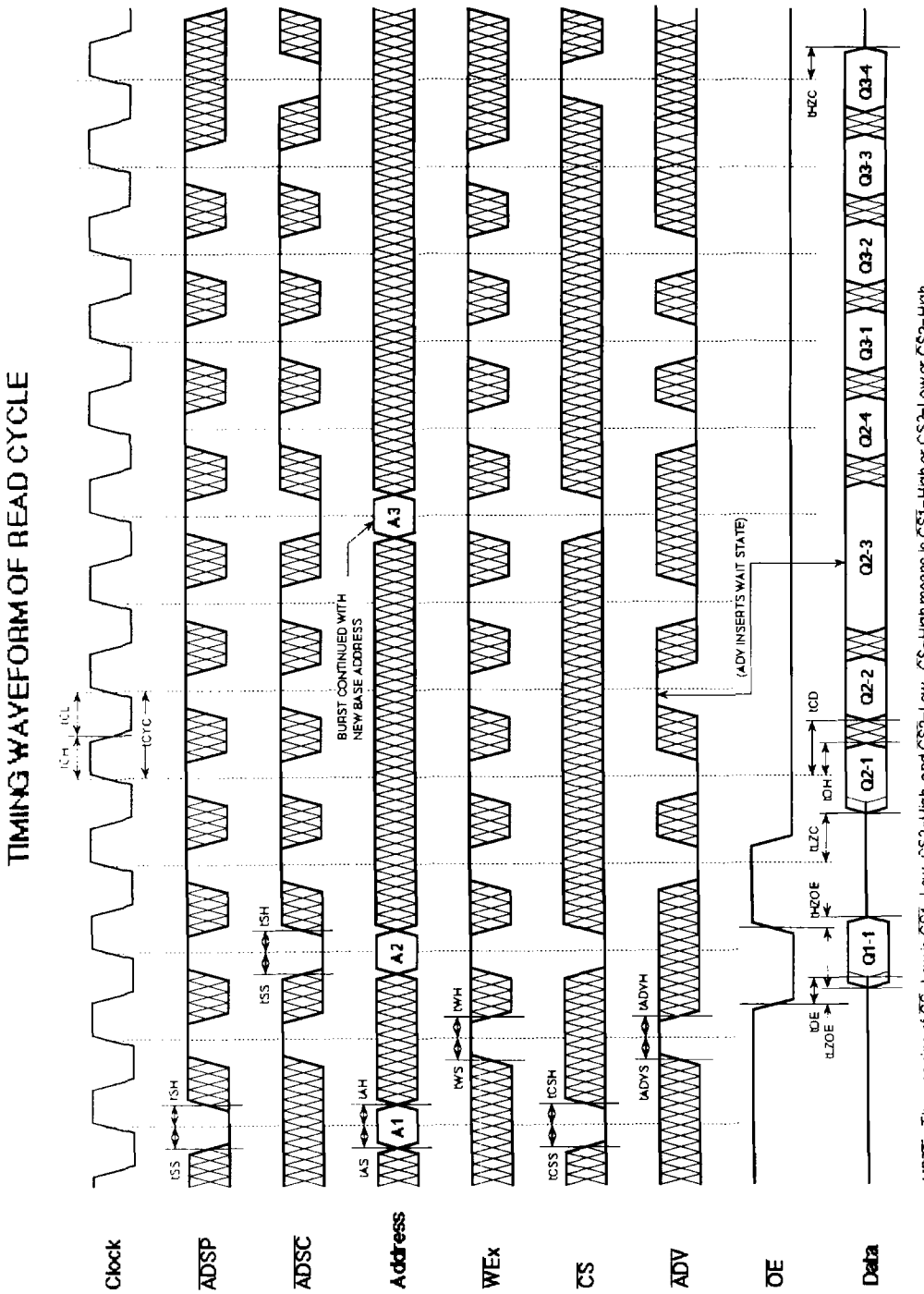
Fig. 1

AC TIMING CHARACTERISTICS (V_{DD}=3.3V-5%/+10%, T_A=0°C to +70°C)

Parameter	Symbol	KM732V588-13		KM732V588-15		KM732V588-17		Unit
		Min	Max	Min	Max	Min	Max	
Cycle Time	tCYC	13		15		17		ns
Clock Access Time	tCD		7		8		9	ns
Output Enable to Data Valid	tOE		5		5		5	ns
Clock High to Output Low-Z	tLZC	6		6		6		ns
Output Hold from Clock High	tOH	2.5		2.5		2.5		ns
Output Enable Low to Output Low-Z	tLZOE	2		2		2		ns
Output Enable High to Output High-Z	tHZOE	2	5	2	6	2	6	ns
Clock High to Output High-Z	tHZC		5		6		6	ns
Clock High Pulse Width	tCH	4.5		5.5		6		ns
Clock Low Pulse Width	tCL	4.5		5.5		6		ns
Address Setup to Clock High	tAS	2.5		2.5		2.5		ns
Address Status Setup to Clock High	tSS	2.5		2.5		2.5		ns
Data Setup to Clock High	tDS	2.5		2.5		2.5		ns
Write Setup to Clock High	tWS	2.5		2.5		2.5		ns
Address Advance Setup to Clock High	tADVS	2.5		2.5		2.5		ns
Chip Select Setup to Clock High	tCSS	2.5		2.5		2.5		ns
Address Hold from Clock High	tAH	0.5		0.5		0.5		ns
Address Status Hold from Clock High	tSH	0.5		0.5		0.5		ns
Data Hold from Clock High	tDH	0.5		0.5		0.5		ns
Write Hold from Clock High	tWH	0.5		0.5		0.5		ns
Address Advance Hold from Clock High	tADVH	0.5		0.5		0.5		ns
Chip Select Hold from Clock High	tCSH	0.5		0.5		0.5		ns

NOTE : All address inputs must meet the specified setup and hold times for all rising clock (Clk) edges whenever $\overline{ADSC}$ and/or $\overline{ADSP}$ is sampled low and this device is chip selected. All other synchronous inputs must meet the specified sample and hold times whenever this device is chip selected. Both chip selects must be active whenever $\overline{ADSC}$ or $\overline{ADSP}$ is sampled low in order for the this device to remain enabled.

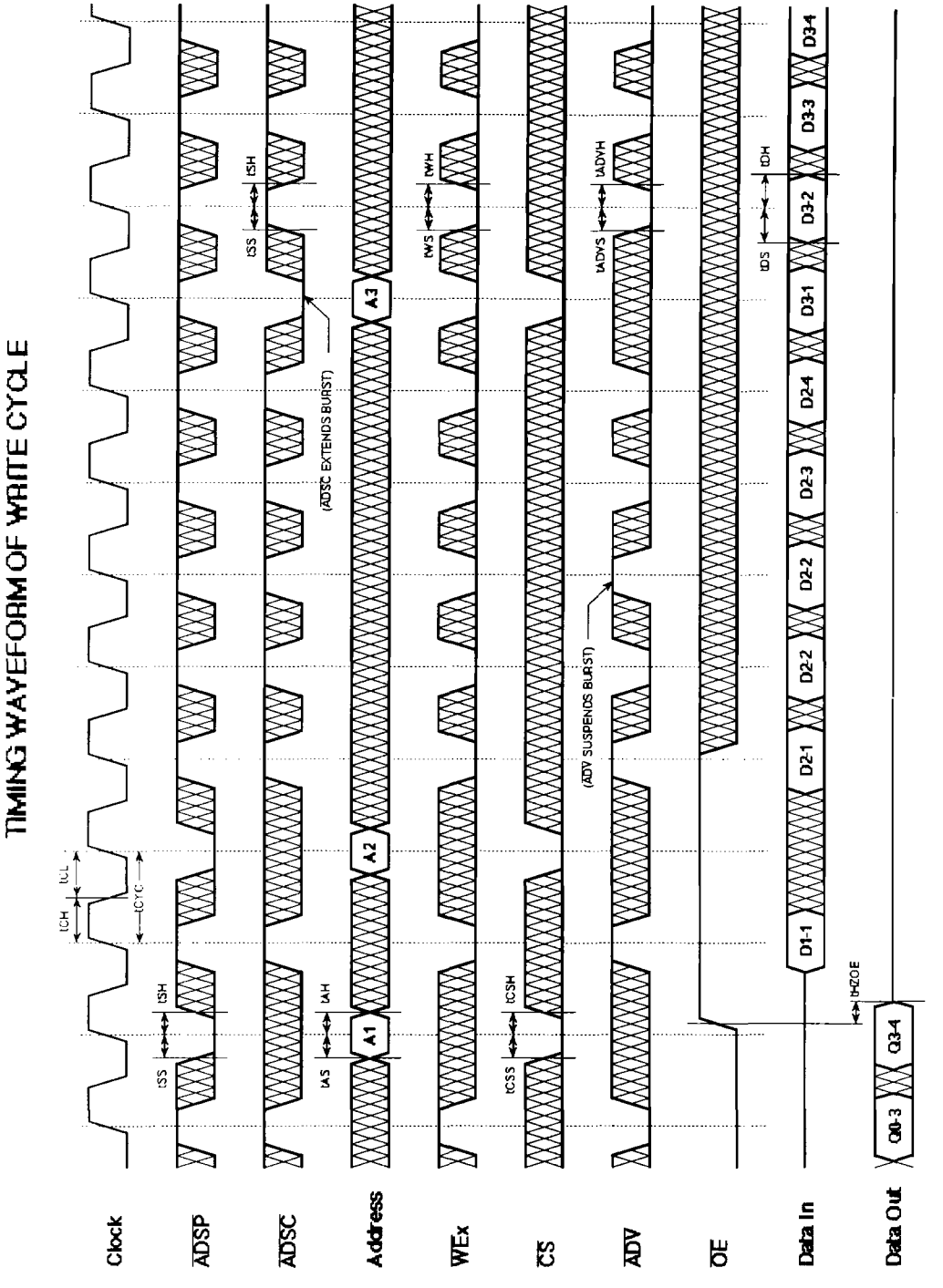
TIMING WAVEFORM OF READ CYCLE



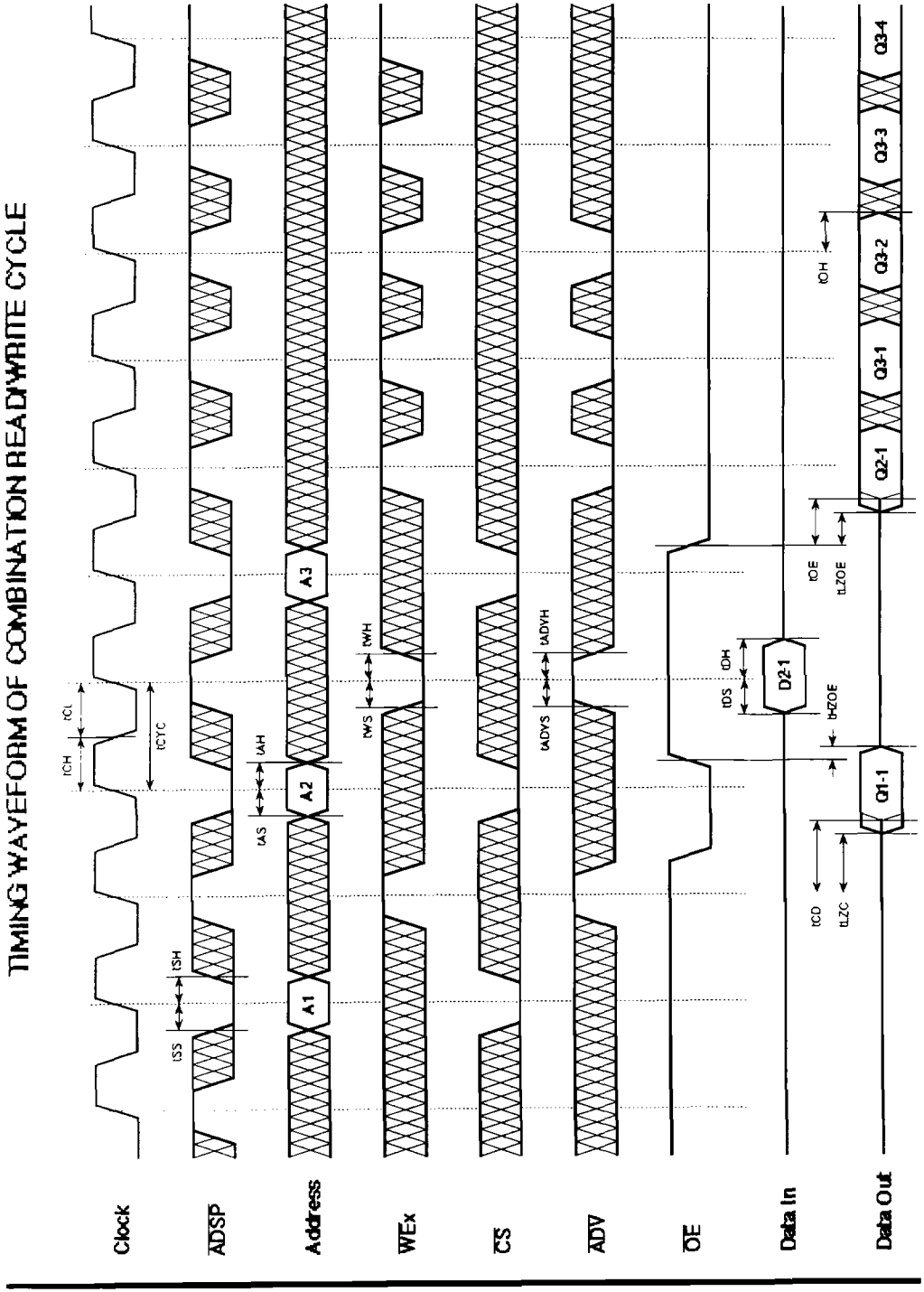
NOTE : The meaning of CS=Low is CS1=Low, CS2=High, and CS2=Low. CS=High means is CS1=High or CS2=Low or CS2=High

2

TIMING WAVEFORM OF WRITE CYCLE



TIMING WAVEFORM OF COMBINATION READ/WRITE CYCLE



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TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE (ADSC Controlled)