VCXO JITTER ATTENUATOR & FEMTOCLOCK™ MULTIPLIER

ICS810252I-03

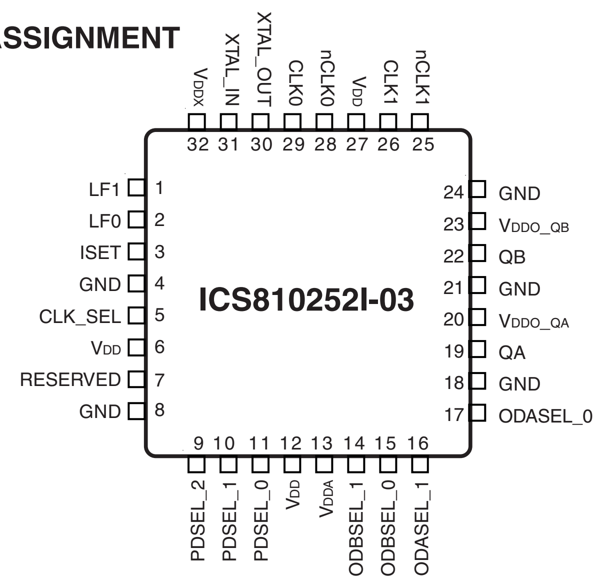
General Description

The ICS810252I-03 is a member of the HiperClockS™ family of high performance clock solutions from IDT. The ICS810252I-03 is a PLL based synchronous multiplier that is optimized for PDH or SONET to Ethernet clock jitter attenuation and frequency translation. The device contains two internal frequency multiplication stages that are cascaded in series. The first stage is a VCXO PLL that is optimized to provide reference clock jitter attenuation. The second stage is a FemtoClock™ frequency multiplier that provides the low jitter, high frequency Ethernet output clock that easily meets Gigabit and 10 Gigabit Ethernet jitter requirements. Pre-divider and output divider multiplication ratios are selected using device selection control pins. The multiplication ratios are optimized to support most common clock rates used in PDH, SONET and Ethernet applications. The VCXO requires the use of an external, inexpensive pullable crystal. The VCXO uses external passive loop filter components which allows configuration of the PLL loop bandwidth and damping characteristics. The device is packaged in a space-saving 32-VFQFN package and supports industrial temperature range.

Features

- Two LVCMOS/LVTTL outputs, 15Ω impedance
  Each output supports independent frequency selection at 25MHz, 62.5MHz, 125MHz, and 156.25MHz
- Two differential inputs support the following input types: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- Accepts input frequencies from 8kHz to 155.52MHz including 8kHz, 1.544MHz, 2.048MHz, 19.44MHz, 25MHz, 77.76MHz, 125MHz and 155.52MHz
- Attenuates the phase jitter of the input clock by using a low-cost pullable funamental mode VCXO crystal
- VCXO PLL bandwidth can be optimized for jitter attenuation and reference tracking using external loop filter connection
- FemtoClock frequency multiplier provides low jitter, high frequency output
- Absolute pull range: 50ppm
- FemtoClock VCO frequency: 625MHz
- RMS phase jitter @ 125MHz, using a 25MHz crystal (12kHz - 20MHz): 1.5ps (typical)
- 3.3V supply voltage
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

Pin Assignment



32-Lead VFQFN
5mm x 5mm x 0.925 package body
K Package
Top View

32-Lead TQFP, E-Pad
7mm x 7mm x 1.0mm package body
Y package
Top View

The Preliminary Information presented herein represents a product in pre-production. The noted characteristics are based on initial product characterization and/or qualification. Integrated Device Technology, Incorporated (IDT) reserves the right to change any circuitry or specifications without notice.

Block Diagram

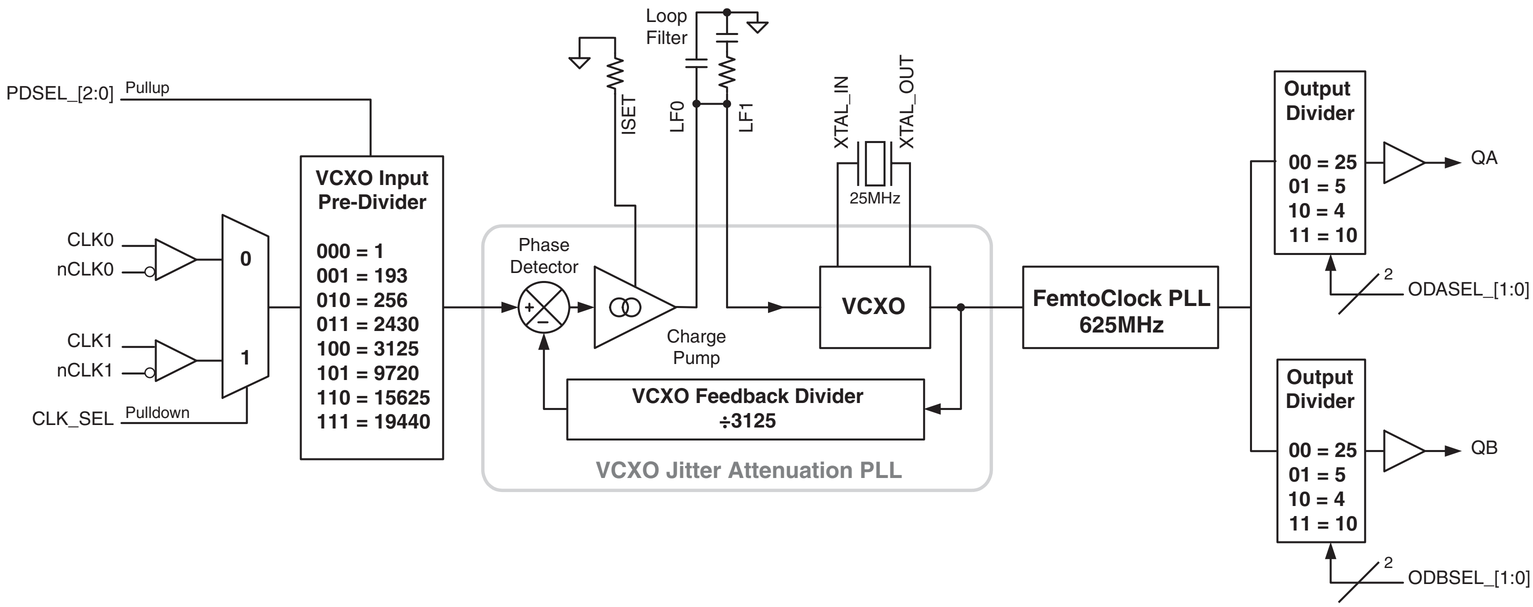


TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 2	LF1, LF0	Analog Input/Output		Loop filter connection node pins.
3	ISET	Analog Input/Output		Charge pump current setting pin.
4, 8, 18, 21, 24	GND	Power		Power supply ground.
5	CLK_SEL	Input	Pulldown	Input clock select. When HIGH selects CLK1/nCLK1. When LOW, selects CLK0/nCLK0. LVCMOS/LVTTL interface levels.
6, 12, 27	V_{DD}	Power		Core power supply pins.
7	RESERVED	Reserved		Reserved pin. Do not connect.
9, 10, 11	PDSEL_2, PDSEL_1, PDSEL_0	Input	Pullup	Pre-divider select pins. LVCMOS/LVTTL interface levels. See Table 3A.
13	V_{DDA}	Power		Analog supply pin.
14, 15	ODBSEL_1, ODBSEL_0	Input	Pulldown	Frequency select pins for Bank B output. See Table 3B. LVCMOS/LVTTL interface levels.
16, 17	ODASEL_1, ODASEL_0	Input	Pulldown	Frequency select pins for Bank A output. See Table 3B. LVCMOS/LVTTL interface levels.
19	QA	Output		Bank A single-ended clock output. LVCMOS/LVTTL interface levels. 15Ω output impedance.
20	V_{DDO_QA}	Power		Output power supply pin for QA clock output.
22	QB	Output		Bank B single-ended clock output. LVCMOS/LVTTL interface levels. 15Ω output impedance.
23	V_{DDO_QB}	Power		Output power supply pin for QB clock output.
25	nCLK1	Input	Pullup/ Pulldown	Inverting differential clock input. $V_{DD}/2$ bias voltage when left floating.
26	CLK1	Input	Pulldown	Non-inverting differential clock input.
28	nCLK0	Input	Pullup/ Pulldown	Inverting differential clock input. $V_{DD}/2$ bias voltage when left floating.
29	CLK0	Input	Pulldown	Non-inverting differential clock input.
30, 31	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input. XTAL_OUT is the output.
32	V_{DDX}	Power		Power supply pin for VCXO charge pump.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
C_{PD}	Power Dissipation Capacitance (per output)	V_{DD}, V_{DDX}, V_{DDO_QA}, V_{DDO_QB} = 3.465V		TBD		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{OUT}	Output Impedance			15		Ω

TABLE 3A. PRE-DIVIDER FUNCTION TABLE

Inputs			Pre-Divider Value
PDSEL_2	PDSEL_1	PDSEL_0	
0	0	0	1
0	0	1	193
0	1	0	256
0	1	1	2430
1	0	0	3125
1	0	1	9720
1	1	0	15625
1	1	1	19440 (default)

TABLE 3B. OUTPUT DIVIDER FUNCTION TABLE

Inputs		Output Divider Value
ODxSEL_1	ODxSEL_0	
0	0	25 (default)
0	1	5
1	0	4
1	1	10

TABLE 3C. FREQUENCY FUNCTION TABLE

Input Frequency (MHz)	Pre-Divider Value	VCXO Frequency (MHz)	FemtoClock Feedback Divider Value	Femtoclock VCO Frequency (MHz)	Output Divider Value	Output Frequency (MHz)
0.008	1	25	25	625	25	25
0.008	1	25	25	625	5	125
0.008	1	25	25	625	4	156.25
0.008	1	25	25	625	10	62.5
1.544	193	25	25	625	25	25
1.544	193	25	25	625	5	125
1.544	193	25	25	625	4	156.25
1.544	193	25	25	625	10	62.5
2.048	256	25	25	625	25	25
2.048	256	25	25	625	5	125
2.048	256	25	25	625	4	156.25
2.048	256	25	25	625	10	62.5
19.44	2430	25	25	625	25	25
19.44	2430	25	25	625	5	125
19.44	2430	25	25	625	4	156.25
19.44	2430	25	25	625	10	62.5
25	3125	25	25	625	25	25
25	3125	25	25	625	5	125
25	3125	25	25	625	4	156.25
25	3125	25	25	625	10	62.5
77.76	9720	25	25	625	25	25
77.76	9720	25	25	625	5	125
77.76	9720	25	25	625	4	156.25
77.76	9720	25	25	625	10	62.5
125	15625	25	25	625	25	25
125	15625	25	25	625	5	125
125	15625	25	25	625	4	156.25
125	15625	25	25	625	10	62.5
155.52	19440	25	25	625	25	25
155.52	19440	25	25	625	5	125
155.52	19440	25	25	625	4	156.25
155.52	19440	25	25	625	10	62.5

Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	
32 Lead VFQFN	37°C/W (0 mps)
32 Lead TQFP	32.2°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDO\_QA} = V_{DDO\_QB} = V_{DDX}$ = 3.3V±5%, TA = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.11	3.3	V_{DD}	V
V_{DDO_QA}, V_{DDO_QB}	Output Supply Voltage		3.135	3.3	3.465	V
V_{DDX}	Charge Pump Supply Voltage		3.135	3.3	3.465	V
$I_{DD} + I_{DDX}$	Power and Charge Pump Supply Current			158		mA
I_{DDA}	Analog Supply Current			11		mA
$I_{DDO\_QA} + I_{DDO\_QB}$	Output Supply Current			1		mA

Table 4B. LVCMOS / LVTTL DC Characteristics, $V_{DD} = V_{DDO\_QA} = V_{DDO\_QB} = V_{DDX}$ = 3.3V±5%, TA = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	CLK_SEL, ODASEL_[0:1], ODBSEL_[0:1]	$V_{DD} = V_{IN}$ = 3.465V			150	µA
		PDSEL{0:2]	$V_{DD} = V_{IN}$ = 3.465V			5	µA
I_{IL}	Input Low Current	CLK_SEL, ODASEL_[0:1], ODBSEL_[0:1]	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		PDSEL{0:2]	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
V_{OH}	Output High Voltage; NOTE 1			2.6			V
V_{OL}	Output Low Voltage; NOTE 1					0.5	V

NOTE 1: Outputs terminated with 50Ω to $V_{DDO\_QA,\_QB}$/2.

TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS, $V_{DD} = V_{DDO\_QA} = V_{DDO\_QB} = V_{DDX}$ = 3.3V±5%, TA = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK0/nCLK0, CLK1/nCLK1	$V_{IN} = V_{DD}$ = 3.465V			150	µA
I_{IL}	Input Low Current	CLK0, CLK1	V_{IN} = 0V, V_{DD} = 3.465V	-5			µA
		nCLK0, nCLK1	V_{IN} = 0V, V_{DD} = 3.465V	-150			µA
V_{PP}	Peak-to-Peak Input Voltage; NOTE 1			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		V_{DD} - 0.85	V

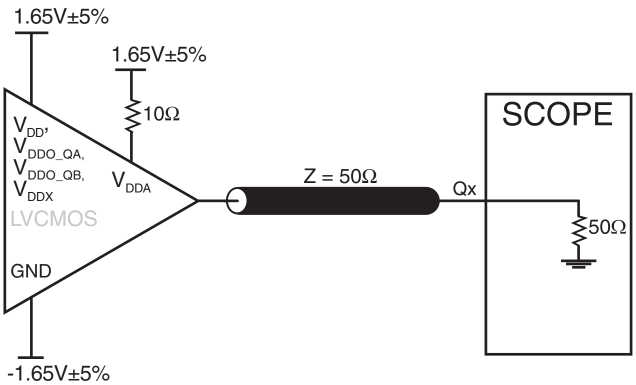
NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2: Common mode voltage is defined as V_{IH}.

TABLE 5. AC CHARACTERISTICS, $V_{DD} = V_{DDO\_QA} = V_{DDO\_QB} = V_{DDX}$ = 3.3V±5%, TA = -40°C TO 85°C

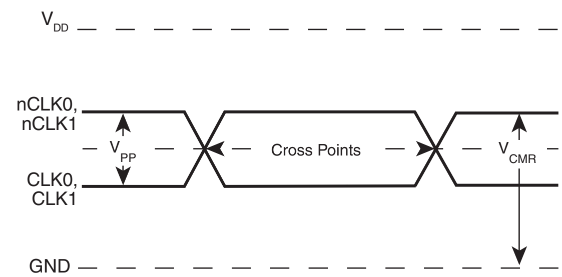
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{IN}	Input Frequency		0.008		155.52	MHz
f_{OUT}	Output Frequency		25		156.25	MHz
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 1	125MHz, 25MHz crystal Integration Range: 12kHz - 20MHz		1.5		ps
*t*sk(o)	Output Skew; NOTE 2, 3			60		ps
odc	Output Duty Cycle			50		%
t_R / t_F	Output Rise/Fall Time	20% to 80%		400		ps
t_{LOCK}	PLL Lock Time			100		ms

NOTE 1: Please refer to the Phase Noise Plot.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load condtions.
Measured at the output differential cross points.

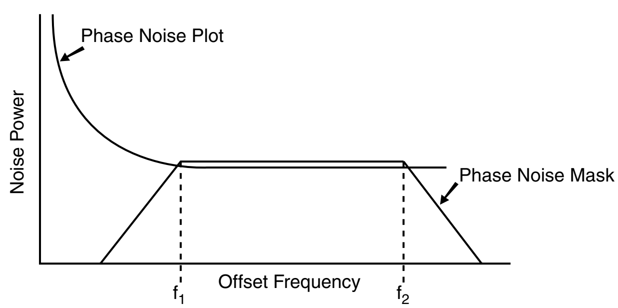
Parameter Measurement Information



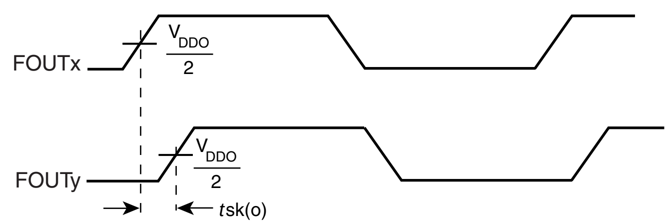
3.3V Output Load AC Test Circuit



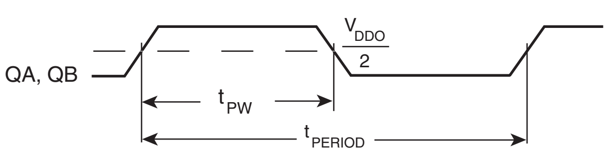
Differential Input Level



Phase Jitter

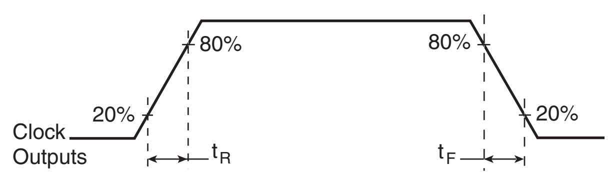


Output Skew



$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

Output Duty Cycle/Pulse Width/tPeriod



Output Rise/Fall Time

Application Information

Power Supply Filtering Techniques

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS810252I-03 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDX}, V_{DDA}, V_{DDO_QA} and V_{DDO_QB} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10mF and a .01mF bypass capacitor should be connected to each V_{DDA} pin.

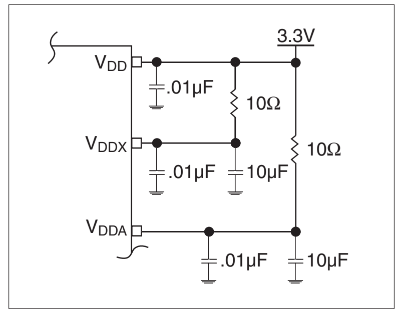


Figure 1. Power Supply Filtering

Recommendations for Unused Input and Output Pins

Inputs:

Crystal Inputs
For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

CLK/nCLK Input
For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

LVCMOS Control Pins
All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVCMOS Outputs
All unused LVCMOS output can be left floating. There should be no trace attached.

Wiring the Differential Input to Accept Single Ended Levels

Figure 2 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF ≃ V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

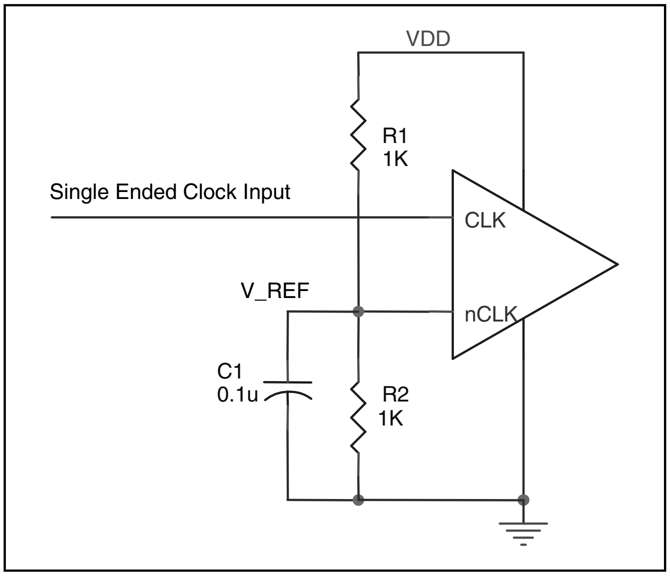


Figure 2. Single Ended Signal Driving Differential Input

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both signals must meet the V_{PP} and V_{CMR} input requirements. *Figures 3A to 3F* show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in Figure 3A, the input termination applies for IDT HiPerClockS open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

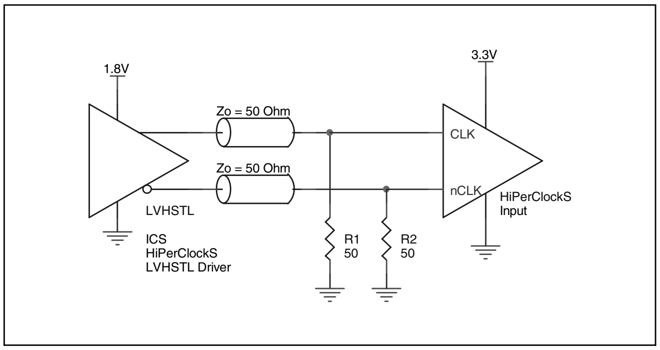


Figure 3A. HiPerClockS CLK/nCLK Input Driven by an IDT Open Emitter HiPerClockS LVHSTL Driver

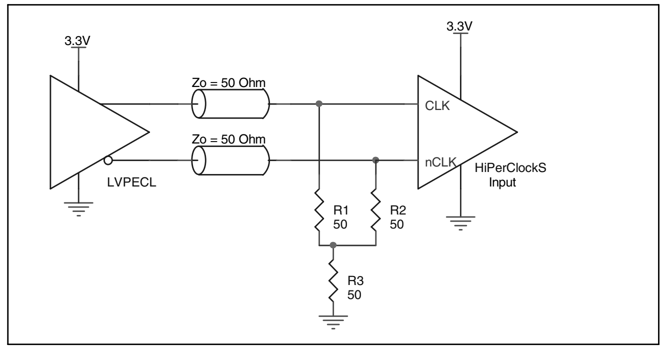


Figure 3B. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver

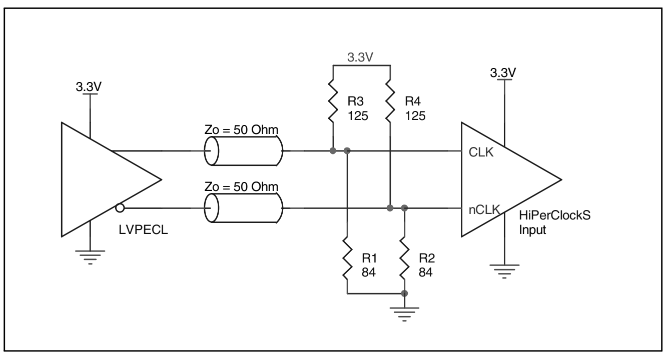


Figure 3C. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver

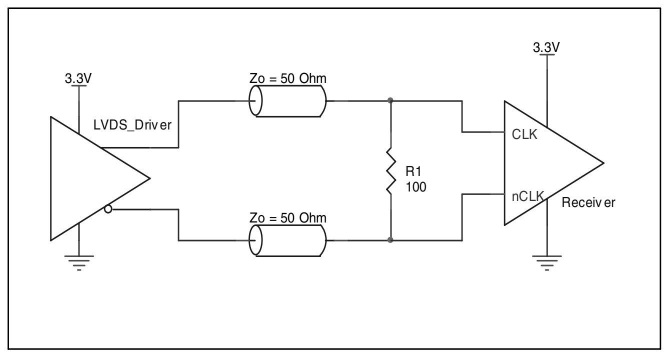


Figure 3D. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVDS Driver

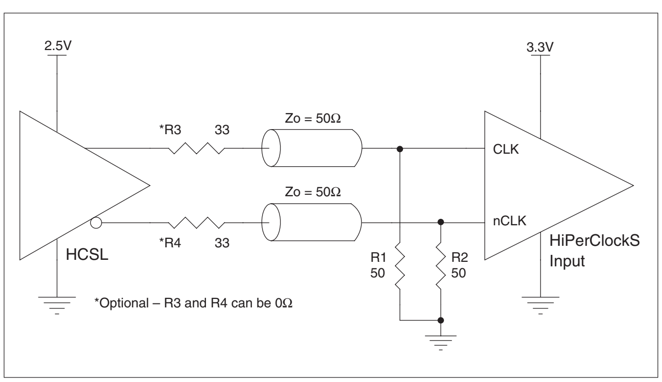


Figure 3E. HiPerClockS CLK/nCLK Input Driven by a 3.3V HCSL Driver

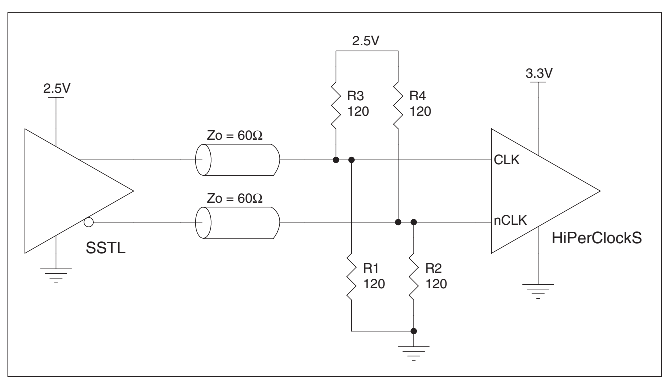


Figure 3F. HiPerClockS CLK/nCLK Input Driven by a 2.5V SSTL Driver

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 4.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as "heat pipes". The number of vias (i.e. "heat pipes") are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, refer to the Application Note on the *Surface Mount Assembly* of Amkor's Thermally/Electrically Enhance Leadfame Base Package, Amkor Technology.

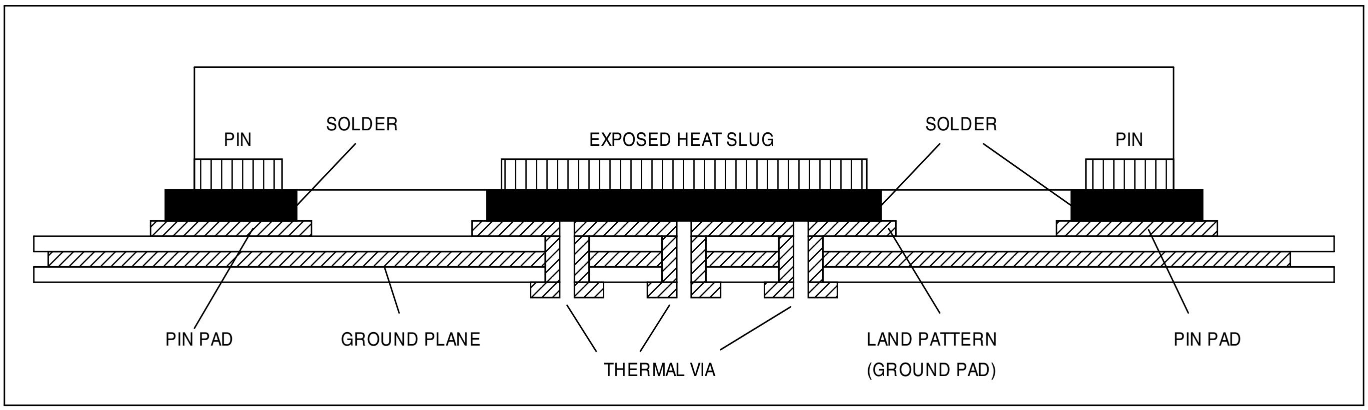


Figure 4. P.C.Assembly for Exposed Pad Thermal Release Path –Side View (Drawing not to Scale)

TQFP Thermal Release Path

The expose metal pad provides heat transfer from the device to the P.C. board. The expose metal pad is ground pad connected to ground plane through thermal via. The exposed pad on the device to the exposed metal pad on the PCB is contacted through solder as shown in *Figure 5.* For further information, please refer to the Application Note on Surface Mount Assembly of Amkor's Thermally /Electrically Enhance Leadframe Base Package, Amkor Technology.

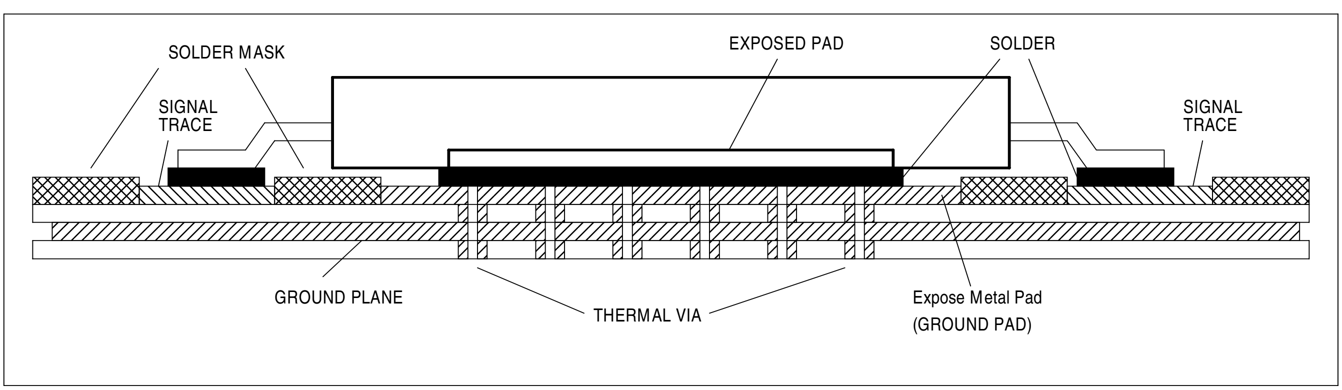


Figure 5. P.C. Board for Exposed Pad Thermal Release Path Example

Layout Guideline

Figure 6 shows an example of the 810252I-03 application schematic. In this example, the device is operated at V_{DD} = 3.3V. The decoupling capacitors should be located as close as possible to the power pin. The input is driven by a 3.3V LVPECL driver.

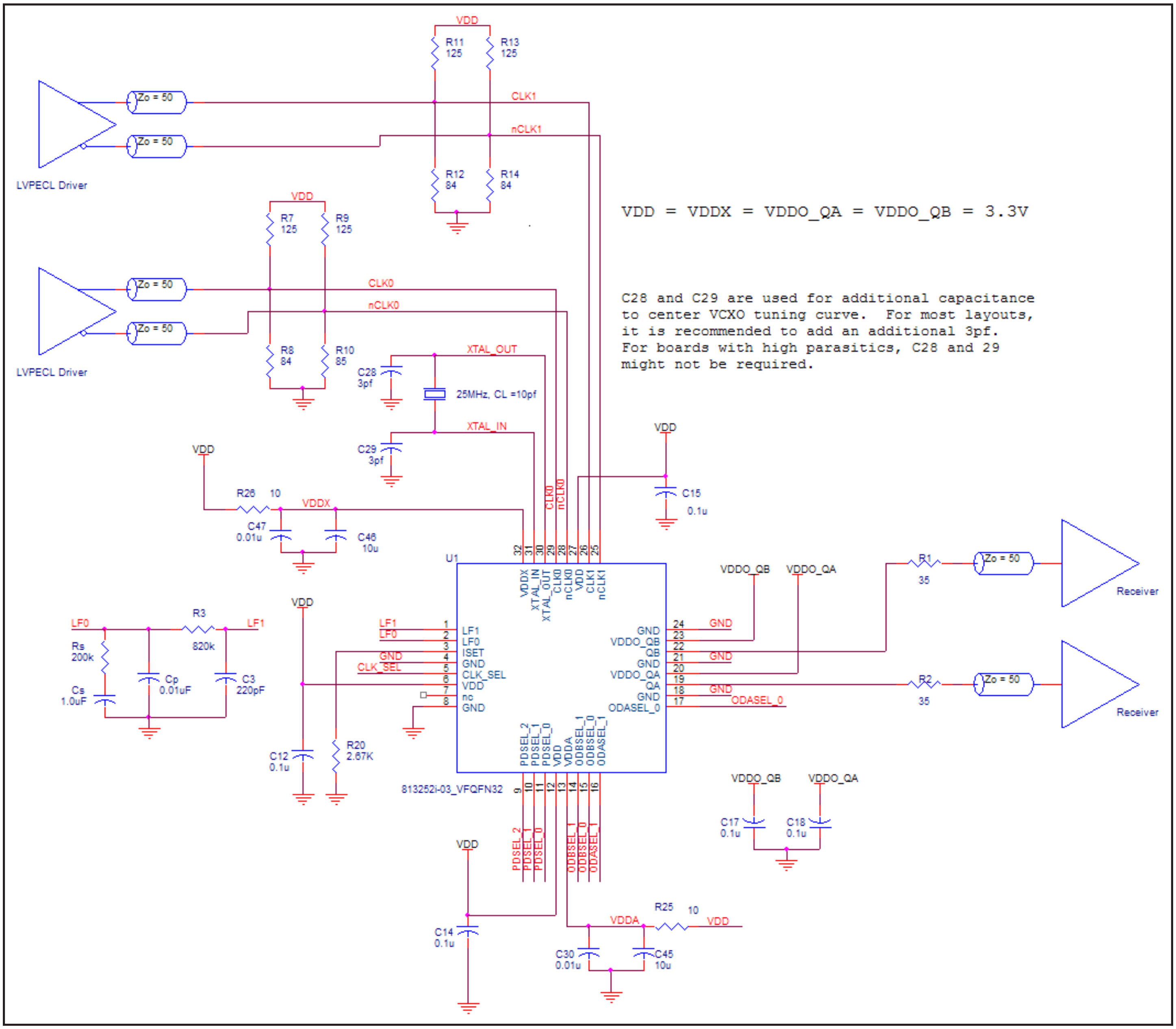


Figure 6. Schematic of Recommended Layout

VCXO-PLL External Components

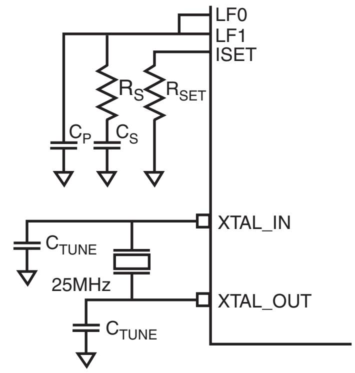
Choosing the correct external components and having a proper printed circuit board (PCB) layout is a key task for quality operation of the VCXO-PLL. In choosing a crystal, special precaution must be taken with the package and load capacitance (C_L). In addition, frequency, accuracy and temperature range must also be considered. Since the pulling range of a crystal also varies with the package, it is recommended that a metal-canned package like HC49 be used. Generally, a metal-canned package has a larger pulling range than a surface mounted device (SMD). For crystal selection information, refer to the *VCXO Crystal Selection Application Note.*

The crystal's load capacitance C_L characteristic determines its resonating frequency and is closely related to the VCXO tuning range. The total external capacitance seen by the crystal when installed on a board is the sum of the stray board capacitance, IC package lead capacitance, internal varactor capacitance and any installed tuning capacitors (C_{TUNE}).

If the crystal C_L is greater than the total external capacitance, the VCXO will oscillate at a higher frequency than the crystal specification. If the crystal C_L is lower than the total external capacitance, the VCXO will oscillate at a lower frequency than the crystal specification. In either case, the absolute tuning range is reduced. The correct value of C_L is dependant on the characteristics of the VCXO. The recommended C_L in the *Crystal Parameter Table* balances the tuning range by centering the tuning curve.

The *VCXO-PLL Loop Bandwidth Selection Table* shows R_s, C_s and C_P values for recommended high, mid and low loop bandwidth configurations. The device has been characterized using these parameters. For other configurations, refer to the *Loop Filter Component Selection for VCXO Based PLLs Application Note.*

The crystal and external loop filter components should be kept as close as possible to the device. Loop filter and crystal traces should be kept short and separated from each other. Other signal traces should be kept separate and not run underneath the device, loop filter or crystal components.



VCXO Characteristics Table

Symbol	Parameter	Typical	Unit
k_{VCXO}	VCXO Gain	8000	Hz/V
C_{V_LOW}	Low Varactor Capacitance	8	pF
C_{V_HIGH}	High Varactor Capacitance	17	pF

VCXO-PLL Loop Bandwidth Selection Table

Bandwidth	Crystal Frequency (MHz)	R_S (kΩ)	C_S (µF)	C_P (µF)	R_{SET} (kΩ)
50Hz (Low)	25MHz	120	1.0	0.01	8.8
50Hz (Mid)	25MHz	221	0.1	0.001	2.21
150Hz (High)	25MHz	680	0.1	0.0001	2.21

Crystal Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Units
	Mode of Operation		Fundamental		
f_N	Frequency		25		MHz
f_T	Frequency Tolerance			±20	ppm
f_S	Frequency Stability			±20	ppm
	Operating Temperature Range	-40		85	°C
C_L	Load Capacitance		10		pF
C_O	Shunt Capacitance		4		pF
C_O/C_1	Pullability Ratio		220	240	
ESR	Equivalent Series Resistance			20	
	Drive Level			1	mW
	Aging @ 25°C			±3 per year	ppm

Reliability Information

Table 6A. θ_{JA} vs. Air Flow Table for 32 Lead VFQFN

θ_{JA} vs. 0 Air Flow (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	37.0°C/W	32.4°C/W	29.0°C/W

Table 6B. θ_{JA} vs. Air Flow Table for 32 Lead TQFP, E-Pad

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	32.2°C/W	26.3°C/W	24.7°C/W

Transistor Count

The transistor count for ICS810252I-03 is: 6597

PACKAGE OUTLINE - Y SUFFIX FOR 32 LEAD TQFP, E-PAD

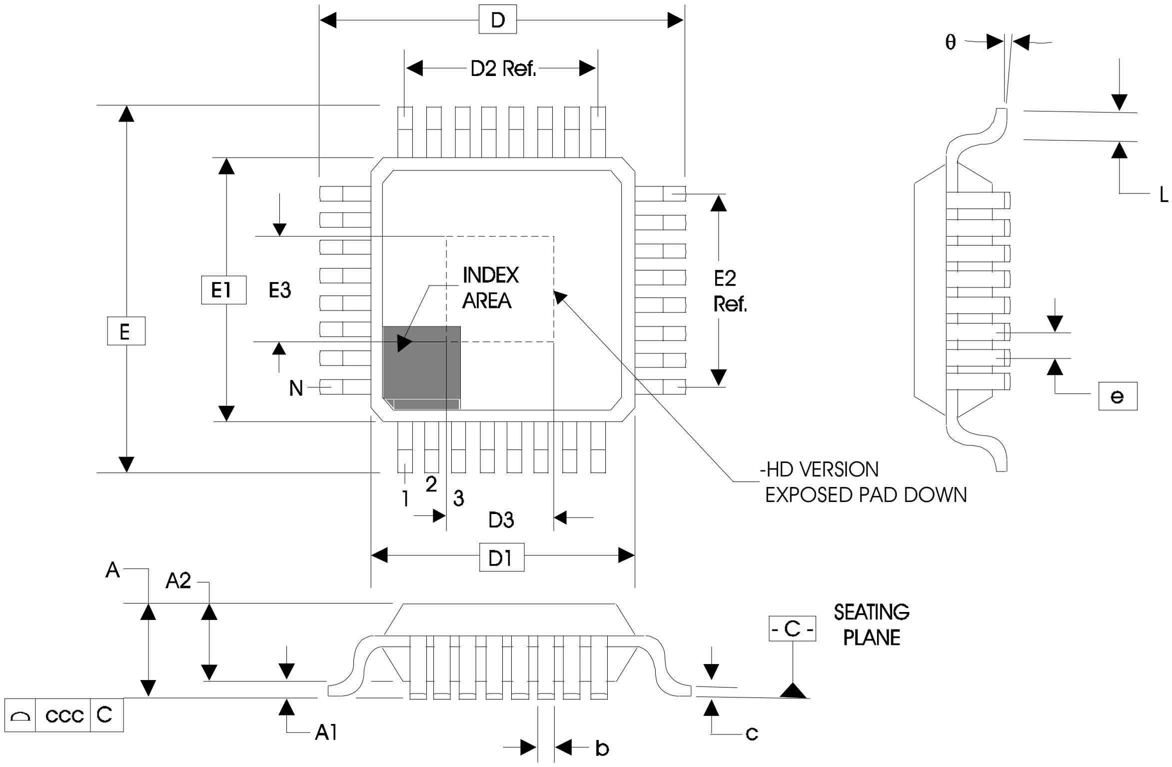
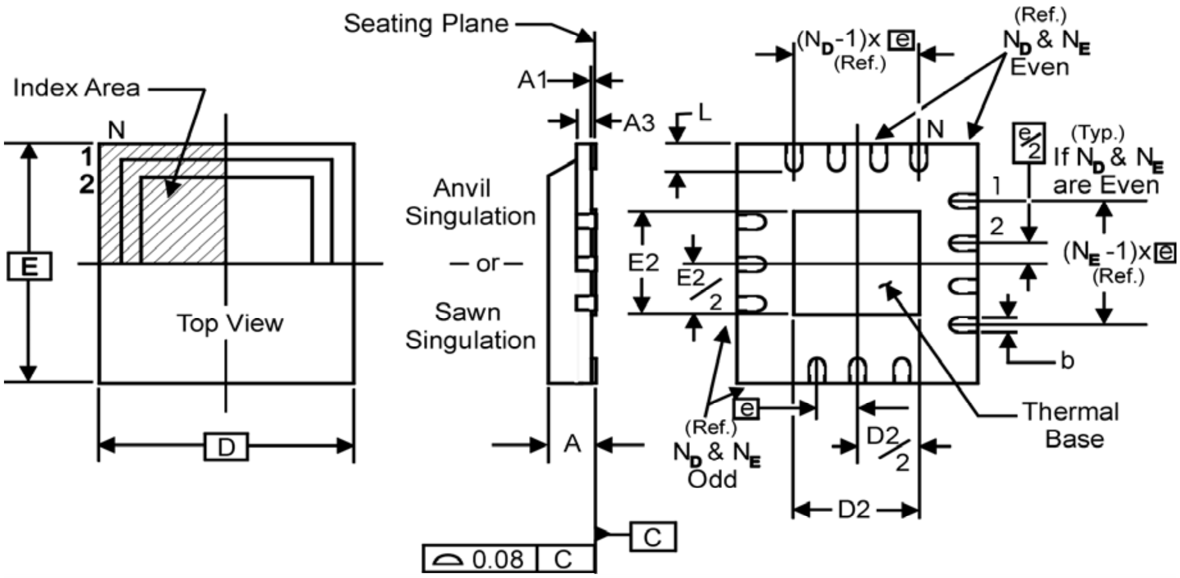


TABLE 7A. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	ABA-HD		
	MINIMUM	NOMINAL	MAXIMUM
N	32		
A	--	--	1.20
A1	0.05	0.10	0.15
A2	0.95	1.0	1.05
b	0.30	0.35	0.40
c	0.09	--	0.20
D, E	9.00 BASIC		
D1, E1	7.00 BASIC		
D2, E2	5.60 Ref.		
e	0.80 BASIC		
L	0.45		0.75
θ	0°	--	7°
ccc	--	--	0.10
D3 & D3	3.0	3.5	4.0

Reference Document: JEDEC Publication 95, MS-026

Package Outline and Dimensions - K Suffix for 32 Lead VFQFN



NOTE: The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this device. The pin count and pinout are shown on the front page. The package dimensions are in Table 7B below.

Table 7B. Package Dimensions

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	VHHD-2		
	MINIMUM	NOMINAL	MAXIMUM
N	32		
A	0.80	--	1.00
A1	0	--	0.05
A3	0.25 Ref.		
b	0.18	0.25	0.30
N_D			8
N_E			8
D	5.00 BASIC		
D2	1.25	2.25	3.25
E	5.00 BASIC		
E2	1.25	2.25	3.25
e	0.50 BASIC		
L	0.30	0.40	0.50

Reference Document: JEDEC Publication 95, MO-220

Table 8. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
810252AKI-03	ICS0252AI03	32 Lead VFQFN	tray	-40°C to 85°C
810252AKI-03T	ICS0252AI03	32 Lead VFQFN	2500 tape & reel	-40°C to 85°C
810252AKI-03LF	ICS252AI03L	32 Lead "Lead-Free" VFQFN	tray	-40°C to 85°C
810252AKI-03LFT	ICS252AI03L	32 Lead "Lead-Free" VFQFN	2500 tape & reel	-40°C to 85°C
810252AYI-03	TBD	32 lead TQFP, E-Pad	tray	-40°C to 85°C
810252AYI-03T	TBD	32 lead TQFP, E-Pad	1000 tape & reel	-40°C to 85°C
810252AYI-03LF	ICS0252AI03L	32 lead "Lead-Free" TQFP, E-Pad	tray	-40°C to 85°C
810252AYI-03LFT	ICS0252AI03L	32 lead "Lead-Free" TQFP, E-Pad	1000 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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