5.0 ELECTRICAL SPECIFICATIONS

5.1 Maximum Ratings

Table 14 is a stress rating only. Extended exposure to the Maximum Ratings may affect device reliability.

Furthermore, although the embedded ULP Intel486 GX processor contains protective circuitry to resist damage from electrostatic discharge, always take precautions to avoid high static voltages or electric fields.

Functional operating conditions are given in **Section 5.2, DC Specifications** and **Section 5.3, AC Specifications**.

Table 14. Absolute Maximum Ratings

Case Temperature under Bias	-65 °C to +110 °C
Storage Temperature	-65 °C to +150 °C
DC Voltage on Any Pin with Respect to Ground	-0.5 V to V_{CCP} + 0.5 V
Supply Voltage V_{CC} with Respect to V_{SS}	-0.5 V to +4.6 V
Supply Voltage V_{CCP} with Respect to V_{SS}	-0.5 V to +4.6 V

5.2 DC Specifications

The following tables show the operating supply voltages, DC I/O specifications, and component power consumption for the embedded ULP Intel486 GX processor.

Table 15. Operating Supply Voltages

Product	V_{CCP} Range[1]	Max. CLK Frequency	V_{CC} Range[2]	V_{CC} Fluctuation	
FA80486GXSF-33	3.3 V ± 0.3 V	16	2.0 V min 3.3 V max	±0.2 V +0.3 V/-0.2 V ±0.3 V	at 2.0 V ≤ V_{CC} ≤ 2.7 V at 2.7 V < V_{CC} < 3.0 V at 3.0 V ≤ V_{CC} ≤ 3.3 V
		20	2.2 V min 3.3 V max		
		25	2.4 V min 3.3 V max		
		33	2.7 V min 3.3 V max		

NOTES:

1. In all cases, V_{CCP} must be ≥ V_{CC}.
2. V_{CC} may be set to any voltage within the V_{CC} Range. The setting determines the allowed V_{CC} Fluctuation.

Table 16. DC Specifications

T_{CASE}=0 °C to +85 °C

Symbol	Parameter	Min.	Max.	Unit	Notes
V_{IL}	Input LOW Voltage	-0.3	+0.8	V	
V_{IH}	Input HIGH Voltage	2.0	V_{CCP} +0.3	V	Note 1
V_{IHC}	Input HIGH Voltage of CLK	V_{CCP} -0.6	V_{CCP} +0.3	V	
V_{OL}	Output LOW Voltage I_{OL} = 2.0 mA I_{OL} = 100 µA		 0.4 0.2	 V V	
V_{OH}	Output HIGH Voltage I_{OH} = -2.0 mA I_{OH} = -100 µA	 2.4 V_{CCP} -0.2		 V V	
I_{LI}	Input Leakage Current		±15	µA	Note 2
I_{IH}	Input Leakage Current		200	µA	Note 3
I_{IL}	Input Leakage Current		-400	µA	Note 4
I_{LO}	Output Leakage Current		±15	µA	
C_{IN}	Input Capacitance		10	pF	Note 5
C_{OUT}	I/O or Output Capacitance		10	pF	Note 5
C_{CLK}	CLK Capacitance		6	pF	Note 5

NOTES:

1. All inputs except CLK.
2. This parameter is for inputs without pull-up or pull-down resistors and $0V \le V_{IN} \le V_{CCP}$.
3. This parameter is for inputs with pull-down resistors and V_{IH} = 2.4V, and for level-keeper pins at V=0.4V.
4. This parameter is for inputs with pull-up resistors and V_{IL} = 0.4V, and for level-keeper pins at V=2.4V.
5. F_C=1 MHz. Not 100% tested.

Table 17. Active I_{CC} Values

T_{CASE}=0 °C to +85 °C

Symbol	Parameter	Frequency	Supply Voltage	Typical I_{CC}	Max. I_{CC}	Notes
I_{CC1}	I_{CC} Active (V_{CC} pins)	16 MHz	V_{CC} = 2.0 ± 0.2 V	65 mA	105 mA	
			V_{CC} = 3.3 ± 0.3 V	105 mA	170 mA	
		20 MHz	V_{CC} = 2.2 ± 0.2 V	85 mA	140 mA	
			V_{CC} = 3.3 ± 0.3 V	130 mA	210 mA	
		25 MHz	V_{CC} = 2.4 ± 0.2 V	120 mA	195 mA	
			V_{CC} = 3.3 ± 0.3 V	165 mA	260 mA	
		33 MHz	V_{CC} = 2.7 ± 0.2 V	180 mA	280 mA	
			V_{CC} = 3.3 ± 0.3 V	220 mA	345 mA	
I_{CC2}	I_{CC} Active (V_{CCP} pins)	16 MHz	V_{CCP} = 3.3 ± 0.3 V	5 mA	16 mA	1
		20 MHz	V_{CCP} = 3.3 ± 0.3 V	6 mA	20 mA	1
		25 MHz	V_{CCP} = 3.3 ± 0.3 V	7 mA	25 mA	1
		33 MHz	V_{CCP} = 3.3 ± 0.3 V	9 mA	32 mA	1

NOTE:

1. These parameters are for C_L = 50 pF

Table 18. Clock Stop, Stop Grant, and Auto HALT Power Down I_{CC} Values

T_{CASE}= 0 °C to +85 °C

Symbol	Parameter	Frequency	Supply Voltage	Typical I_{CC}	Max. I_{CC}	Notes
I_{CCS0}	I_{CC} Stop Clock (V_{CC} pins)	0 MHz	V_{CC} = 2.0 ± 0.2 V	3 µA	105 µA	Note 1
			V_{CC} = 2.2 ± 0.2 V	3 µA	110 µA	
			V_{CC} = 2.4 ± 0.2 V	4 µA	120 µA	
			V_{CC} = 2.7 ± 0.2 V	4 µA	130 µA	
			V_{CC} = 3.3 ± 0.3 V	5 µA	150 µA	
I_{CCS2}	I_{CC} Stop Clock (V_{CCP} pins)	0 MHz	V_{CCP} = 3.3 ± 0.3 V	3 µA	80 µA	
I_{CCS1}	I_{CC} Stop Grant, Auto HALT Power Down (V_{CC} pins)	16 MHz	V_{CC} = 2.0 ± 0.2 V	8 mA	15 mA	
			V_{CC} = 3.3 ± 0.3 V	12 mA	20 mA	
		20 MHz	V_{CC} = 2.2 ± 0.2 V	10 mA	20 mA	
			V_{CC} = 3.3 ± 0.3 V	15 mA	25 mA	
		25 MHz	V_{CC} = 2.4 ± 0.2 V	14 mA	25 mA	
			V_{CC} = 3.3 ± 0.3 V	20 mA	30 mA	
		33 MHz	V_{CC} = 2.7 ± 0.2 V	20 mA	30 mA	
			V_{CC} = 3.3 ± 0.3 V	25 mA	35 mA	
I_{CCS3}	I_{CC} Stop Grant, Auto HALT Power Down (V_{CCP} pins)	16 MHz	V_{CCP} = 3.3 ± 0.3 V	270 µA	1.0 mA	
		20 MHz	V_{CCP} = 3.3 ± 0.3 V	340 µA	1.2 mA	
		25 MHz	V_{CCP} = 3.3 ± 0.3 V	425 µA	1.5 mA	
		33 MHz	V_{CCP} = 3.3 ± 0.3 V	610 µA	2.0 mA	

NOTE:

1. The I_{CC} Stop Clock specification refers to the I_{CC} value once the processor enters the Stop Clock state. For all input signals, the V_{IH} and V_{IL} levels must be equal to V_{CCP} and 0V, respectively, to meet the I_{CC} Stop Clock specifications.

5.3 AC Specifications

The AC specifications for the embedded ULP Intel486 GX processor are given in this section.

Table 19. AC Characteristics (Sheet 1 of 2)

valid over the operating supply voltages listed in Table 15, Operating Supply Voltages (pg. 30).
T_{CASE}= 0 °C to +85 °C; C_L= 50 pF

Symbol	Parameter	2.0V ≤ V_{CC} < 2.2V		2.2V ≤ V_{CC} < 2.4V		2.4V ≤ V_{CC} < 2.7V		2.7V ≤ V_{CC} ≤ 3.3V		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
	Frequency	0	16	0	20	0	25	0	33	MHz	Note 1
t_1	CLK Period	62.5		50		40		30		ns	Note 1
t_{1a}	CLK Period Stability		250		250		250		250	ps/CLK	Note 2
t_2	CLK High Time	23		18		14		11		ns	at 2V
t_3	CLK Low Time	23		18		14		11		ns	at 0.8V
t_4	CLK Fall Time		4		4		4		3	ns	2V to 0.8V Note 3
t_5	CLK Rise Time		4		4		4		3	ns	0.8V to 2V Note 3
t_6	A2-A31, PWT, PCD, BE0#-BE3#, M/IO#, D/C#, W/R#, ADS#, LOCK#, BREQ, HLDA, SMIACT# Valid Delay	3	30	3	24	3	19	3	16	ns	
t_7	A2-A31, PWT, PCD, BE0#-BE3#, M/IO#, D/C#, W/R#, ADS#, LOCK#, BREQ, Float Delay		36		30		28		20	ns	Note 3
t_8	PCHK# Valid Delay	3	34	3	29	3	24	3	22	ns	
t_{8a}	BLAST#, PLOCK# Valid Delay	3	34	3	29	3	24	3	20	ns	
t_9	BLAST#, PLOCK# Float Delay		36		30		28		20	ns	Note 3
t_{10}	D0-D15, DP0, DP1 Write Delay	3	31	3	26	3	20	3	19	ns	
t_{11}	D0-D15, DP0, DP1 Float Delay		36		30		28		20	ns	Note 3
t_{12}	EADS# Setup Time	13		11		8		6		ns	
t_{13}	EADS# Hold Time	4		4		3		3		ns	
t_{14}	KEN# Setup Time	13		11		8		6		ns	
t_{15}	KEN# Hold Time	4		4		3		3		ns	
t_{16}	RDY#, BRDY# Setup Time	13		11		8		6		ns	
t_{17}	RDY#, BRDY# Hold Time	4		4		3		3		ns	
t_{18}	HOLD, AHOLD Setup Time	15		13		10		6		ns	

Table 19. AC Characteristics (Sheet 2 of 2)

valid over the operating supply voltages listed in Table 15, Operating Supply Voltages (pg. 30).
T_{CASE}= 0 °C to +85 °C; C_L= 50 pF

Symbol	Parameter	2.0V ≤ V_{CC} < 2.2V		2.2V ≤ V_{CC} < 2.4V		2.4V ≤ V_{CC} < 2.7V		2.7V ≤ V_{CC} ≤ 3.3V		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
t_{18a}	BOFF# Setup Time	15		13		10		9		ns	
t_{19}	HOLD, AHOLD, BOFF# Hold Time	4		4		3		3		ns	
t_{20}	FLUSH#, A20M#, NMI, INTR, SMI#, STPCLK#, SRESET, RESET Setup Time	15		13		10		6		ns	
t_{21}	FLUSH#, A20M#, NMI, INTR, SMI#, STPCLK#, SRESET, RESET Hold Time	4		4		3		3		ns	
t_{22}	D0-D15, DP0, DP1, A4-A31 Read Setup Time	11		8		6		6		ns	
t_{23}	D0-D15, DP0, DP1, A4-A31 Read Hold Time	4		4		3		3		ns	

NOTES:

1. 0 Hz operation is tested and guaranteed by the STPCLK# and Stop Grant bus cycle protocol. 0 Hz < CLK < 8 MHz operation is confirmed by design characterization, but not 100% tested in production.
2. Specification t1a is available only when CLK frequency is changed without STPCLK# / STOP GRANT bus cycle protocol.
3. Not 100% tested, guaranteed by design characterization.
4. CLK reference voltage for timing measurement is 1.5 V except t2 through t5. Other signals are measured at 1.5 V.

Table 20. AC Specifications for the Test Access Port

Symbol	Parameter	1.8 V ≤ Vcc < 3.0 V		Vcc = 3.3 ± 0.3 V		Unit	Figure	Notes
		Min	Max	Min	Max			
t_{24}	TCK Frequency		5		8	MHz	15	
t_{25}	TCK Period	200		125		ns	15	Note 1
t_{26}	TCK High Time	65		40		ns	15	@ 2.0V
t_{27}	TCK Low Time	65		40		ns	15	@0.8V
t_{28}	TCK Rise Time		15		8	ns	15	Note 2
t_{29}	TCK Fall Time		15		8	ns	15	Note 2
t_{30}	TDI, TMS Setup Time	16		8		ns	16	Note 3
t_{31}	TDI, TMS Hold Time	20		10		ns	16	Note 3
t_{32}	TDO Valid Delay	3	46	3	30	ns	16	Note 3
t_{33}	TDO Float Delay		52		36	ns	16	Notes 3, 4
t_{34}	All Outputs (except TDO) Valid Delay	3	80	3	30	ns	16	Note 3
t_{35}	All Outputs (except TDO) Float Delay		88		36	ns	16	Notes 3, 4
t_{36}	All Inputs (except TDI, TMS, TCK) Setup Time	16		8		ns	16	Note 3
t_{37}	All Inputs (except TDI, TMS, TCK) Hold Time	35		15		ns	16	Note 3

NOTES:

1. TCK period ≥ CLK period.
2. Rise/Fall Times are measured between 0.8 V and 2.0 V. Rise/Fall times can be relaxed by 1 ns per 10 ns increase in TCK period.
3. Parameter measured from TCK.
4. Not 100% tested, guaranteed by design characterization.

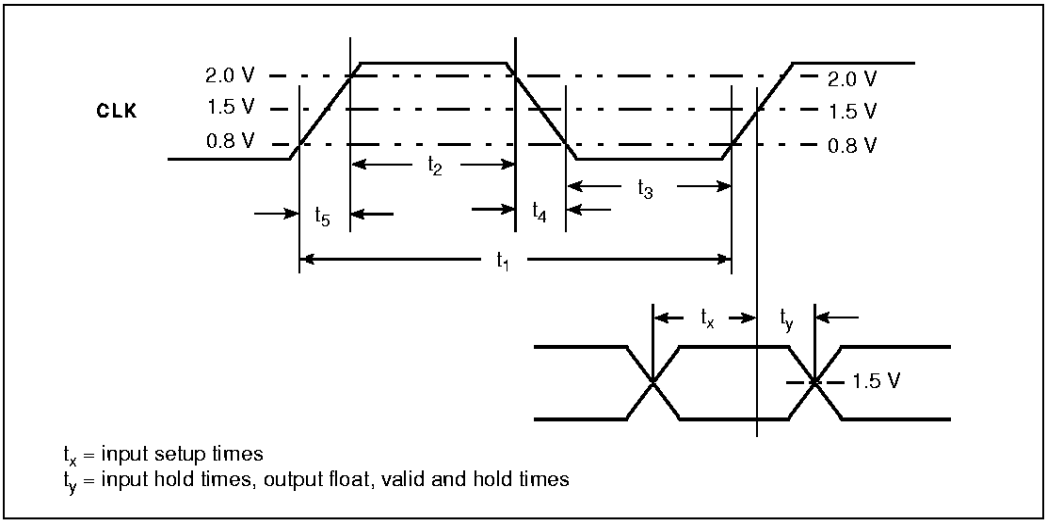


Figure 9. CLK Waveform

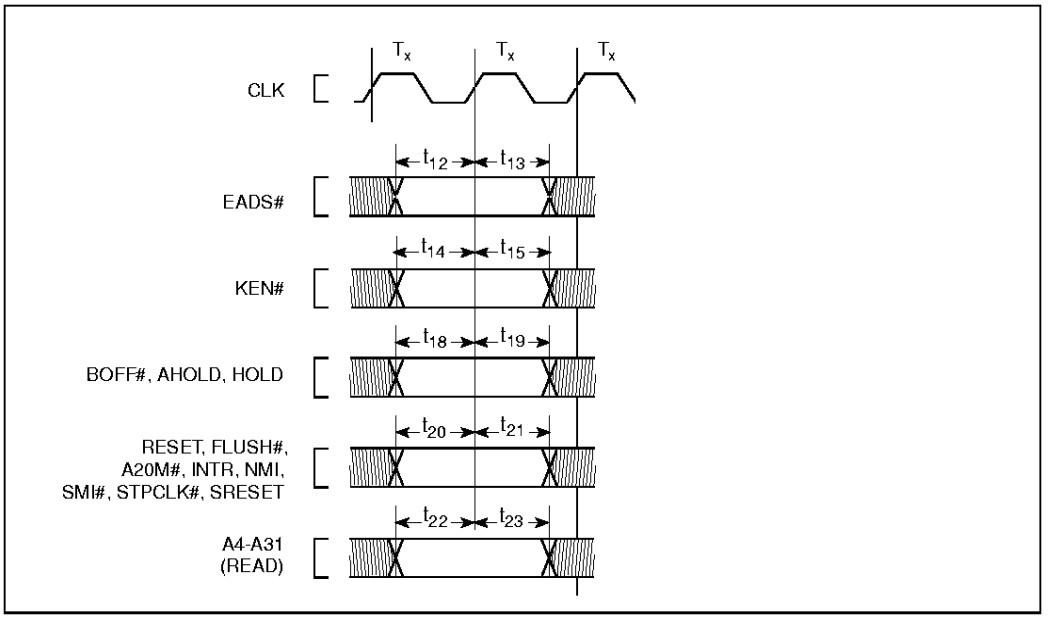


Figure 10. Input Setup and Hold Timing

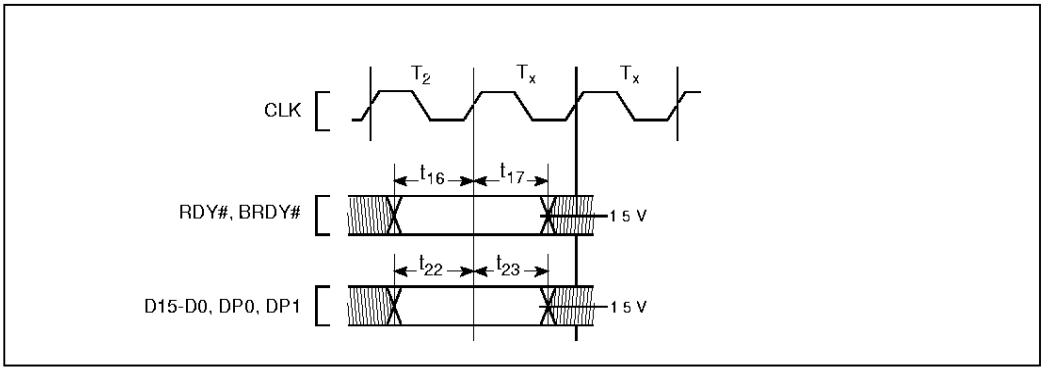


Figure 11. Input Setup and Hold Timing

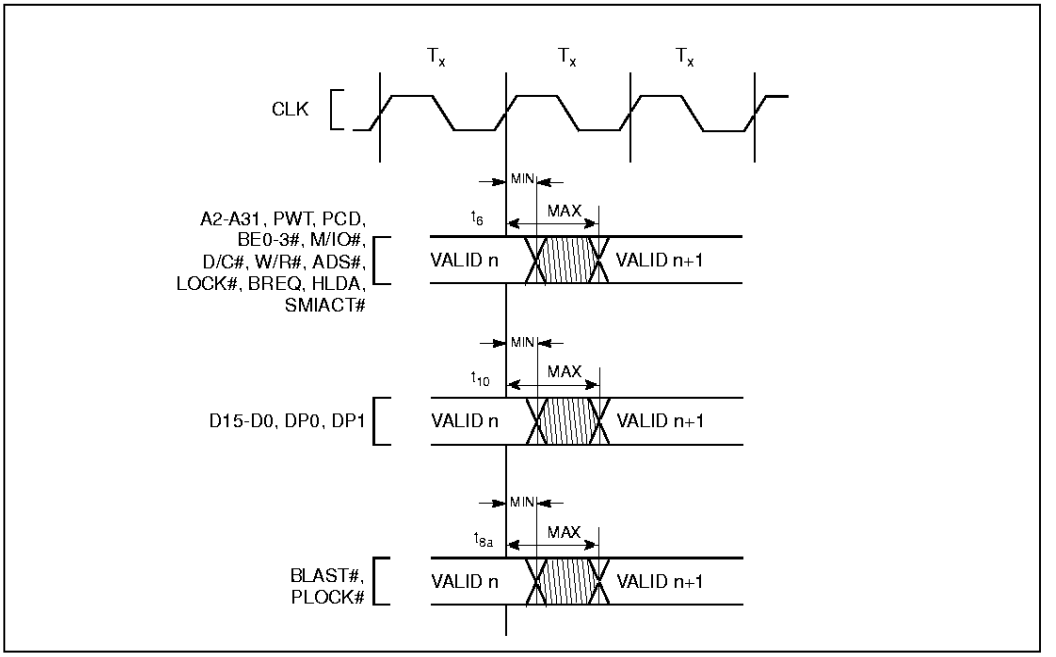


Figure 12. Output Valid Delay Timing

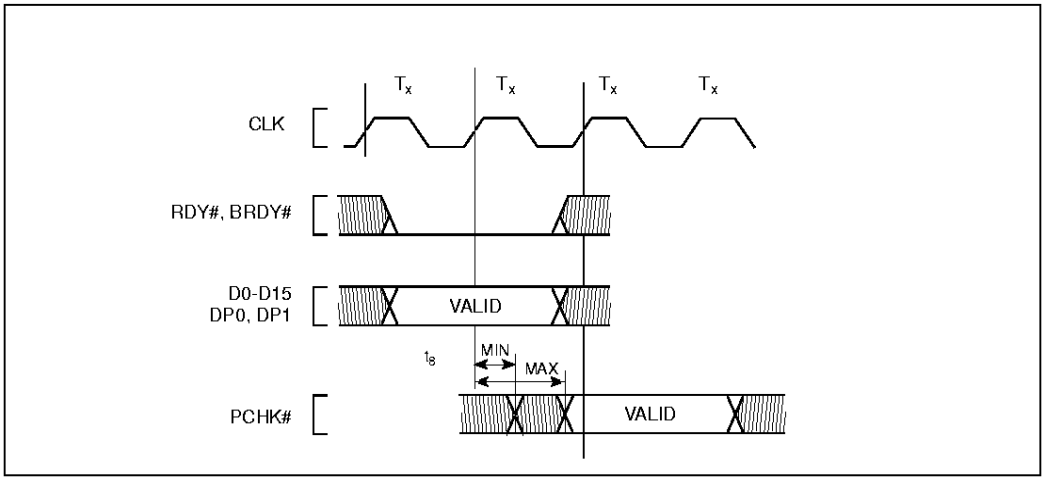


Figure 13. PCHK# Valid Delay Timing

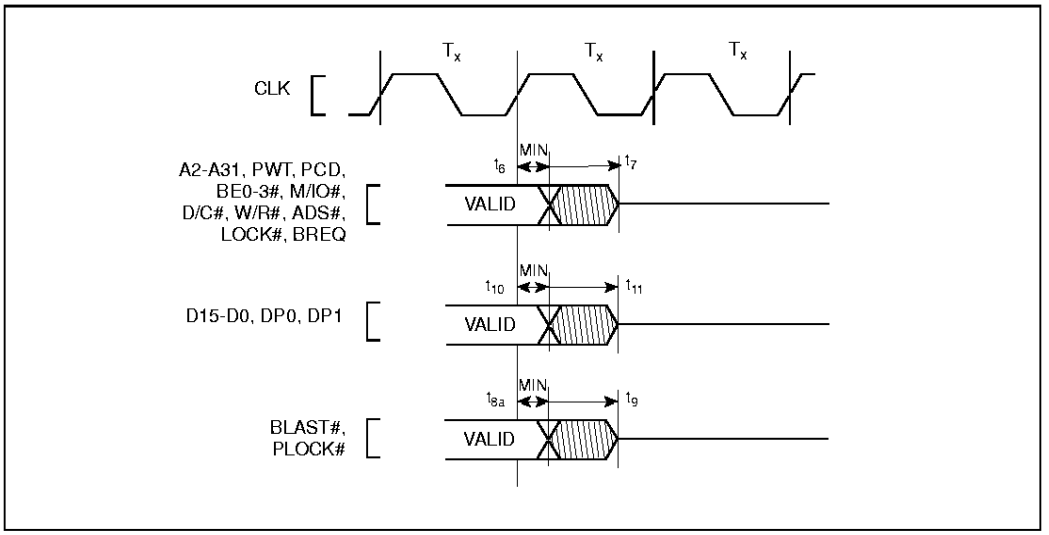


Figure 14. Maximum Float Delay Timing

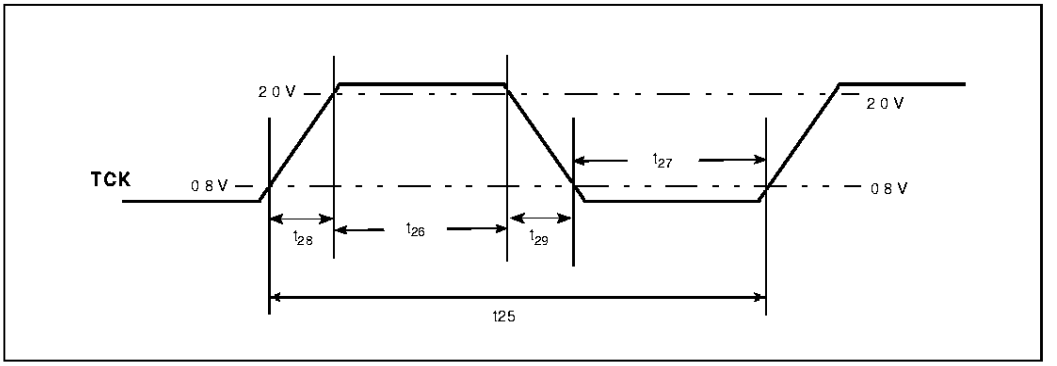


Figure 15. TCK Waveform

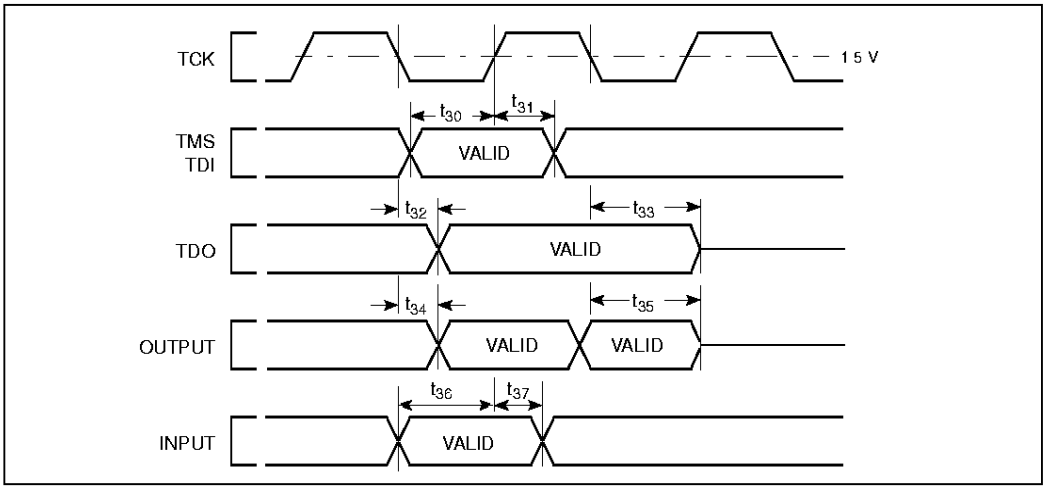
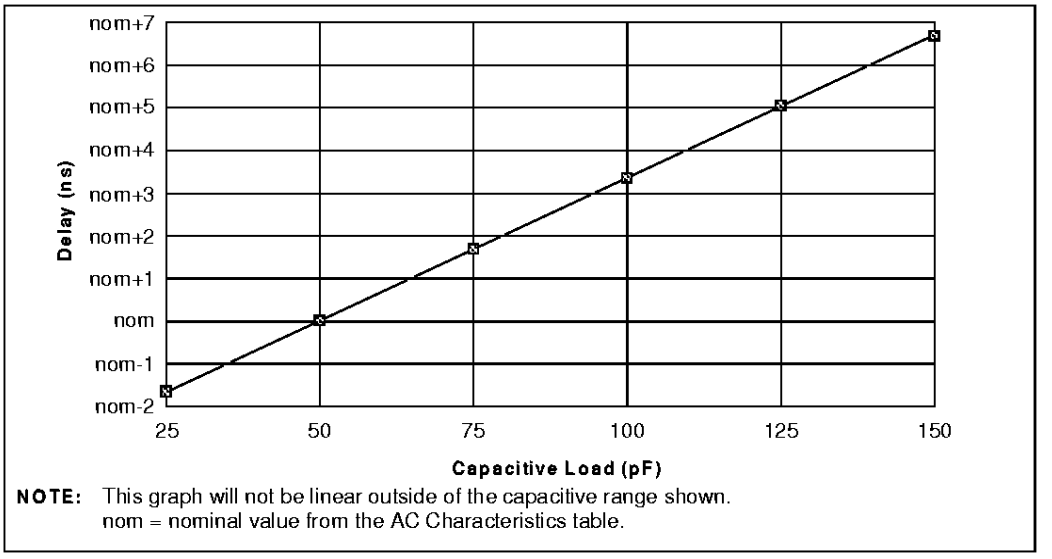


Figure 16. Test Signal Timing Diagram

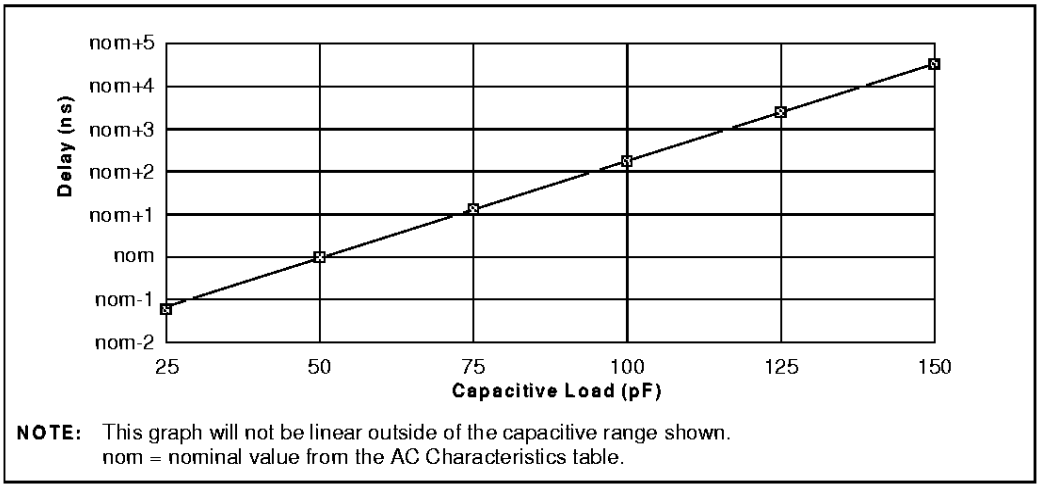
5.4 Capacitive Derating Curves

The following graphs are the capacitive derating curves for the embedded ULP Intel486 GX processor.



NOTE: This graph will not be linear outside of the capacitive range shown.
nom = nominal value from the AC Characteristics table.

Figure 17. Typical Loading Delay versus Load Capacitance under Worst-Case Conditions for a Low-to-High Transition



NOTE: This graph will not be linear outside of the capacitive range shown.
nom = nominal value from the AC Characteristics table.

Figure 18. Typical Loading Delay versus Load Capacitance under Worst-Case Conditions for a High-to-Low Transition