This is an abbreviated datasheet. Contact a Cypress representative for complete specifications.

CYPRESS SEMICONDUCTOR

CYM1423

128K x 8 Static RAM Module

Features

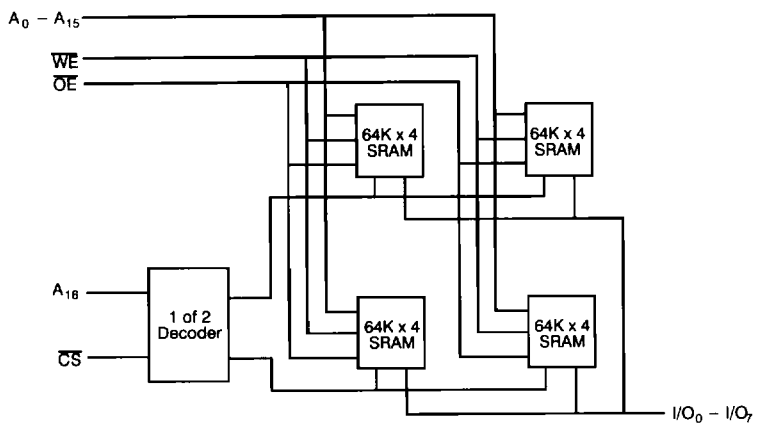
- **High-density 1-megabit SRAM module**
- **High-speed CMOS SRAMs**
  - **Access time of 45 ns**
- **32-pin, 0.6-inch-wide DIP package**
- **JEDEC-compatible pinout**
- **Low active power**
  - **1.2W (max.)**
- **SMD technology**
- **TTL-compatible inputs and outputs**
- **Commercial temperature range**
- **Small PCB footprint**
  - **1.1 sq. in.**

Functional Description

The CYM1423 is a high-performance 1-megabit static RAM module organized as 128K words by 8 bits. This module is constructed using four 64K x 4 static RAMs in SOJ packages mounted onto an epoxy laminate board with pins. A decoder is used to interpret the higher-order address and select two of the four RAMs.

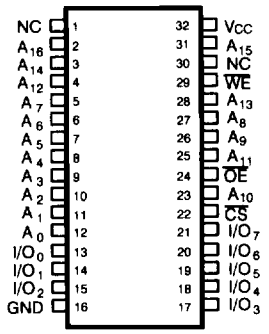
Writing to the module is accomplished when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the eight input/output pins (I/O_0 through I/O_7) of the device is written into the memory location specified on the address pins (A_0 through A_{16}). Reading the device is accomplished by taking chip select ($\overline{CS}$) and output enable ($\overline{OE}$) LOW, while write enable ($\overline{WE}$) remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins (A_0 through A_{16}) will appear on the eight input/output pins (I/O_0 through I/O_7). The input/output pins remain in a high-impedance state unless the module is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH.

Logic Block Diagram



Pin Configuration

DIP
Top View



Selection Guide

	1423–45	1423–55	1423–70
Maximum Access Time (ns)	45	55	70
Maximum Operating Current (mA)	210	210	210
Maximum Standby Current (mA)	80	80	80