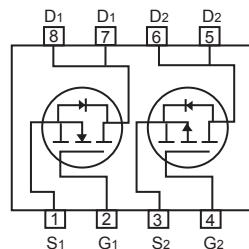
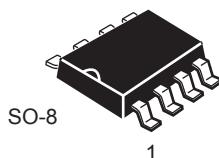


## Dual Enhancement Mode Field Effect Transistor (N and P Channel)

### FEATURES

- 40V, 6.1A,  $R_{DS(ON)} = 32m\Omega$  @ $V_{GS} = 10V$ .  
 $R_{DS(ON)} = 46m\Omega$  @ $V_{GS} = 4.5V$ .
- -40V, -5.2A,  $R_{DS(ON)} = 43m\Omega$  @ $V_{GS} = 10V$ .  
 $R_{DS(ON)} = 65m\Omega$  @ $V_{GS} = 4.5V$ .
- Super high dense cell design for extremely low  $R_{DS(ON)}$ .
- High power and current handing capability.
- Lead free product is acquired.
- Surface mount Package.



### ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ C$ unless otherwise noted

Parameter	Symbol	Channel 1	Channel 2	Units
Drain-Source Voltage	$V_{DS}$	40	-40	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	$\pm 20$	V
Drain Current-Continuous	$I_D$	6.1	-5.2	A
		4.9	-4.2	
Drain Current-Pulsed <sup>a</sup>	$I_{DM}$	20	-20	
Maximum Power Dissipation	$P_D$	2.0		W
		1.28		
Operating and Store Temperature Range	$T_J, T_{stg}$	-55 to 150		°C

### Thermal Characteristics

Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Ambient <sup>b</sup>	$R_{\theta JA}$	62.5	°C/W



CEM4269

**N-Channel Electrical Characteristics**  $T_A = 25^\circ\text{C}$  unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$\text{BV}_{\text{DSS}}$	$V_{\text{GS}} = 0\text{V}, I_D = 250\mu\text{A}$	40			V
Zero Gate Voltage Drain Current	$I_{\text{DSS}}$	$V_{\text{DS}} = 40\text{V}, V_{\text{GS}} = 0\text{V}$		1		$\mu\text{A}$
Gate Body Leakage Current, Forward	$I_{\text{GSSF}}$	$V_{\text{GS}} = 20\text{V}, V_{\text{DS}} = 0\text{V}$		100		nA
Gate Body Leakage Current, Reverse	$I_{\text{GSSR}}$	$V_{\text{GS}} = -20\text{V}, V_{\text{DS}} = 0\text{V}$		-100		nA
<b>On Characteristics</b> <sup>c</sup>						
Gate Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{GS}} = V_{\text{DS}}, I_D = 250\mu\text{A}$	1		3	V
Static Drain-Source On-Resistance	$R_{\text{DS}(\text{on})}$	$V_{\text{GS}} = 10\text{V}, I_D = 6\text{A}$		32		$\text{m}\Omega$
		$V_{\text{GS}} = 4.5\text{V}, I_D = 5\text{A}$		46		$\text{m}\Omega$
Forward Transconductance	$g_{\text{FS}}$	$V_{\text{DS}} = 5\text{V}, I_D = 6\text{A}$		3		S
<b>Dynamic Characteristics</b> <sup>d</sup>						
Input Capacitance	$C_{\text{iss}}$	$V_{\text{DS}} = 20\text{V}, V_{\text{GS}} = 0\text{V}, f = 1.0 \text{ MHz}$		1050		pF
Output Capacitance	$C_{\text{oss}}$			155		pF
Reverse Transfer Capacitance	$C_{\text{rss}}$			95		pF
<b>Switching Characteristics</b> <sup>d</sup>						
Turn-On Delay Time	$t_{\text{d}(\text{on})}$	$V_{\text{DD}} = 20\text{V}, I_D = 6\text{A}, V_{\text{GS}} = 10\text{V}, R_{\text{GEN}} = 3\Omega$		14	30	ns
Turn-On Rise Time	$t_r$			10	20	ns
Turn-Off Delay Time	$t_{\text{d}(\text{off})}$			17	35	ns
Turn-Off Fall Time	$t_f$			18	35	ns
Total Gate Charge	$Q_g$	$V_{\text{DS}} = 20\text{V}, I_D = 6\text{A}, V_{\text{GS}} = 10\text{V}$		20.5	27	nC
Gate-Source Charge	$Q_{\text{gs}}$			3.5		nC
Gate-Drain Charge	$Q_{\text{gd}}$			4.0		nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
Drain-Source Diode Forward Current <sup>b</sup>	$I_S$				1.0	A
Drain-Source Diode Forward Voltage <sup>c</sup>	$V_{\text{SD}}$	$V_{\text{GS}} = 0\text{V}, I_S = 1.0\text{A}$			1.0	V

## Notes :

- a.Repetitive Rating : Pulse width limited by maximum junction temperature.
- b.Surface Mounted on FR4 Board, t ≤ 10 sec.
- c.Pulse Test : Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
- d.Guaranteed by design, not subject to production testing.



CEM4269

**P-Channel Electrical Characteristics**  $T_A = 25^\circ\text{C}$  unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$\text{BV}_{\text{DSS}}$	$V_{\text{GS}} = 0\text{V}, I_D = -250\mu\text{A}$	-40			V
Zero Gate Voltage Drain Current	$I_{\text{DSS}}$	$V_{\text{DS}} = -40\text{V}, V_{\text{GS}} = 0\text{V}$			-1	$\mu\text{A}$
Gate Body Leakage Current, Forward	$I_{\text{GSSF}}$	$V_{\text{GS}} = 20\text{V}, V_{\text{DS}} = 0\text{V}$			100	nA
Gate Body Leakage Current, Reverse	$I_{\text{GSSR}}$	$V_{\text{GS}} = -20\text{V}, V_{\text{DS}} = 0\text{V}$			-100	nA
<b>On Characteristics</b> <sup>c</sup>						
Gate Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{GS}} = V_{\text{DS}}, I_D = -250\mu\text{A}$	-1		-3	V
Static Drain-Source On-Resistance	$R_{\text{DS}(\text{on})}$	$V_{\text{GS}} = -10\text{V}, I_D = -5\text{A}$			43	$\text{m}\Omega$
		$V_{\text{GS}} = -4.5\text{V}, I_D = -2\text{A}$			65	$\text{m}\Omega$
Forward Transconductance	$g_{\text{FS}}$	$V_{\text{DS}} = -5\text{V}, I_D = -4.8\text{A}$		3		S
<b>Dynamic Characteristics</b> <sup>d</sup>						
Input Capacitance	$C_{\text{iss}}$	$V_{\text{DS}} = -20\text{V}, V_{\text{GS}} = 0\text{V}, f = 1.0 \text{ MHz}$		1125		pF
Output Capacitance	$C_{\text{oss}}$			150		pF
Reverse Transfer Capacitance	$C_{\text{rss}}$			100		pF
<b>Switching Characteristics</b> <sup>d</sup>						
Turn-On Delay Time	$t_{\text{d}(\text{on})}$	$V_{\text{DD}} = -20\text{V}, I_D = -5\text{A}, V_{\text{GS}} = -10\text{V}, R_{\text{GEN}} = 3\Omega$		12	24	ns
Turn-On Rise Time	$t_r$			5	30	ns
Turn-Off Delay Time	$t_{\text{d}(\text{off})}$			33	66	ns
Turn-Off Fall Time	$t_f$			4	8	ns
Total Gate Charge	$Q_g$	$V_{\text{DS}} = -20\text{V}, I_D = -5\text{A}, V_{\text{GS}} = -10\text{V}$		20	26	nC
Gate-Source Charge	$Q_{\text{gs}}$			2.5		nC
Gate-Drain Charge	$Q_{\text{gd}}$			3.5		nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
Drain-Source Diode Forward Current <sup>b</sup>	$I_S$				-1.0	A
Drain-Source Diode Forward Voltage <sup>c</sup>	$V_{\text{SD}}$	$V_{\text{GS}} = 0\text{V}, I_S = -1.0\text{A}$			-1.0	V

## Notes :

- a.Repetitive Rating : Pulse width limited by maximum junction temperature.
- b.Surface Mounted on FR4 Board, t ≤ 10 sec.
- c.Pulse Test : Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
- d.Guaranteed by design, not subject to production testing.

## N-CHANNEL

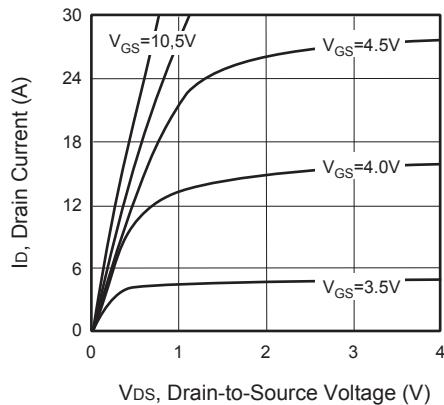


Figure 1. Output Characteristics

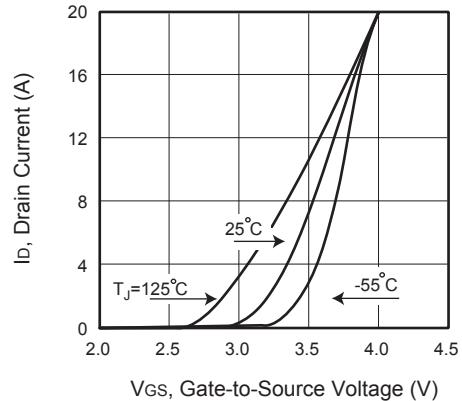


Figure 2. Transfer Characteristics

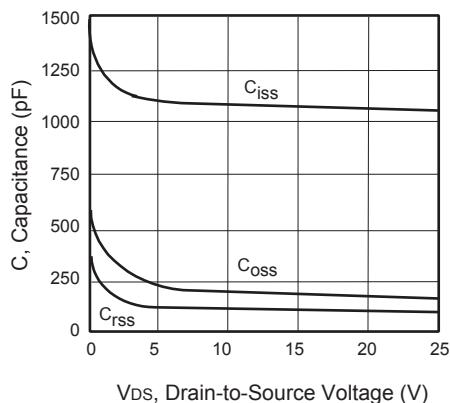


Figure 3. Capacitance

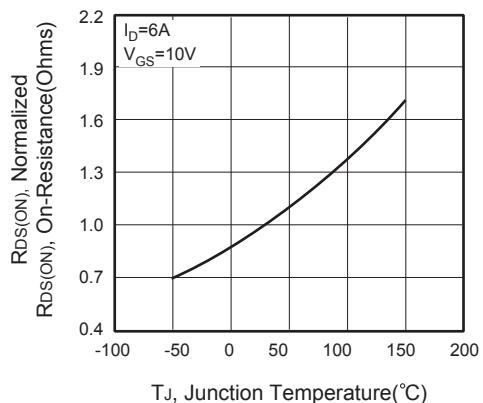


Figure 4. On-Resistance Variation with Temperature

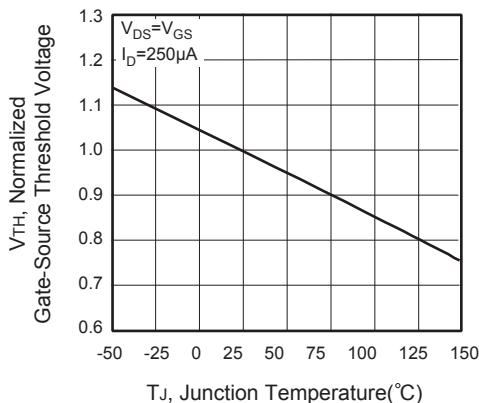


Figure 5. Gate Threshold Variation with Temperature

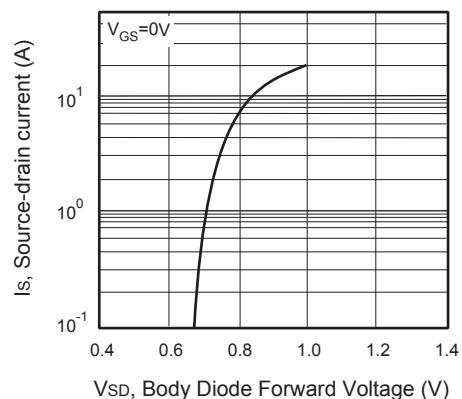


Figure 6. Body Diode Forward Voltage Variation with Source Current

## P-CHANNEL

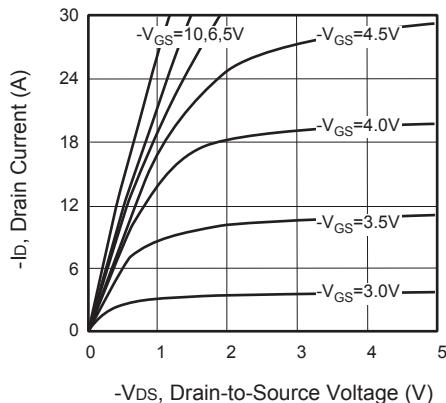


Figure 7. Output Characteristics

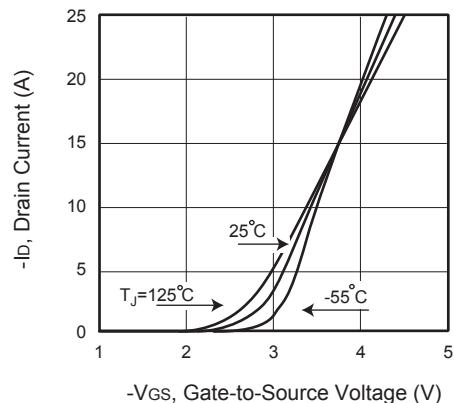


Figure 8. Transfer Characteristics

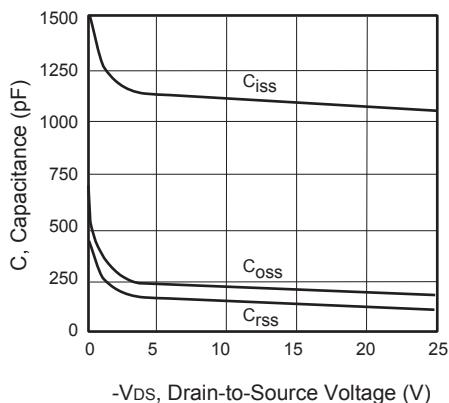


Figure 9. Capacitance

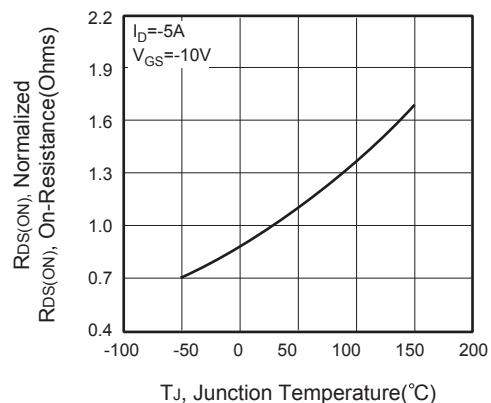


Figure 10. On-Resistance Variation with Temperature

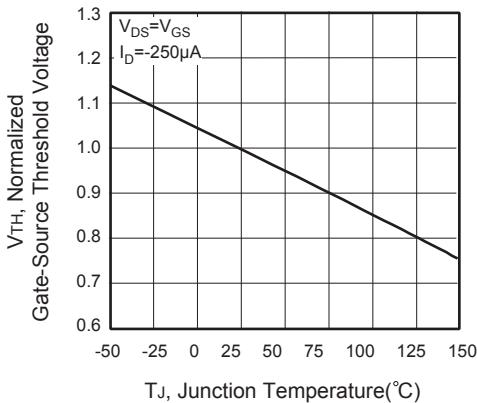


Figure 11. Gate Threshold Variation with Temperature

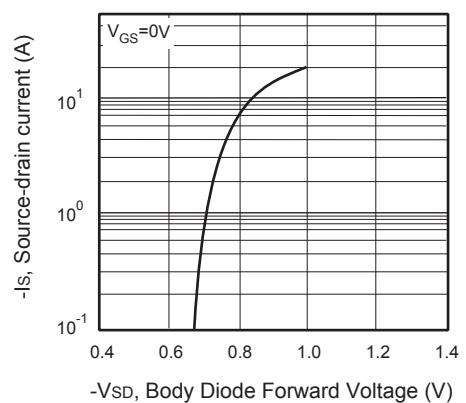
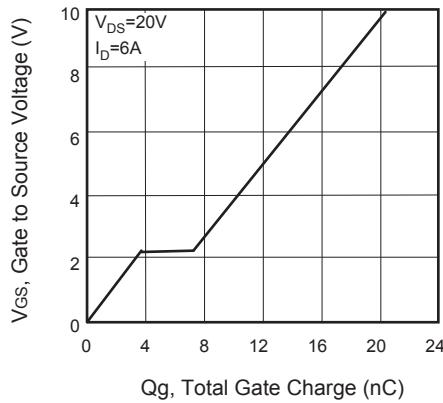
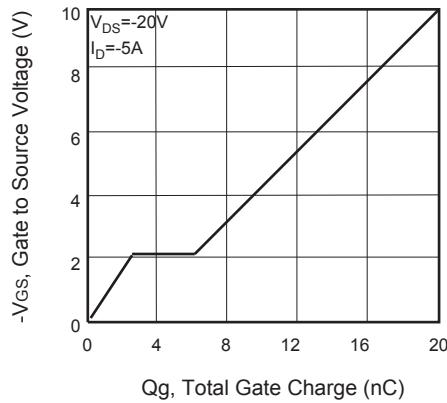
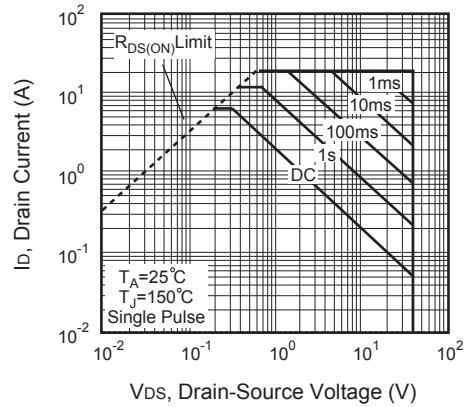
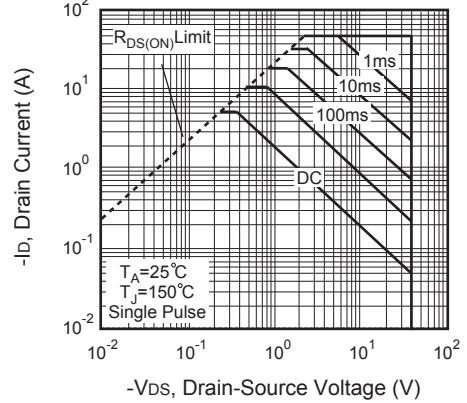


Figure 12. Body Diode Forward Voltage Variation with Source Current

**N-CHANNEL**

**Figure 13. Gate Charge**
**P-CHANNEL**

**Figure 15. Gate Charge**

**Figure 14. Maximum Safe Operating Area**

**Figure 16. Maximum Safe Operating Area**

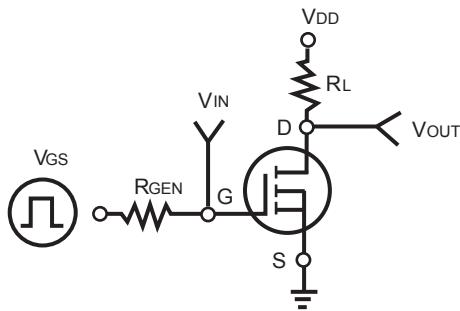


Figure 17. Switching Test Circuit

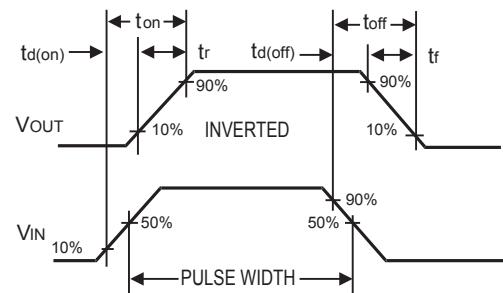


Figure 18. Switching Waveforms

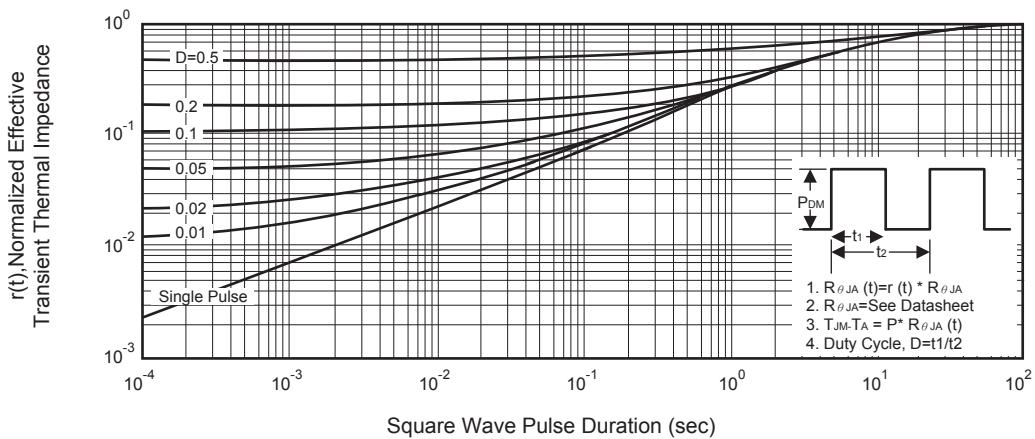


Figure 19. Normalized Thermal Transient Impedance Curve