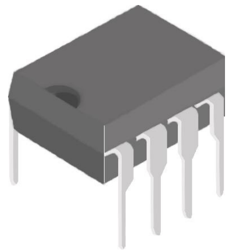
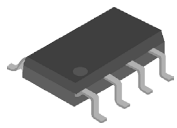
# DC to DC Converter Controller

## FEATURES

- operation from 3.0 to 40V input
- short circuit current limiting
- low standby current
- output switch current of 1.5A
- output voltage adjustable
- frequency of operation from 100Hz to 100KHz
- step-up, step-down or inverting switching regulators
- current limiting



DIP-8



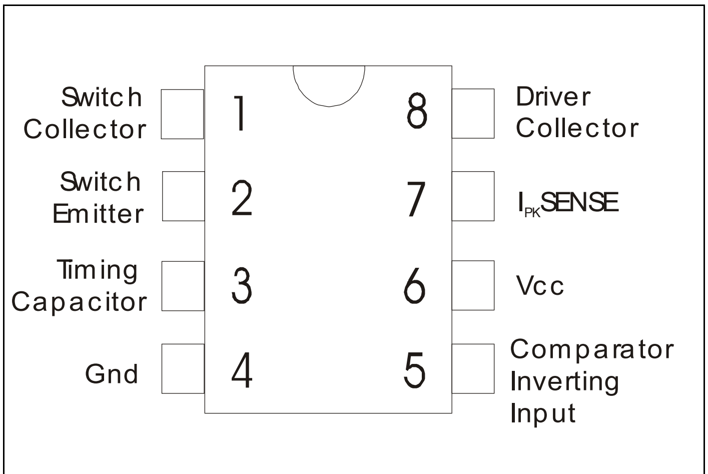
SOP-8

## PRODUCT DESCRIPTION

The SM34063 is a monolithic control circuit containing the primary functions required for DC-to-DC converters. This device consists of an internal temperature compensated reference, comparator, controlled duty cycle oscillator with an active current limit circuit, driver and high current output switch.

This device was specifically designed to be incorporated in Step-Down and Step-Up and Voltage-inverting applications with a minimum number of external components.

## PIN CONFIGURATION




## ORDERING INFORMATION

| Part Number | Operating Temperature Range | Package Type |
|---|---|---|
| SM34063N | 0℃~+70℃ | DIP-8 |
| SM34063M | 0℃~+70℃ | SOP-8 |

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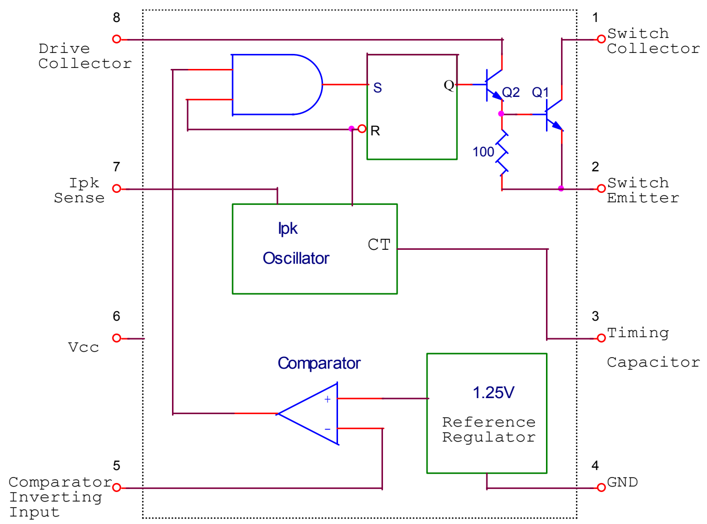
## ABSOLUTE MAXIMUM RATING

| Characteristic | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | 40 | V |
| Comparator Input Voltage Range | $V_{IR}$ | -0.3 to +40 | V |
| Switch Collector Voltage | $V_{C(switch)}$ | 40 | V |
| Switch Emitter Voltage ($V_{Pin\ 1}$=40V) | $V_{E(switch)}$ | 40 | V |
| Switch Collector to Emitter Voltage | $V_{CE(switch)}$ | 40 | V |
| Driver Collector Voltage | $V_{C(driver)}$ | 40 | V |
| Driver Collector Current (Note 1) | $I_{C(driver)}$ | 100 | mA |
| Switch Current | $I_{SW}$ | 1.5 | A |
| Power Dissipation and Thermal Characteristics | | | |
| Plastic Package $T_A$=25℃ | $P_D$ | 1.25 | W |
| Thermal Resistance | $R_{\theta JA}$ | 100 | ℃/W |
| SOIC Package $T_A$=25℃ | $P_D$ | 0.625 | W |
| Thermal Resistance | $R_{\theta JA}$ | 100 | ℃/W |
| Operating Junction Temperature | $T_J$ | +150 | ℃ |
| Operating Ambient Temperature Range | $T_A$ | 0 to +70 | ℃ |
| Storage Temperature Range | $T_{stg}$ | -65 to +150 | ℃ |

NOTES: 1. Maximum package power dissipation limits must be observed. 2. ESD data available upon request.

## BLOCK DIAGRAM



## ELECTRICAL CHARACTETRISTICS ($V_{CC}$=5.0V, $T_A$=$T_{low}$ to $T_{high}$ [Note1], unless otherwise specified.)

| Characteristics | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **OSCILLATOR** | | | | | |
| Frequency($V_{Pin\ 5}$=0V, $C_T$=1.0nF, $T_A$=25℃) | $f_{OSC}$ | 24 | 33 | 42 | kHz |
| Charge Current ($V_{CC}$=5.0V to 40V, $T_A$=25℃) | $I_{chg}$ | 24 | 35 | 42 | μA |
| Discharge Current ($V_{CC}$=5.0V to 40V, $T_A$=25℃) | $I_{dischg}$ | 140 | 220 | 260 | μA |
| Discharge to Charge Current Ratio (Pin 7 to $V_{CC}$, $T_A$=25℃) | $I_{dischg}/I_{chg}$ | 5.2 | 6.5 | 7.5 | - |
| Current Limit Sense Voltage ($I_{chg=}$=$I_{dischg}$, $T_A$=25℃) | $V_{ipk(sence)}$ | 250 | 300 | 350 | mV |
| **OUTPUT SWITCH (NOTE 2)** | | | | | |
| Saturation Voltage, Darlington Connection (Note 3) ($I_{SW}$=1.0A, Pins 1, 8 connected) | $V_{CE(sat)}$ | - | 1.0 | 1.3 | V |
| Saturation Voltage, Darlington Connection ($I_{SW}$=1.0A, $R_{Pin\ 8}$=82Ω to $V_{CC}$, Forced $\beta \cong 20$) | $V_{CE(sat)}$ | - | 0.45 | 0.7 | V |
| DC Current Gain ($I_{SW}$=1.0A, $V_{CE}$=5.0V, $T_A$=25℃) | $h_{FE}$ | 50 | 75 | - | - |
| Collector Off-State Current ($V_{CE}$=40V) | $I_{C(off)}$ | - | 0.01 | 100 | μA |
| **COMPARATOR** | | | | | |
| Threshold Voltage | $V_{th}$ | | | | V |
| ($T_A$=25℃) | | 1.238 | 1.25 | 1.262 | |
| ($T_A$=$T_{low}$ to $T_{high}$) | | 1.225 | - | 1.275 | |
| Threshold Voltage Line Regulation ($V_{CC}$=3.0V to 40V) | $Reg_{line}$ | - | 1.4 | 5.0 | mV |
| Input Bias Current ($V_{in}$=0V) | $I_{IB}$ | - | -20 | -400 | nA |
| **TOTAL DEVICE** | | | | | |
| Supply Current ($V_{CC}$=5.0V to 40V, $C_T$=1.0nF, Pin 7=$V_{CC}$, $V_{Pin\ 5}$>$V_{th}$, Pin 2=Gnd, remaining pins open) | $I_{CC}$ | - | - | 4.0 | mA |

NOTES:
1. Tlow=0℃ Thigh=+70℃
2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.
3. If the output switch is driven into hard saturation (non-Darlington) at low switch currents (≤300mA) and high driver currents (≥30mA), it may take up to 2.0μs for it to come out of saturation. This condition will shorten the off time at frequencies ≥30kHz, and is magnified at high temperature. This condition does not occur with a Darlington configuration, since the output switch cannot saturate. If a non-Darlington configuration is used, the following output drive condition is recommended:

Forced $\beta$ of output switch: $$\frac{I_C \text{ output}}{I_C \text{ driver - 7.0mA *}} \geq 10$$

*The 100Ω resister in the emitter of the driver device requires about 7.0mA before the output switch conducts.

# DC to DC Converter Controller

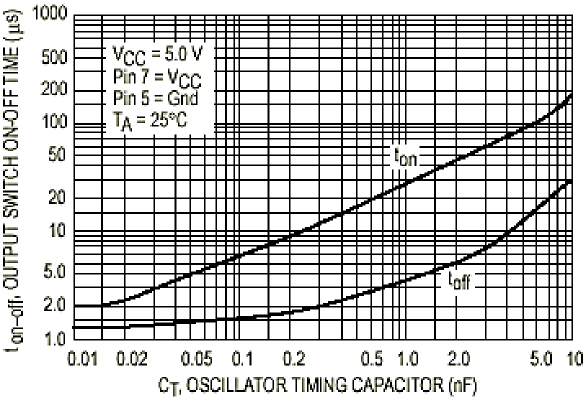



**Fig 1.Output Switch On-Off Time versus Oscillator Timing Capacitor**

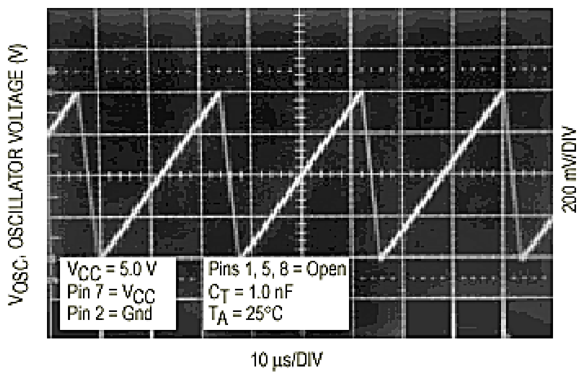



**Fig 2. Timing Capacitor Waveform**

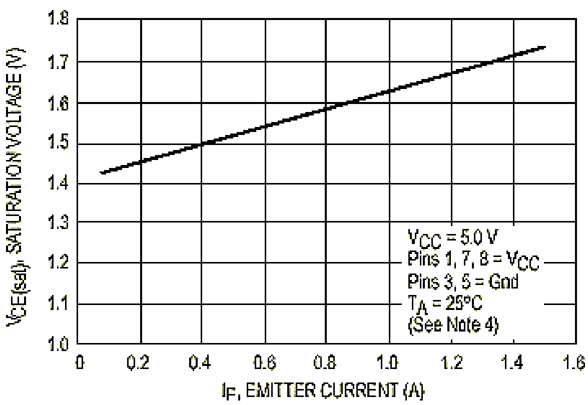



**Fig 3.Emitter Follower Configuration Output Saturation Voltage versus Emitter Current**

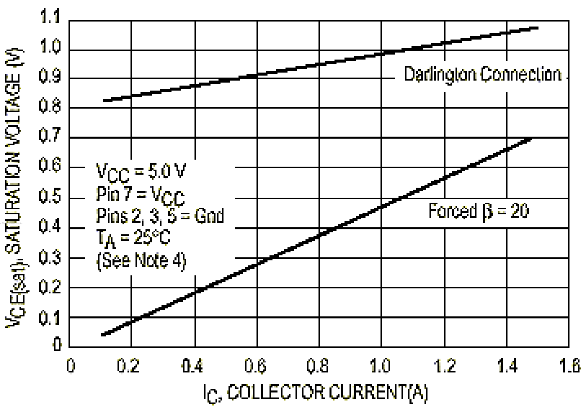



**Fig 4.Common Emitter Configuration Output Switch Saturation Voltage versus Collector Current**

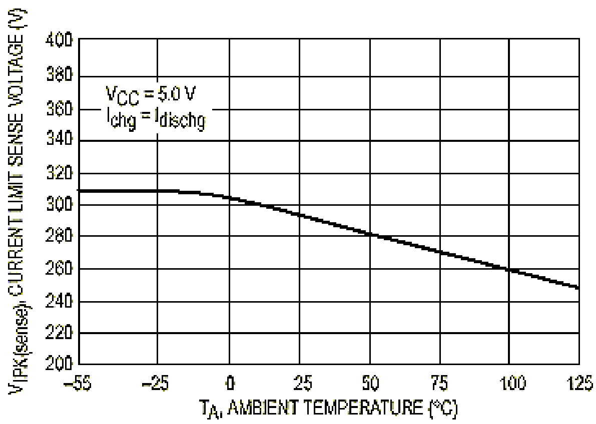



**Fig 5.Current Limit Sense Voltage versus Temperature**

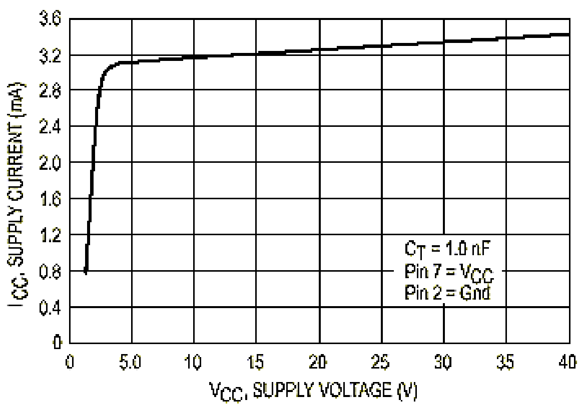
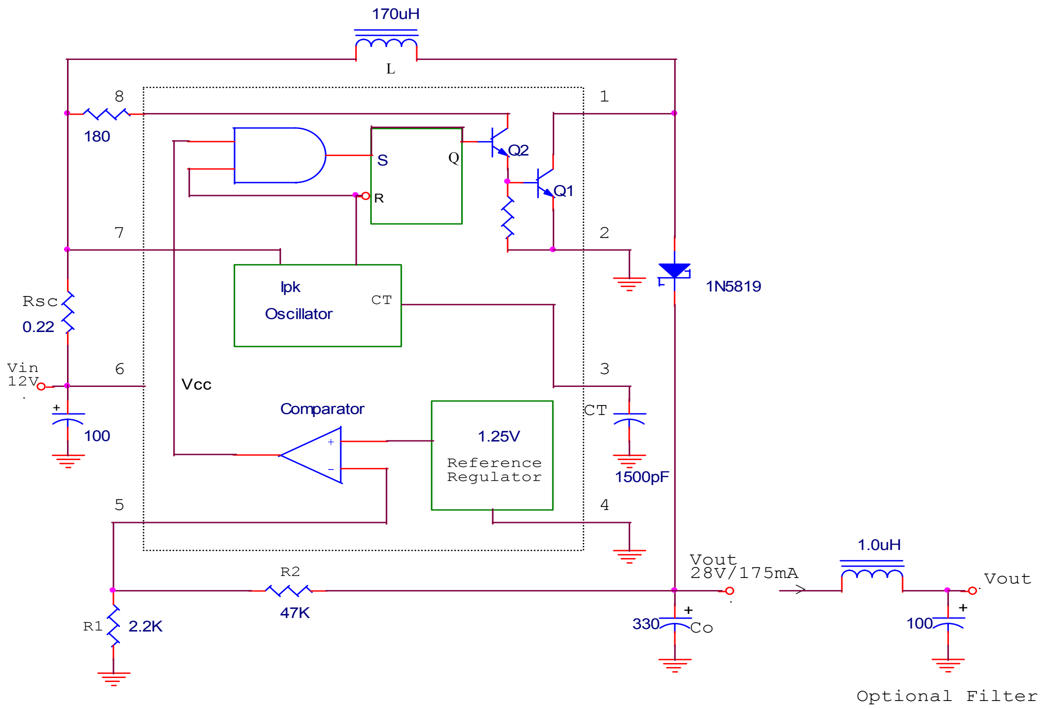
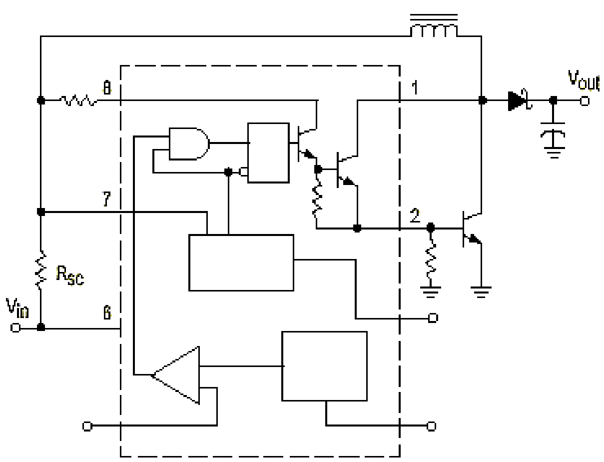



**Fig 6.Standby Supply Current versus Supply Voltage**

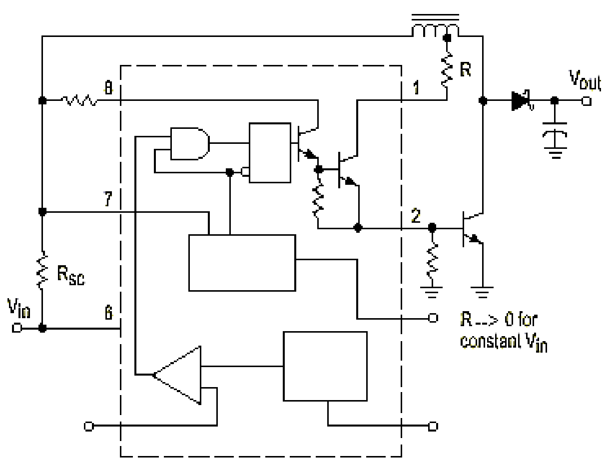



| Test | Conditions | Results |
|---|---|---|
| Line Regulation | $V_{in}$=8.0 V to 16V, $I_O$=175 mA | 30 mV=±0.05% |
| Load Regulation | $V_{in}$=12 V, $I_O$=75 mA to 175 mA | 10 mV=±0.017% |
| Output Ripple | $V_{in}$=12 V, $I_O$=175 mA | 400 mVpp |
| Effciency | $V_{in}$=12 V, $I_O$=175 mA | 87.7% |
| Output Ripple With Optional Filter | $V_{in}$=12 V, $I_O$=175 mA | 40 mVpp |

**Fig 7. Step-Up Converter**



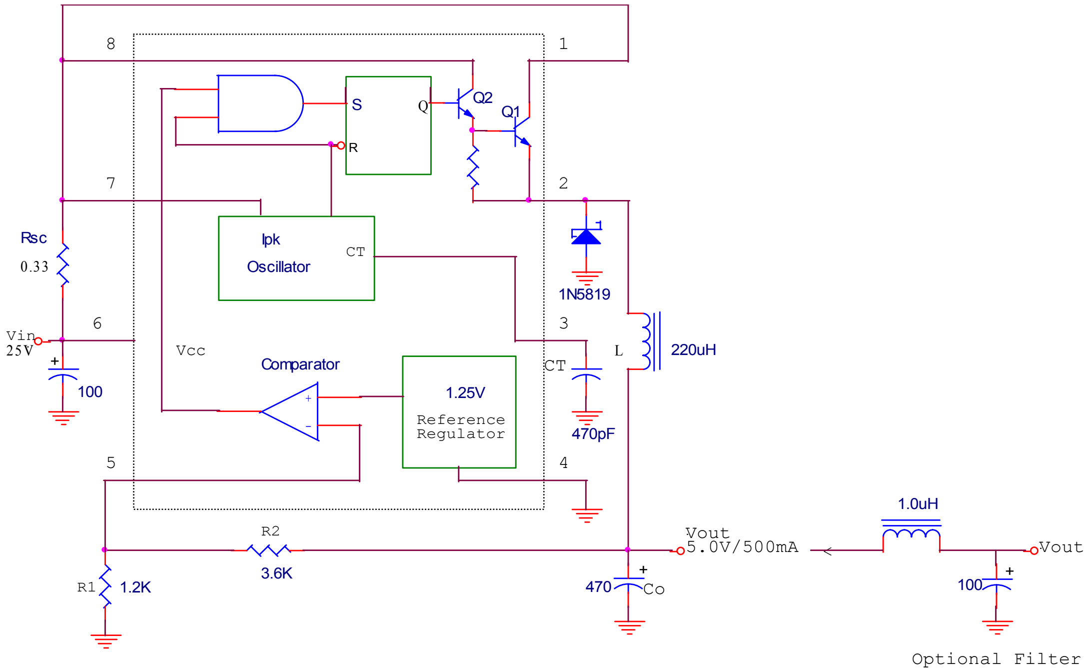

**8-1. External NPN Switch**




**8-2. External NPN Saturated Switch(See Note 5)**

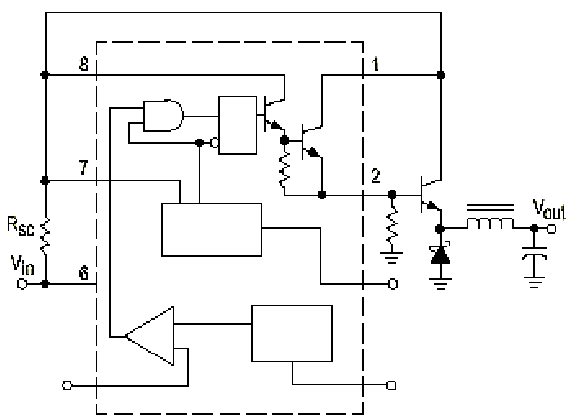
# DC to DC Converter Controller

**Fig 8. External Current Boost Connections for $I_C$ Peak Greater than 1.5A**

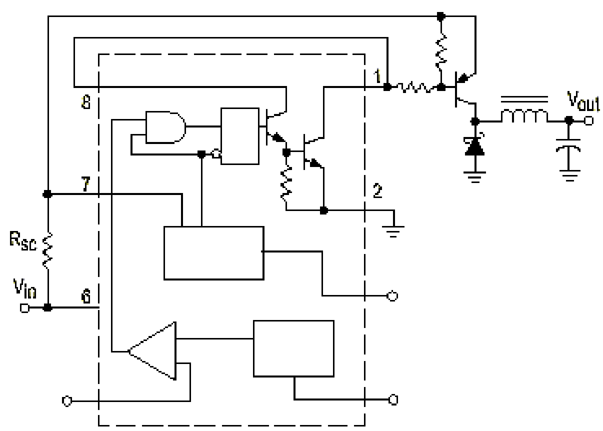



| Test | Conditions | Results |
|---|---|---|
| Line Regulation | $V_{in}$=15 V to 25V, $I_O$=500 mA | 12 mV=±0.12% |
| Load Regulation | $V_{in}$=25 V, $I_O$=50 mA to 500 mA | 3.0 mV=±0.03% |
| Output Ripple | $V_{in}$=25 V, $I_O$=500 mA | 120 mVpp |
| Short Circuit Current | $V_{in}$=25 V, $R_L$=0.1 Ω | 1.1 A |
| Effciency | $V_{in}$=25 V, $I_O$=500 mA | 83.7% |
| Output Ripple With Optional Filter | $V_{in}$=25 V, $I_O$=500 mA | 40 mVpp |

**Fig 9. Step-Down Converter**



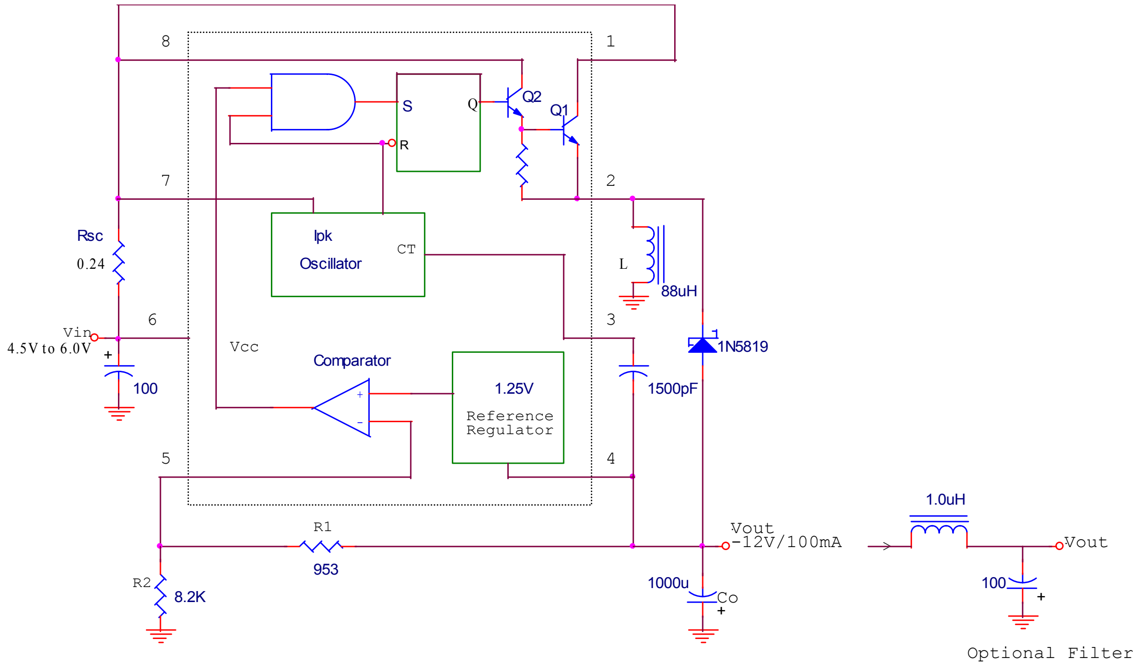

**10-1. External NPN Switch**




**10-2. External PNP Saturated Switch**

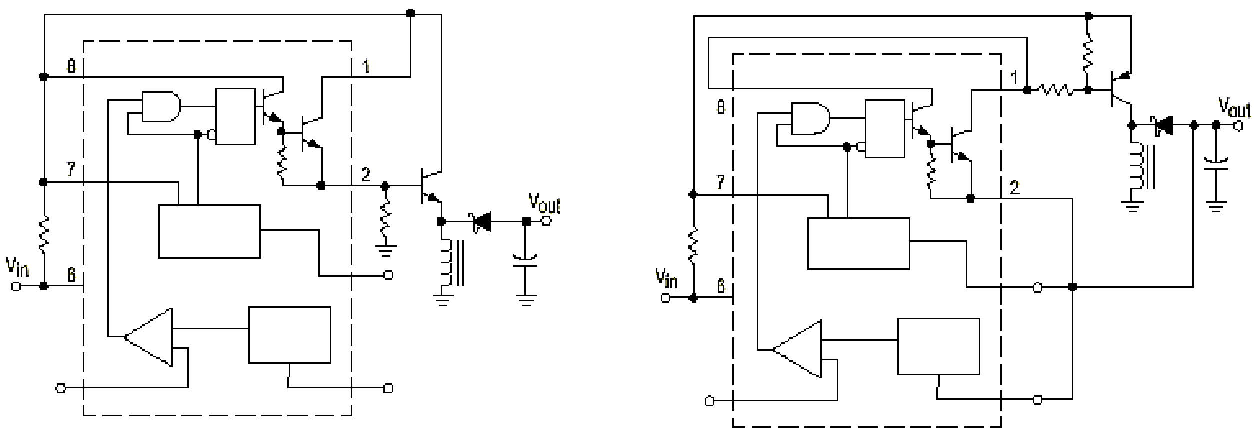
# DC to DC Converter Controller

**Fig 10. External Current Boost Connections for $I_C$ Peak Greater than 1.5A**




| Test | Conditions | Results |
|---|---|---|
| Line Regulation | $V_{in}$=4.5 V to 6.0V, $I_O$=100 mA | 3.0 mV=±0.012% |
| Load Regulation | $V_{in}$=5.0 V, $I_O$=10 mA to 100 mA | 0.022 V=±0.09% |
| Output Ripple | $V_{in}$=5.0 V, $I_O$=100 mA | 500 mVpp |
| Short Circuit Current | $V_{in}$=5.0 V, $R_L$=0.1 Ω | 910 mA |
| Effciency | $V_{in}$=5.0 V, $I_O$=100 mA | 62.2% |
| Output Ripple With Optional Filter | $V_{in}$=5.0 V, $I_O$=100 mA | 70 mVpp |

**Fig 11. Voltage Inverting Converter**




**12-1. External NPN Switch**

**12-2. External PNP Saturated Switch**

**Fig 12. External Current Boost Connections for $I_C$ Peak Greater than 1.5A**

NOTE: 5. If the output switch is driven into hard saturation (non-Darlington configuration) at low switch currents (≤300 mA) and high driver currents (≥ 30 mA), it may take up to 2.0 µs to come out of saturation. This condition will shorten the off time at frequencies ≥ 30 kHz, and is magnified at high temperatures. This condition does not occur with a Darlington configuration, since the output switch cannot saturate. If a non-Darlington configuration is used, the following output drive condition is recommended.

| Calculation | Step-Up | Step-Down | Voltage-inverting |
|---|---|---|---|
| $t_{on}/t_{off}$ | $\frac{V_{out}+V_F-V_{in(min)}}{V_{in(min)}-V_{sat}}$ | $\frac{V_{out}+V_F}{V_{in(min)}-V_{sat}-V_{out}}$ | $\frac{\lvert V_{out}\rvert+V_F}{V_{in}-V_{sat}}$ |
| $t_{on}+t_{off}$ | $\frac{1}{f}$ | $\frac{1}{f}$ | $\frac{1}{f}$ |
| $t_{off}$ | $\frac{t_{on}+t_{off}}{\frac{t_{on}}{t_{off}}+1}$ | $\frac{t_{on}+t_{off}}{\frac{t_{on}}{t_{off}}+1}$ | $\frac{t_{on}+t_{off}}{\frac{t_{on}}{t_{off}}+1}$ |
| $t_{on}$ | $(t_{on}+t_{off})-t_{off}$ | $(t_{on}+t_{off})-t_{off}$ | $(t_{on}+t_{off})-t_{off}$ |
| $C_T$ | $4.0\times10^{-5}t_{on}$ | $4.0\times10^{-5}t_{on}$ | $4.0\times10^{-5}t_{on}$ |
| $I_{pk(switch)}$ | $2I_{out(max)}(\frac{t_{on}}{t_{off}}+1)$ | $2I_{out(max)}$ | $2I_{out(max)}(\frac{t_{on}}{t_{off}}+1)$ |
| $R_{sc}$ | $0.3/I_{pk(switch)}$ | $0.3/I_{pk(switch)}$ | $0.3/I_{pk(switch)}$ |
| $L_{(min)}$ | $(\frac{(V_{in(min)}-V_{sat})}{I_{pk(switch)}})t_{on(max)}$ | $(\frac{(V_{in(min)}-V_{sat}-V_{out})}{I_{pk(switch)}})t_{on(max)}$ | $(\frac{(V_{in(min)}-V_{sat})}{I_{pk(switch)}})t_{on(max)}$ |
| $C_O$ | $9\frac{I_{out}t_{on}}{V_{ripple(pp)}}$ | $\frac{I_{pk(switch)}(t_{on}+t_{off})}{8V_{ripple(pp)}}$ | $9\frac{I_{out}t_{on}}{V_{ripple(pp)}}$ |

**Fig 13. Design Formula Table**

$V_{sat}$ = Saturation voltage of the output switch.

$V_F$ = Forward voltage drop of the output rectifier.

**The following power supply characteristics must be chosen:**

$V_{in}$ – Nominal input voltage.

$V_{out}$ – Desired output voltage, $|V_{out}|=1.25(1+\frac{R_2}{R_1})$

$I_{out}$ –Desired output current.

$f_{min}$ – Minimum desired output switching frequency at the selected values of $V_{in}$ and $I_O$.

$V_{ripple(p-p)}$ –Desired peak-to-peak output ripple voltage. In practice, the calculated capacitor value will need to be increased due to its equivalent series resistance and board layout. The ripple voltage should be kept to a low value since it will directly affect the line and load regulation.