

NP55N04SLG

R07DS0242EJ0100

Rev.1.00

Feb 23, 2011

MOS FIELD EFFECT TRANSISTOR

Description

The NP55N04SLG is N-channel MOS Field Effect Transistor designed for high current switching applications.

Features

- Channel temperature 175 degree rating
- Super low on-state resistance
 - $R_{DS(on)1} = 6.5 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 28 \text{ A)}$
 - $R_{DS(on)2} = 8.5 \text{ m}\Omega \text{ MAX. (} V_{GS} = 5 \text{ V, } I_D = 28 \text{ A)}$
 - $R_{DS(on)3} = 15 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.5 \text{ V, } I_D = 11 \text{ A)}$
- Low input capacitance
- Gate to Source ESD protection diode built-in

Ordering Information

Part No.	LEAD PLATING	PACKING	Package
NP55N04SLG-E1-AY *1	Pure Sn (Tin)	Tape 2500 p/reel	TO-252 (MP-3ZK)
NP55N04SLG-E2-AY *1			

Note: *1. Pb-free (This product does not contain Pb in external electrode.)

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to Source Voltage ($V_{GS} = 0 \text{ V}$)	V_{DSS}	40	V
Gate to Source Voltage ($V_{DS} = 0 \text{ V}$)	V_{GSS}	± 20	V
Drain Current (DC) ($T_C = 25^\circ\text{C}$)	$I_{D(DC)}$	± 55	A
Drain Current (pulse) *1	$I_{D(pulse)}$	± 220	A
Total Power Dissipation ($T_C = 25^\circ\text{C}$)	P_{T1}	77	W
Total Power Dissipation ($T_A = 25^\circ\text{C}$)	P_{T2}	1.2	W
Channel Temperature	T_{ch}	175	$^\circ\text{C}$
Storage Temperature	T_{stg}	$-55 \text{ to } +175$	$^\circ\text{C}$
Repetitive Avalanche Current *2	I_{AR}	30	A
Repetitive Avalanche Energy *2	E_{AR}	90	mJ

Thermal Resistance

Channel to Case Thermal Resistance	$R_{th(ch-C)}$	1.95	$^\circ\text{C/W}$
Channel to Ambient Thermal Resistance *2	$R_{th(ch-A)}$	125	$^\circ\text{C/W}$

Notes: *1. $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

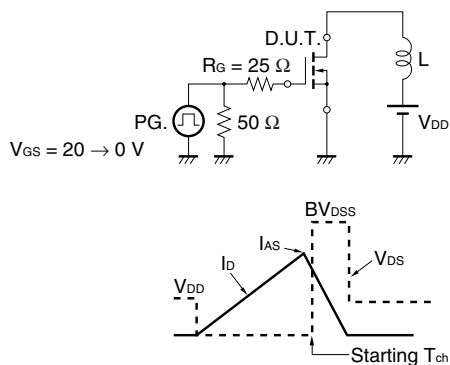
*2. Starting $T_{ch} \leq 150^\circ\text{C}$, $V_{DD} = 20 \text{ V}$, $R_G = 25 \Omega$, $V_{GS} = 20 \rightarrow 0 \text{ V}$

Electrical Characteristics ($T_A = 25^\circ\text{C}$)

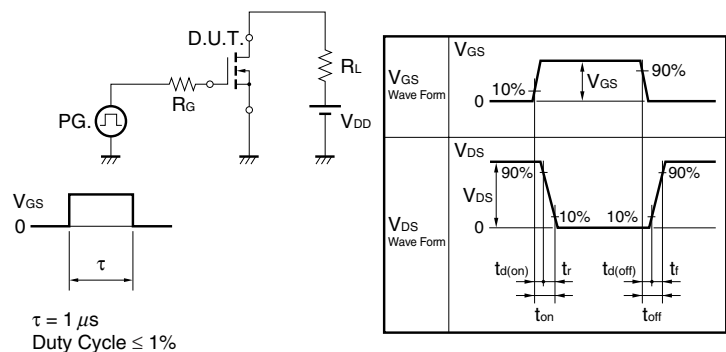
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	I_{DSS}			1	μA	$V_{DS} = 40\text{ V}$, $V_{GS} = 0\text{ V}$
Gate Leakage Current	I_{GSS}			± 10	μA	$V_{GS} = \pm 20\text{ V}$, $V_{DS} = 0\text{ V}$
Gate to Source Threshold Voltage	$V_{GS(th)}$	1.5	2.0	2.5	V	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$
Forward Transfer Admittance ^{*1}	$ y_{fs} $	12	32		S	$V_{DS} = 10\text{ V}$, $I_D = 28\text{ A}$
Drain to Source On-state Resistance ^{*1}	$R_{DS(on)1}$		4.7	6.5	$\text{m}\Omega$	$V_{GS} = 10\text{ V}$, $I_D = 28\text{ A}$
	$R_{DS(on)2}$		5.7	8.5	$\text{m}\Omega$	$V_{GS} = 5.0\text{ V}$, $I_D = 28\text{ A}$
	$R_{DS(on)3}$		6.3	15	$\text{m}\Omega$	$V_{GS} = 4.5\text{ V}$, $I_D = 11\text{ A}$
Input Capacitance	C_{iss}		2700	4050	pF	$V_{DS} = 25\text{ V}$,
Output Capacitance	C_{oss}		310	465	pF	$V_{GS} = 0\text{ V}$,
Reverse Transfer Capacitance	C_{rss}		200	380	pF	$f = 1\text{ MHz}$
Turn-on Delay Time	$t_{d(on)}$		15	33	ns	$V_{DD} = 20\text{ V}$, $I_D = 28\text{ A}$, $V_{GS} = 10\text{ V}$, $R_G = 0\text{ }\Omega$
Rise Time	t_r		17	43	ns	
Turn-off Delay Time	$t_{d(off)}$		60	120	ns	
Fall Time	t_f		8	20	ns	
Total Gate Charge	Q_G		57	86	nC	$V_{DD} = 32\text{ V}$, $V_{GS} = 10\text{ V}$, $I_D = 55\text{ A}$
Gate to Source Charge	Q_{GS}		9		nC	
Gate to Drain Charge	Q_{GD}		17		nC	
Body Diode Forward Voltage ^{*1}	$V_{F(S-D)}$		0.9	1.5	V	$I_F = 55\text{ A}$, $V_{GS} = 0\text{ V}$
Reverse Recovery Time	t_{rr}		30		ns	$I_F = 55\text{ A}$, $V_{GS} = 0\text{ V}$, $di/dt = 100\text{ A}/\mu\text{s}$
Reverse Recovery Charge	Q_{rr}		28		nC	

Note: *1. Pulsed test

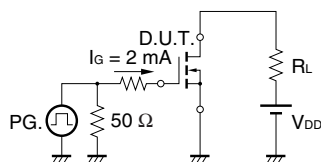
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

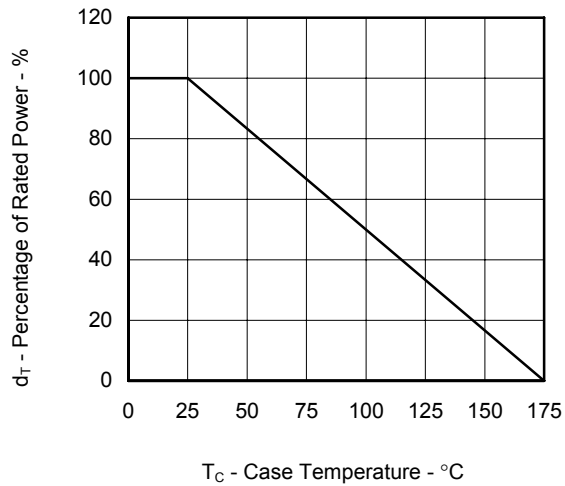


TEST CIRCUIT 3 GATE CHARGE

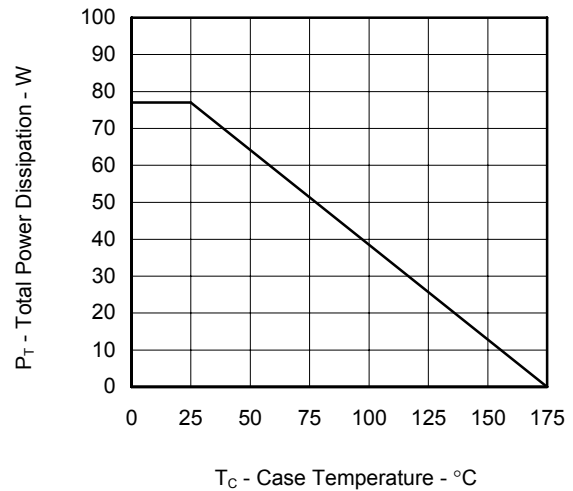


Typical Characteristics ($T_A = 25^\circ\text{C}$)

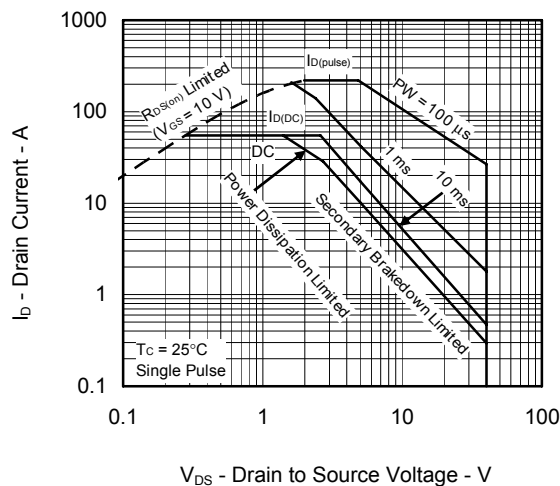
DERATING FACTOR OF FORWARD BIAS
SAFE OPERATING AREA



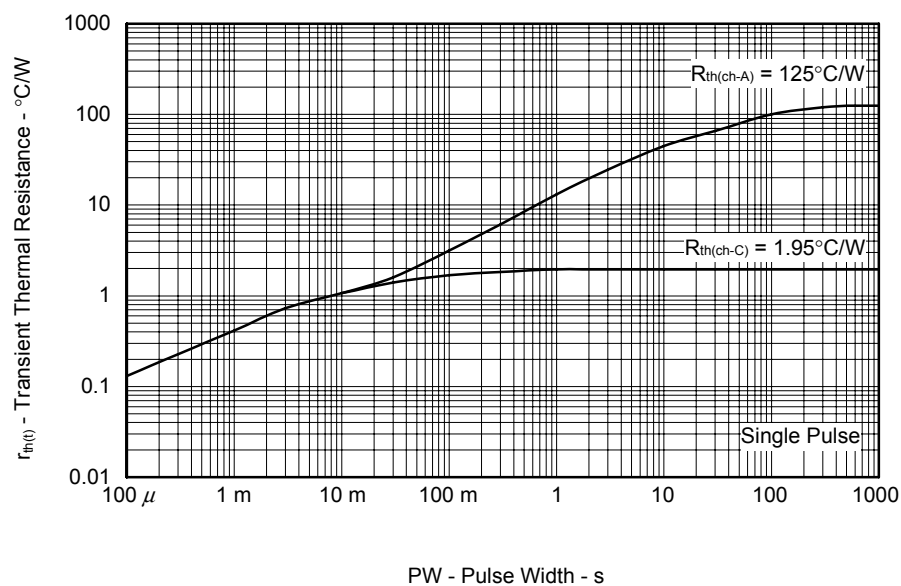
TOTAL POWER DISSIPATION vs.
CASE TEMPERATURE

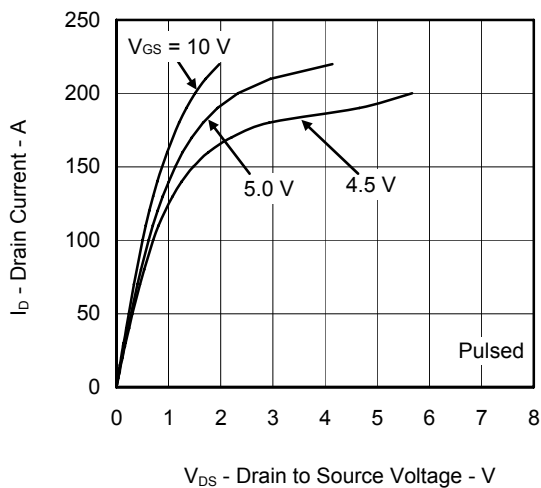


FORWARD BIAS SAFE OPERATING AREA

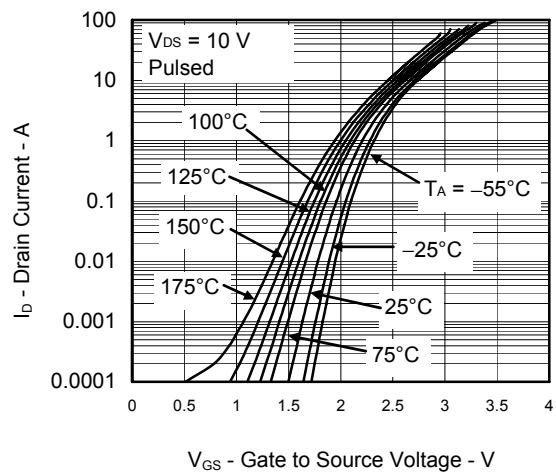
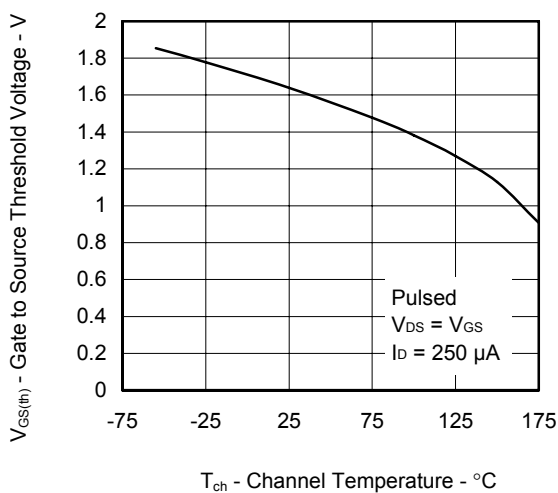
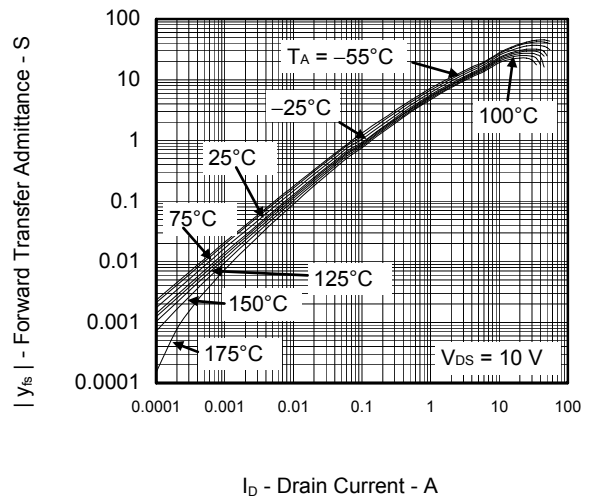
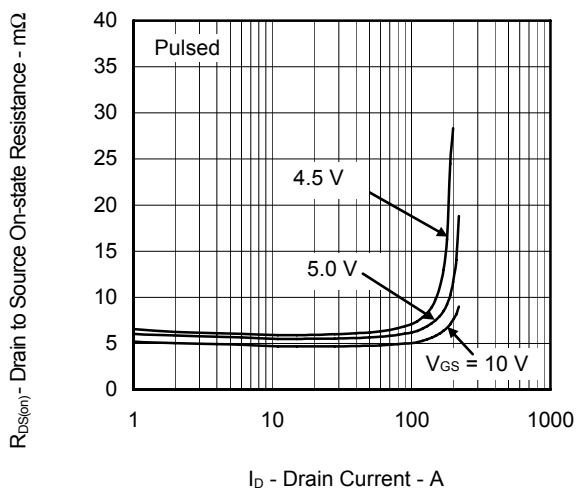
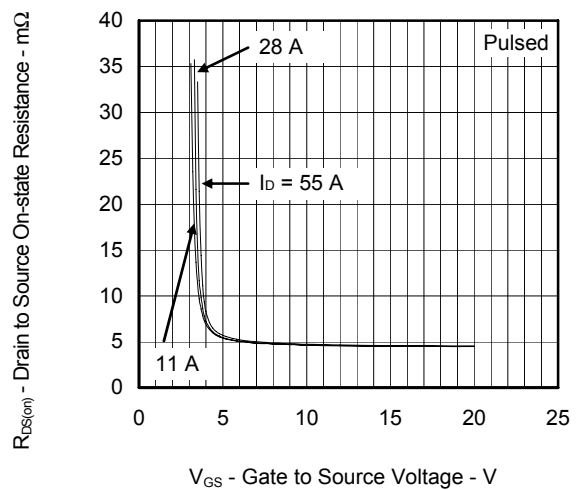


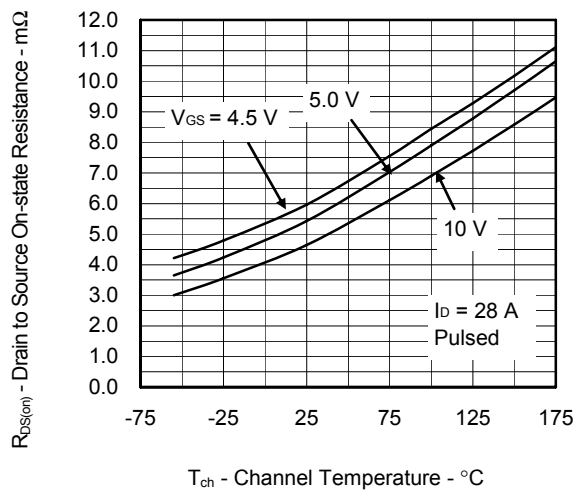
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



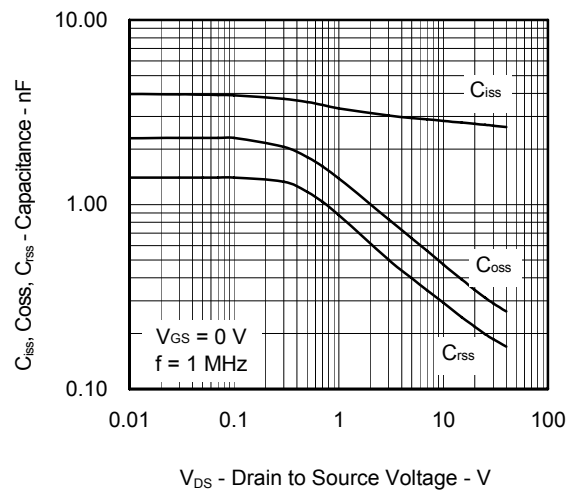
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE

FORWARD TRANSFER CHARACTERISTICS

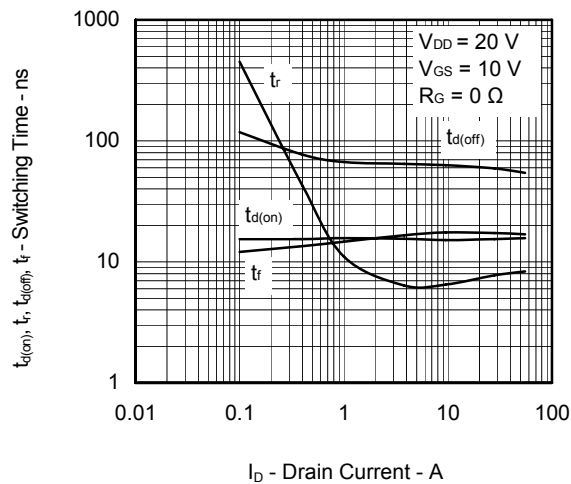
GATE TO SOURCE THRESHOLD VOLTAGE vs.
CHANNEL TEMPERATUREFORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENTDRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENTDRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE

DRAIN TO SOURCE ON-STATE RESISTANCE vs.
CHANNEL TEMPERATURE

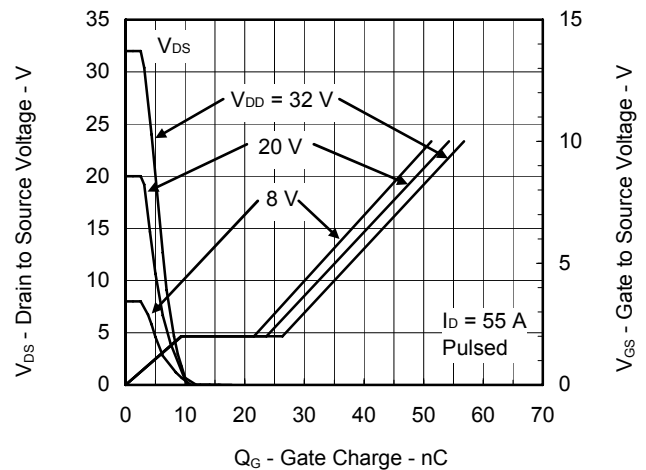
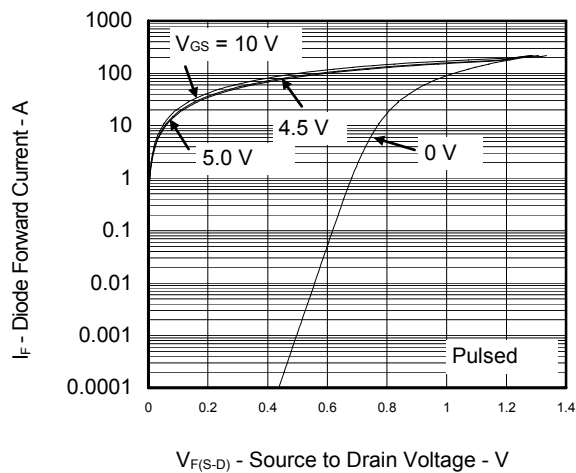
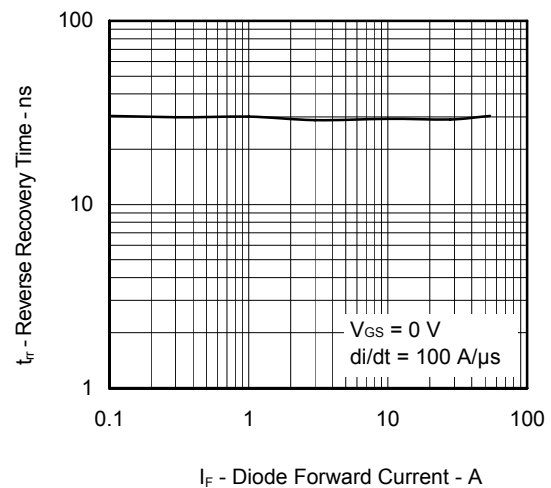
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



SWITCHING CHARACTERISTICS

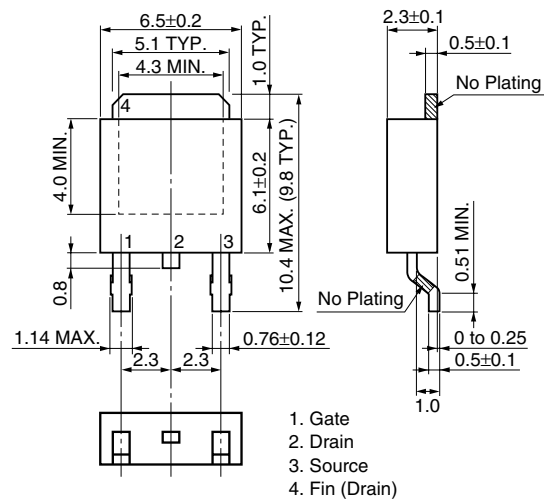


DYNAMIC INPUT/OUTPUT CHARACTERISTICS

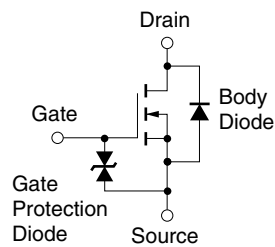
SOURCE TO DRAIN DIODE
FORWARD VOLTAGEREVERSE RECOVERY TIME vs.
DIODE FORWARD CURRENT

Package Drawings (Unit: mm)

TO-252 (MP-3ZK)



Equivalent Circuit



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

Revision History	NP55N04SLG Data Sheet
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Rev.	Date	Description	
		Page	Summary
1.00	Feb 23, 2011	–	First Edition Issued

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Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
7F, No. 363 Fu Shing North Road Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
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Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Laved' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141