MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Advanced Information I/O EXPANDER (PORT REPLACEMENT UNIT)

The MC68HC25 is a peripheral device which permits simple interfacing of a range of MCUs to external devices without potential loss of port I/O. Intended for use with the 146805E2, 6801, 6801U4, 6803, 6803U4, and 68HC11 processors manufactured by Motorola, the MC68HC25 provides address/data demultiplexing and port operation which replicates that of the displaced ports.

Use of the MC68HC25 provides a cost effective, monolithic solution to the situation of an MCU/MPU operating in expanded mode. This is particularly relevant where board space is at a premium.

Features

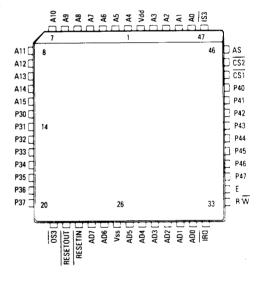
- Choice of Memory Map Size: 8K, 64K
- Choice of Memory Devices: 16K, 32K, 64K, 256K
- 2 Chip Select Signals for use with External Devices
- 8 Bit Bi-Directional Port with 2 Handshake Control Lines (Port 3), plus IRQ output for signalling MCU
- 8 Bit Bi-Directional Port (Port 4)
- Shift Mode to Permit Full Utilisation of On-Board and External Memory (No "Holes" in Map)
- TTL or CMOS Input Capability
- Full Demultiplexing of Address and Data
- System Reset Controlled through MC68HC25 allows Full Reset or Resetting of MCU without Affecting Port I/O Status
- Low Power Consumption HCMOS Technology
- 0 2.1 Mhz Operation
- Compatible with 6801, 6801U4, 6803, 6803U4, 146805E2, 68HC11 Devices

MC68HC25



FN SUFFIX PLCC CASE 778-01

PIN ASSIGNMENT 52 Pin Quad Pack



| PIN = | PIN NAME | DESCRIPTION |
|-------|-----------|-----------------------|
| 1-4 | A4-A7 | ADDRESS LOW OUT |
| 5-12 | A8-A15 | ADDRESS HIGH N |
| 13-20 | P30-P37 | PORT =3 |
| 21 | 083 | PORT #3 OUTPUT STROBE |
| 22 | Reset out | RESET OUT |
| 23 | Reset in | RESET IN |
| 24-25 | A07-AD6 | ADDRESS DATA 10 |
| 26 | Vss | GROUND |
| 27-32 | ADS-AD0 | ADDRESS DATA - 0 |
| 33 | (RQ | PORT #31 0 INTERRUPT |
| 34 | RW | READ WRITE |
| 35 | E | CLOCK N |
| 36-43 | P47-P40 | PORT #1 |
| 44 | CS1 | CHIP SELECT : |
| 45 | CS2 | CHIP SELECT 2 |
| 46 | AS | ADDRESS STROBE |
| 47 | 1\$3 | PORT #31NPUT STROBE |
| 48-51 | A0-A3 | ADDRESS LOW OUT |
| 52 | Vdd | SUPPLY |

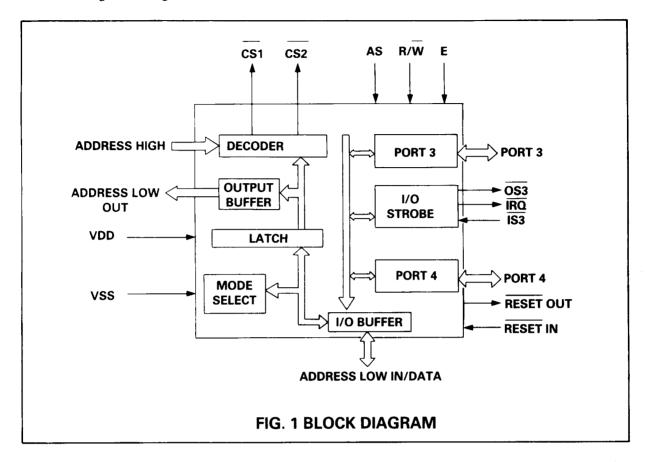


MOTOROLA

SYSTEM CONFIGURATION

Device Organisation

The block diagram of Figure 1 shows the main functional elements of the device.



High-order address bits (ADDRESS HIGH) are provided by the MPU/MCU on the non-multiplexed bus. The bus is also connected directly to the memory devices within the user's system. Low-order address bits and the data transferred in either direction between the MC68HC25 and the processor are multiplexed on a single 8-bit bus (ADDRESS LOW IN/DATA). The low-order addresses are latched on the negative edge of AS supplied by the MPU/MCU. The address inputs are fed to the decoder which determines the output low-order address (ADDRESS LOW OUT) and activates the relevant chip select (CS1, CS2). Decoding is controlled by the user-programmable mode select register (MODE SELECT) as described below.

The direction of valid data on the multiplexed address/data bus is determined by the R/\overline{W} input. Demultiplexing of address and data is carried out directly using the Address Strobe (AS) signal. $\overline{\text{CS1}}$ is intended for enabling read-only devices and is only qualified when R/\overline{W} is high. CS2 is qualified independently of R/W and therefore may be used to enable PROM, RAM, and peripheral devices. Both CS1 and CS2 are qualified by E-clock and therefore may be used with EPROMS which do not have a separate output enable line, eg. MCM68766.

Ports 3 and 4 operate similarly to those of the MCU/MPU to which the MC68HC25 is connected. Port 3 offers handshaking facilities identical to those found on the 6801/03 and 6801U4/03U4 through the OS3, IS3 and IRQ signals.

RESET IN is intended as the master reset, initialising the system to a known state. The MPU/MCU reset line should be connected to the RESET OUT output which becomes active two E-cycles after the reset condition is detected. The time between the two signals is used to input the mode select information from the external memory.

Since the RESET OUT output is designed with a resistive pull-up, it may be wire-OR'ed with another reset signal. This allows an MPU/MCU reset without affecting the condition of the MC68HC25 thus maintaining the status of the ports.

FUNCTIONAL PIN DESCRIPTION

The following paragraphs describe the function pins.

Note: all timings are referred to the E-clock provided by the controlling MCU/MPU.

Vdd AND Vss

Power is supplied to the 68HC25 using these two pins. Vdd is the power input and Vss is ground.

RESET IN

This active low high impedance input is used to initialise the MC68HC25 to a known state. Minimum low time is 1 E-clock cycle. During the low time of this input, Address/Data I/O pins and Address Low Out pins are forced to high impedance; Ports 3 & 4 data direction registers are initialised such that the ports are in the input mode; Port 3 handshake register is initialised; Chip Select (CS) 1 & 2 outputs are disabled and RESET OUT is held active low.

RESET IN is sampled on the rising edge of E-clock. the input must be stable prior to E rising edge. After the rising edge of E, the required mode selection information is captured from the external memory prior to the rising edge of RESET OUT. See **Mode Select Register**.

Note: When RESET IN is low, external PROMs may be programmed since Address/Data and Address Low Out busses are held at high impedance.

RESET OUT

This output is intended for connection to the controlling MCU and any other peripherals. RESET OUT follows RESET IN in phase with change of state occurring on the rising edge of Eclock. Immediately after RESET IN goes high, Address Low Out is configured to \$BF and CS1 is held active low allowing the Mode Select information to be retrieved. See **Mode Select Register**. Two cycles after RESET IN has been recognised as returning high, RESET OUT follows.

Note: RESET OUT contains an active pulldown device and a resistive pullup device with a typical impedance of 40kohms in a CMOS push-pull configuration. Thus a wire-or configuration is possible externally permitting the controlling MCU to be reset without affecting the registers of the MC68HC25. This facility permits continuity of the port outputs.

CLOCK (E)

E CLOCK is a high impedance input which provides timing reference information for the MC68HC25. In general, when E is low an internal process is taking place and when high, data is being accessed.

ADDRESS STROBE

ADDRESS STROBE(AS) demultiplexes the Address/Data bus. The falling edge of AS causes the low order address A0-A7 to be latched within the MC68HC25. Note that AS has an internal pullup of 40kohm nominal active during RESET OUT low.

READ/WRITE (R/W)

R/W is a high impedance input and is used to control the direction of transfers on the multiplexed Address/Data bus. Data is transferred on the high half cycle of E-clock. When the 68HC25 is selected and R/W is high (read), data output buffers are enabled. A low level on R/W enables data to be written to a selected register.

CHIP SELECT 1 (CS1)

CS1 is a push-pull output which is active low when a specific memory zone is being addressed. The relevant zone is defined by the **Mode Select Register**. While RESET IN is low, CS1 is disabled with only a 40kohm nominal pullup visible. This pullup is disconnected while the output buffer is enabled. The buffer is capable of driving 90pF and 1 TTL load. In normal operation, CS1 is qualified only on E-clock high and R/W high.

CHIP SELECT 2 (CS2)

CS2 performs in a similar manner to CS1. (See **Mode Select Register**). However, CS2 is independent of R/W.

ADDRESS/DATA I/O

Address and data information must be supplied to the 68HC25 during the low and high half cycles of the E-clock respectively. Low order address bits (A0-A7) must be stable prior to the falling edge of AS at which time they are latched. This address in conjunction with the high order address (A8-A15) is used to decode the internal registers and assert CS1 or CS2 as appropriate. Valid write data must be presented to the MC68HC25 with R/W active low during the high half of the E-clock. Where R/W is asserted high, read data will be output during the high half cycle of E. (See **Bus Timing Characteristics**). Output buffers are capable of driving 90pF and 1 TTL load. Pullup devices of 40kohm nominal are active only during RESET IN.

ADDRESS LOW OUT

Address Low Out provides the demultiplexed low order address bits (A0-A7). Note that ALO bus is transparent during AS high and follows Address/Data bus in order to provide maximum access time to the PROMs. Push-pull buffers are implemented, capable of driving 90pF and 1 TTL load. While RESET IN is low, a high impedance is presented.

ADDRESS HIGH IN

Address High In bits (A8-A15) are decoded internally. In the case of 64K map operation, all bits are valid. For 8K mode, the upper three address lines are "dont-cared" within the device. However, it is recommended that the unused pins are grounded on the application board.

PORT 3

Port 3 is an 8-bit bidirectional I/O port (P30-P37). Each output buffer is capable of driving 30pF and 1 TTL load. Port operation is controlled through data and data direction registers. The data register for Port 3 is normally resident at address \$0006, except in displace mode. The data direction register is decoded at \$0002 in CMOS mode and \$0004 in TTL mode, again with the exception of displace mode. (See **Mode Select Register**). Both data and data direction registers are readable and writable.

A zero written to the specific data direction bit forces the corresponding output buffer to go to the high impedance input mode. A logic one written to the DDR bit configures the corresponding port line to the output mode. Transitions of data and data direction register bits are synchronised to occur on the rising edge of AS after a Port 3 register access.

A zero written to the data register drives the pulldown device of the output buffer when the corresponding DDR bit is preset to the output mode. Note that a write to the data register is retained even where the DDR is preset to the input mode which allows clean simultaneous switching of outputs upon configuring the port lines as outputs. A read of the data register where the DDR is configured as output returns the value currently stored in the data register, irrespective of the actual level on the pin. However in the input mode, only the actual level on the pin is returned. The level on the pin is latched on the rising edge of E and maintained until the falling edge irrespective of changes to the input.

During RESET IN, the data direction and data registers are set to \$00, hence the ports are preset to the input mode.

PORT 3 HANDSHAKE SIGNALS

Port 3 handshaking is analogous to that found on the M6801 family of MCUs. The three active signals, OS3, IS3 and IRQ, are predefined by the Handshake Control and Status register (HCS) located at address \$0F.

| | 7 | 6 5 | 4 | 3 | 2 | 1 | 0 | _ |
|---------------|------------|-------------------------------------|--|--|---------------------|-----------------------|----------------------|---|
| \$0F : | ISF : IS | SE : MOD : | OSS : | LEN : | ISS : | OS1 : | OS0 | - : - |
| Bit 7 | ISF | Read Only. reset. | Set by ac | ctive IS3 | edge. C | Cleared b | y read o | f Port 3 data register or |
| Bit 6 | ISE | When set, I Cleared at r | | ed wher | iever IS | F set. Wh | nen clea | r, IRQ is inhibited. |
| Bit 5 | MOD | | | | | | | ow. when clear, these eared at reset. |
| Bit 4 | oss | When clear, set, generat | | | | | of Port | 3 data register. When |
| Bit 3 | LEN | clear. If MO MOD bit, th | D is set, a e latch is | active lat transpa | ching e rent aft | dge depe er a Port | ends on 3 read. \ | IS3, provided MOD is ISS. Irrespective of When clear, Port 3 data ared at reset. |
| Bit 2 | ISS | is captured | on the ri | sing edg ns logica | e. Whe | n MOD is | clear, IS | ge of IS3. When set, data SS is cleared and a read are generated while |
| Bit 1/0 | OS1/OS0 | OS3 operat | ion is cor | ntrolled a | as follo | ws: | | |
| Soo Br | ant 2 Outo | OS1 OS0 1 1 1 0 0 1 0 0 | OS3 alv OS3 alv OS3 in OS3 in | OS3 vays hig vays lov pulse mo handsha | v ode | le | | |

See Port 3 Output Strobe OS3.

OS1 and OS0 are preset to zero when MOD is clear. A write instruction which sets MOD cannot simultaneously affect ISS, OS1 and OS0. These bits may be manipulated only on subsequent instructions. However, resetting the MOD bit has immediate effect on ISS, OS1 and OS0, putting them to their preset states.

PORT 3 OUTPUT STROBE OS3

OS3 may be used to strobe outputs to an external device or provide acknowledgement depending on the configuration of Port 3. In pulse mode, the active pulse low time is one Eclock cycle. Assertion of OS3 is synchronised to the rising edge of E on the machine cycle after the access of Port 3 and negated on the next rising edge of E. In handshake mode, the pulse width is determined by successive reads of the Port 3 data register. OS3 is asserted on the rising edge of E following the Port 3 data register access and remains active until the next rising edge of E following a Port 3 data register access. The Handshake Control and Status Register (HCS) determines whether a read or write is the active access.

In the case of constant high or constant low modes, OS3 changes state synchronised to the rising edge of E which follows the modifying access to HCS. See **Port 3 Handshake Signals**.

OS3 is capable of driving 30pF and 1 TTL load.

DATA INPUT STROBE IS3

IS3 may be used as an input strobe or data acknowledgement from an external device depending on Port 3 configuration. See **Port 3 Handshake Signals**. An active IS3 edge will set ISF flag in HCS which may be used to generate an IRQ signal. IS3 may also be used to latch data into Port 3 where LEN in HCS is set. IS3 is an asynchronous input therefore the timings specified in **Bus Timing Characteristics** must be adhered to. The IS3 input contains an active pullup device of 40kohm nominal which is active during normal operation.

INTERRUPT REQUEST IRQ

IRQ is a push-pull output with an active pulldown device and a driven resistive pullup device. Pullup impedance is nominally 40kohm. As a result, other active low interrupt sources can be wire or'ed to IRQ with the resistive pullup serving all sources. Secondly, if the MC68HC25 is the only device present, the buffer avoids DC current drain. The output of IRQ is dependent on CMOS/TTL mode. See **Mode Select Register**. If TTL mode is selected, then IRQ output is a NAND function of ISF and ISE. See **Port 3 Handshake Signals**. However, if CMOS mode is selected, IRQ generates a 1 E-clock cycle pulse as a result of the falling edge of the NAND function of ISF and ISE. This facilitates compatibility with the latched negative edge sensitive interrupt of 146805E2.

PORT 4

Port 4 performs in the same way as Port 3 with the exception of handshaking facilities. Also, in TTL mode an active pullup of 40kohm nominal is connected on all pins. The pullups are disabled in CMOS mode, except during RESET OUT low when pullups are enabled in both modes. Port 4 data register is decoded at address \$07, except in displace mode. See Mode Select Register. Port 4 data direction register is decoded at \$03 for CMOS mode and \$05 for TTL mode, except in displace mode.

OPERATIONAL ENVIRONMENTS

The MC68HC25 allows the user to select specific modes of operation depending on the desired environment.

In the 6801/03 environment, Ports 3 and 4 are replaced by the MC68HC25 and an address range of 64K bytes of memory is available. Port 3 handshaking is implemented on the 68HC25 via 0S3 and 1S3 in the same way as in the MC6801.

In the 146805E2 environment, two additional ports are provided whilst up to 8K bytes of external memory may be addressed.

In the 68HC11 environment ports B and C are replaced, although it should be noted that handshaking is not fully replicated. Up to 64K bytes of memory may be addressed.

Consult the relevant Motorola data sheets in each case.

MODE SELECT REGISTER

The mode select register must be configured by the user to determine the required memory decoding. Six types of information are required:

MAP SIZE : either 8K or 64K bytes

SHIFT : re-locate external memory addressing to allow use of internal MCU ROM

SIZE 1 : 16K, 32K or 64K bit external PROM 1 SIZE 2 : 16K, 32K, 64K or 256K bit external PROM 2

CMOS/TTL : CMOS or TTL input capability

DISPLACE : Support 6801U4 or 68HC11 operation by re-mapping I/O registers

The register value is programmed by the user at external memory address \$XFBF. (X= 1 for 8K memory map, X=F for 64K memory map.) The information is transferred to the MC68HC25 during the rising edge of the RESET IN (RSI) signal prior to the rising edge of the RESET OUT. During this period, the MPU/MCU is in reset and hence the Address High bus output is in the default condition of \$FF. During the cycle following the rising edge of RSI, the Address Low Out lines are forced to \$BF. Simultaneously Chip Select 1 (CS1) is asserted low, ensuring that PROM 1 is activated at \$XFBF. During the E high-time of this cycle, the contents of the PROM at this address are transferred and latched in an internal register inaccessible to the user. Note that an EPROM device must be connected to CS1 for correct operation. (See Figure 12.)

| M7 | M6 | M5 | M4 | M3 | M2 | M1 | MO |
|--------------------------|--------------------------|--------------------------|--------------------------|-----------------------------------|------------------------|-----------------------|----------------------------|
| PROM 2 SIZE SELECT | PROM 2 SIZE SELECT | PROM 1 SIZE SELECT | PROM 1 SIZE SELECT | PROM 1 DECODE ZONE SHIFT | CMOS OR TTL MODE | MEMORY MAP SIZE | PORT DECODE DISPLACE |

DISPLACE (M0)

If M0 is read as 1, then both Port 3 and Port 4 data and data direction registers are translated by \$0100. This permits Port 4 to act as a fully programmable I/O port, even when the 6801U4 is configured in mode 1*. The displace mode also prevents conflict of the on-board RAM of the MC68HC11 with both Port 3 and Port 4 by translating the relevant addresses outwith the RAM area.

* See MC6801U4 data sheet

MEMORY MAP SIZE (M1)

The map size information determines the total memory map available in the system. If the value of M1 transferred during reset to the MC68HC25 is high, then a 64K memory map size is recognised. If M1 is low, then an 8K map is used. In the latter case, the uppermost 3 inputs of the ADDRESS HIGH bus are ignored within the MC68HC25. This feature effectively remaps CHIP SELECT 2 to the 8K memory map during reset.

In the case of 8K memory map mode, a zero level must be hardwired on the corresponding pins on the MC68HC25, namely the uppermost 3 addresses of the ADDRESS HIGH input bus address A15, A14 and A13. These are ignored (don't cared) during all the internal decoding as well as for the CHIP SELECT 1 and 2 outputs.

CMOS OR TTL MODE (M2)

This bit allows the MC68HC25 to configure Port 4 address decoding, Port 4 pull up device control, as well as IRQ edge or level output modes. If M2 is low, TTL mode is active. For M2 high, CMOS mode is used.

PROM 1 DECODE ZONE SHIFT (M3)

When set, this bit translates (shifts) the decode zone of CS1 by \$2000. See Figure 4. The translation facilitates the use of the on-board ROM of the MCU.

PROM 1 SIZE SELECT (M4, M5)

These two bits select the decode zone for Chip Select 1. The available combinations allow full use of 16K, 32K or 64K bit PROMs. See Figures 3 and 4.

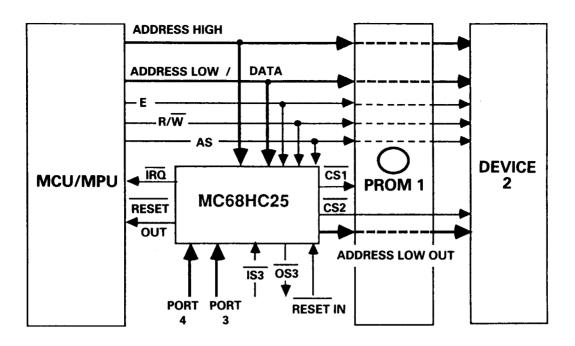
| M4 | M5 | M3 | CHIP SELECT 1 DECODE RANGE | |
|----|----|-------|--|--|
| 1 | 1 | 0 | 16K PROM DECODE : X800-XFFF | |
| 1 | 1 | (*) 1 | 16K PROM DECODE : D800-DFFF + FFF0-FFFF | |
| o | 1 | 0 | 32K PROM DECODE : X000-XFFF | |
| 0 | 1 | (*) 1 | 32K PROM DECODE : D000-DFFF + FFF0-FFFF | |
| 1 | 0 | (*) 0 | 64K PROM DECODE : E000-FFFF | X=F IN 64K MAP |
| 1 | 0 | (*) 1 | 64K PROM DECODE : C000-DFFF +FFF0-FFFF | X=1 IN 8K MAP |
| 0 | 0 | x | NOT USED – RESERVED | * This mode should not be used in the 8K Memory Map mode |

Chip Select 1 is active low when the above addresses are decoded. For correct operation of the whole system, an external memory device must be present as the mode select information is transferred from this device during reset.

PROM 2 SIZE SELECT (M6, M7)

Mode register bits M6 and M7 select the address decode zone of CHIP SELECT #2. Connection of an external prom to this select output is optional.

| M6 | M7 | CHIP SELECT #2 DECODE RANGE |
|----|----|-----------------------------|
| 1 | 1 | 16K PROM : 0800-0FFF |
| 0 | 1 | 32K PROM: 0800-17FF |
| 1 | 0 | 64K PROM: 0800-27FF |
| 0 | 0 | 256K PROM: 0800-87FF |



* DEVICE 2 MAY BE AN EPROM, RAM, OR PERIPHERAL DEVICE SUCH AS MC146818

FIGURE 2 MC68HC25 SYSTEM CONFIGURATION

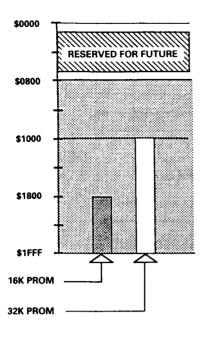


FIGURE 3
MC68HC25 PROM 1 DECODE FOR
8K MEMORY MAP OPERATION

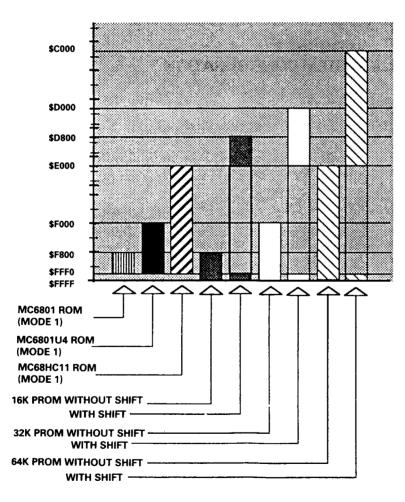


FIGURE 4
MC68HC25 PROM 1 DECODE FOR
64K MEMORY MAP OPERATION

ELECTRICAL SPECIFICATIONS

This section contains the electrical specification and related timing information for the MC68HC25.

MAXIMUM RATINGS (Vdd=5.0V (+/-10%), Vss=0V, Ta=-40°C to +85°C unless otherwise stated)

| Rating | Symbol | Value | Unit | |
|-----------------------------|--------|--------------------|------|--|
| Supply voltage | Vdd | -0.5 to 0.7 | V | |
| Input voltage | Vin | Vss-0.5 to Vdd+0.5 | V | |
| Current drain per pin | lik | 10 | mA | |
| Operating temperature range | Та | -40 to +85 | °C | |
| Storage temperature range | Tstg | −65 to +125 | °C | |

THERMAL CHARACTERISTICS

| Characteristics | Symbol | Value | Unit |
|--------------------------------|--------|-------|------|
| Thermal resistance 52 pin quad | θ ја | 50 | °C/W |

POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_{J} = T_{A} + (P_{D} \cdot \theta_{JA}) \tag{1}$$

Where:

Ambient Temperature °C

Package Thermal Resistance, Junction to Ambient °C/W

 P_D $P_{INT} + P_{I \setminus O}$

ICC x V_{CC}, Watts - Chip Internal Power Power Dissipation on Input and Output Pins - User Determined

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273^{\circ}C)$$
 (2)

Solving equations (1) and (2) for K gives:

$$K = P_D \cdot (T_A + 273^{\circ}C) + \theta_{JA} \cdot P_D^2$$
(3)

Where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) from a known T_A. Using this value of K the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of TA.

DC ELECTRIC CHARACTERISTICS

(Vdd=5.0V (+/-10%), Vss=0V, Ta=-40°C to +85°C unless otherwise stated)

| CHARACTERISTICS | Symbol | Min | Max | Unit |
|---|--------|-----------------|--------|------|
| Output low voltage @ lol = 2.0mA | Vol | | 0.5 | ٧ |
| Output high voltage (for IRQ and RESET OUT) lload = 0.1mA | Vohr | Vdd-0.8 | | ٧ |
| Output high voltage @ lol = 0.36mA | Voh | 4.1 | | ٧ |
| Input low voltage (TTL MODE) + RESET (CMOS MODE) | Vil | Vss | 0.8 | ٧ |
| Input high voltage (TTL MODE) (except RESET IN (CMOS MODE)) | Vih | 2.44 Vdd-2.0 | Vdd | ٧ |
| Input high voltage RESET IN | Vihr | 4.0 | Vdd | ٧ |
| Input leakage current PORT 3, A8-A15, E, AS, RW, RESET IN, IS3 | ldz | | +/- 10 | μА |
| Input current CS1, CS2, PORT 4 ADDRESS LOW/DATA @ RESET IN low | ldzz | | -150 | μА |
| Total supply current (tcyc=470ns) | ldd | | 350 | μА |
| Total capacitance* | Cin | | 12 | pF |

^{(*} Design specification value only - NOT tested)

BUS TIMING CHARACTERISTICS (Vdd=5.0V (+/-10%) Vss=0V Ta=-40°C to +85°C)

| ldent | | | 2.1 MHz | | |
|--------|---|---------|----------|-----|------|
| Number | Characteristics | Symbol | Min | Max | Unit |
| 1 | Cycle Time | tcyc | 476 | | ns |
| 213 | Pulse Width Low (high) | pwel(h) | 200(210) | | ns |
| 4 | E Clock Rise and Fall | tr,tf | | 25 | ns |
| 8 | R/W Hold Time | trwh | 10 | | ns |
| 12 | Non-Muxed Address Valid Time to E | tav | 70 | | ns |
| 13 | R/W Setup Time before E Rise | trws | 70 | | ns |
| 18 | Read Data Hold Time | tdhr | 10 | | ns |
| 21 | Write Data Hold Time | tdhw | 10 | | ns |
| 22 | A0-A7 Valid Time to E Rise | tavm | 75 | | ns |
| 24 | A0-A7 Setup Time before AS Fall | tfal | 20 | | ns |
| 25 | A0-A7 Hold Time after AS Fall | tahl | 10 | | ns |
| 26 | Delay Time E fall to AS rise | tasd | 50 | | ns |
| 27 | AS Pulse Width High | twash | 90 | | ns |
| 28 | Delay Time AS Fall to E Rise | tased | 50 | | ns |
| 29 | A0-A7 Output Delay see Note 2 | taod | | 90 | ns |
| 30 | Data Out Delay (read) | tddr | | 175 | ns |
| 31 | Data In Data Setup Time (write) | tdsw | 125 | | ns |
| 33 | Peripheral Data Setup Time | tpwsu | 100 | | ns |
| 34 | Peripheral Data Hold Time | tpdh | 100 | | ns |
| 35 | Input Data Hold Time | tih | 30 | | ns |
| 36 | Input Data Setup Time | tis | 40 | | ns |
| 37 | Input Strobe Pulse Width | tpwis | 100 | | ns |
| 38 | Delay Time, Peripheral Data Write | tpwd | | 210 | ns |
| 39 | Delay Time, Enable Positive Transition to OS3 Negative Transition | tosd1 | | 200 | ns |
| 40 | Delay Time, Enable Positive Transition to OS3 Positive Transition | tosd2 | | 200 | ns |
| 41 | Delay Time E Rise to CS1 / CS2 Asserted (Low) | tcsl | | 120 | ns |
| 42 | Delay Time E Fall to CS1 / CS2 Negated (High) | tcsh | | 120 | ns |
| 43 | Delay Time E Rise to IRQ Asserted (Low) | tirq | | 150 | ns |
| 44 | Delay Time E Rise to RSO Asserted (Low) | trso | | 200 | ns |
| 45 | Delay Time E Rise to RSO Negated (High) | trsh | | 200 | ns |

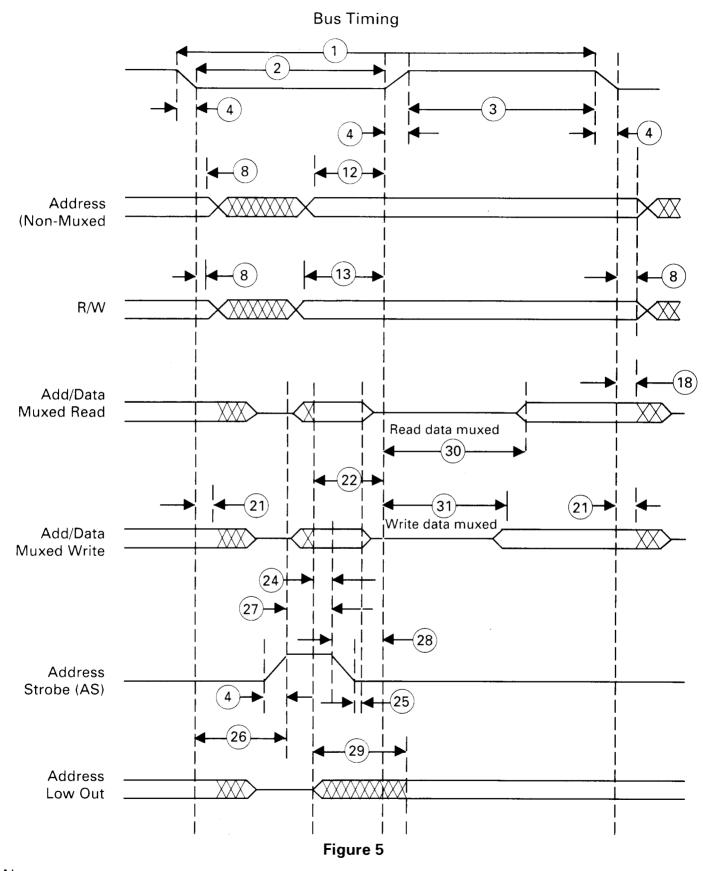
NOTES:

^{1.} All Timing is shown with respect to 20% VDD unless otherwise noted.

^{2.} VOH level measurement point is at 60% VDD.

TIMING CHARACTERISTICS

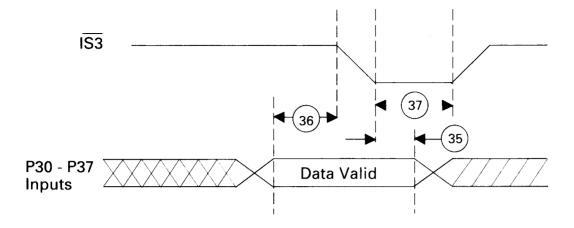
The external timing of the circuit is shown in figures 5 to 11



Note:

I. All Timing is shown with respect to 20% VDD and 70% VDD unless otherwise noted.

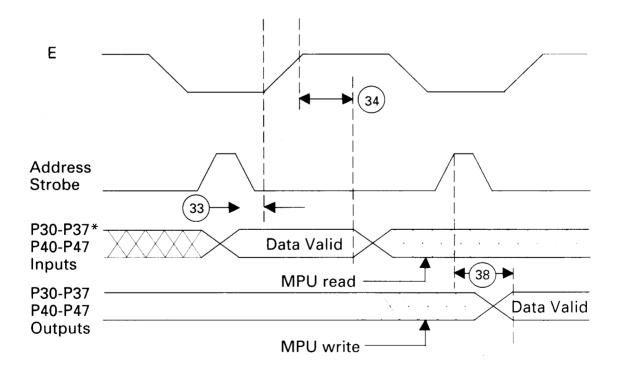
Port #3 Latch Timing



Port 3 latched operation

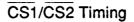
Figure 6

Data Setup/Hold times



Port 3 non-latched operation

Figure 7



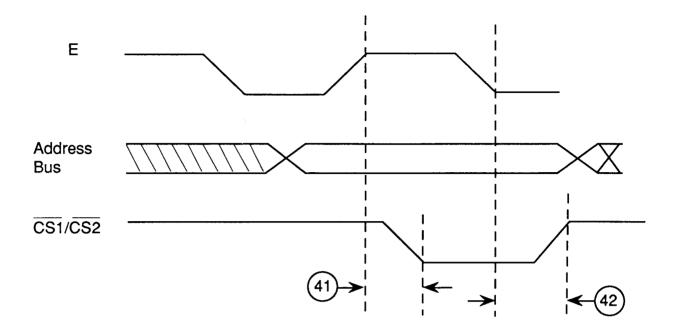
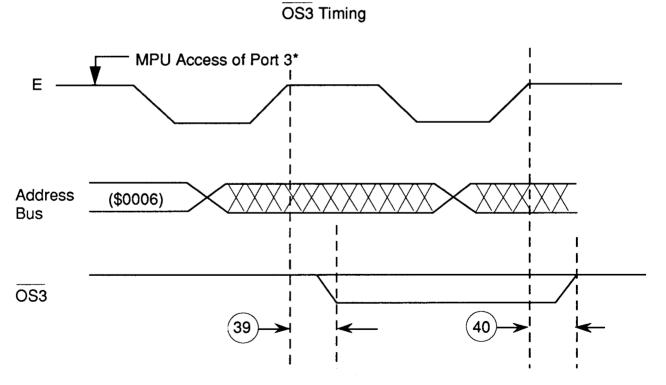


Figure 8



Access matches output strobe select (OSS = 0, a read; OSS = 1, a write)

Figure 9

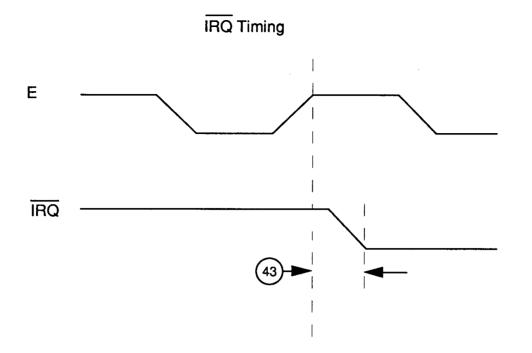


Figure 10

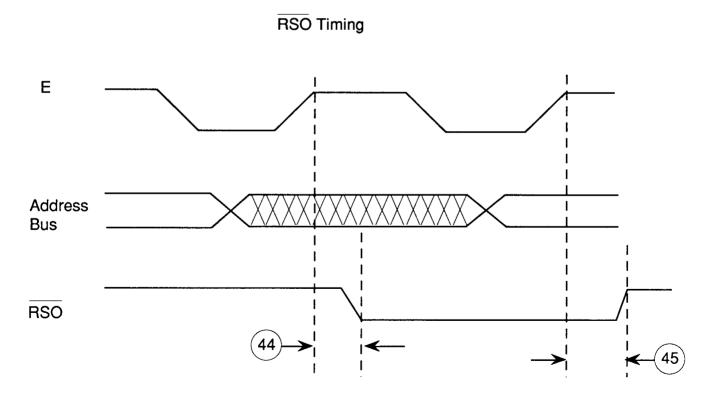


Figure 11

Mode Select Register Load Sequence

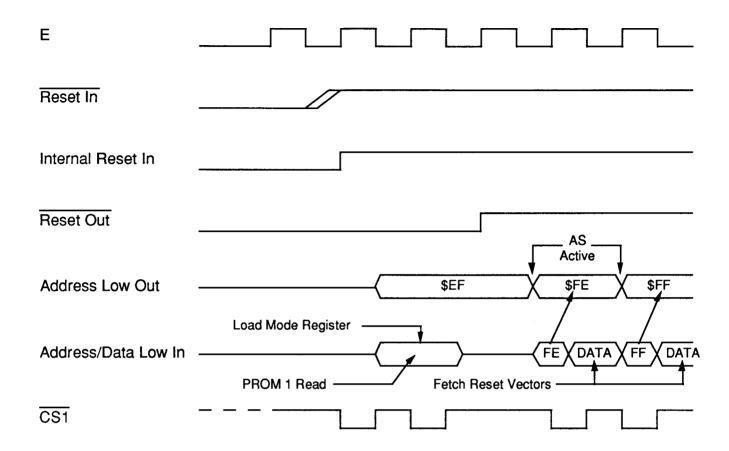


Figure 12

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