



SANYO Semiconductors
DATA SHEET

LC87F54C8A

CMOS IC
 FROM 128K-byte, RAM 4K-byte on chip
8-bit 1-chip Microcontroller

Overview

The LC87F54C8A is 8-bit single chip microcontroller with the following one-chip features :

- CPU : Operable at a minimum bus cycle time of 100ns
- On-chip Flash ROM Capacity : 128K bytes (on-board rewritable)
- On-chip RAM Capacity : 4K bytes
- Two high performance 16-bit timer/counters (can be divided into 8-bit timers)
- Four 8-bit timers with prescalers
- Timer for use as date/time clock
- Two synchronous serial I/O ports (with automatic block transmit/receive function)
- One asynchronous/synchronous serial I/O port
- 12-bit PWM × 2
- 12-channel × 8-bit AD converter
- High speed 8-bit parallel interface
- High speed clock counter
- System clock divider
- 21-source 10-vectored interrupt system

Features

- Read Only Memory (Flash ROM)
 - Single 5V power supply, on-board writeable
 - Block erase in 128 byte units
 - 131071 × 8 bits (LC87F54C8A)
- Bus Cycle Time
 - 100ns (10MHz)
 Note : Bus cycle time indicates the speed to read ROM.
- Minimum Instruction Cycle Time (tCYC)
 - 300ns (10MHz)

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■ Ports

- Input/output ports
Input/output programmable for each bit individually 59 (P1n, P2n, P3n, P70 to P73, P8n, PAn, PBn, PCn, S2Pn)
Data direction programmable in nibble units 8 (P0n)
- Input ports 2 (XT1, XT2)
- PWM output ports 2 (PWM0, PWM1)
- Oscillator pins 2 (CF1, CF2)
- Reset pin 1 (RES)
- Power supply 8 (VSS1 to 3, VDD1 to 3)

■ Timer

- Timer 0 : 16-bit timer/counter with capture register
 - Mode 0 : Two 8-bit timers with programmable 8-bit prescaler and 8-bit capture register
 - Mode 1 : 8-bit timer with 8-bit programmable prescaler and 8-bit capture register + 8-bit counter with 8-bit capture register
 - Mode 2 : 16-bit timer with 8-bit programmable prescaler and 16-bit capture register
 - Mode 3 : 16-bit counter with 16-bit capture register
- Timer 1 : PWM/16-bit timer/counter with toggle output
 - Mode 0 : 8-bit timer (with toggle output) + 8-bit timer/counter (with toggle output)
 - Mode 1 : Two 8-bit PWM
 - Mode 2 : 16-bit timer/counter (with toggle output) Toggle output is also possible by using the lower order 8-bits
 - Mode 3 : 16-bit timer (with toggle output) The lower order 8 bits can be used as PWM output.
- Timer 4 : 8-bit timer with 6-bit prescaler
- Timer 5 : 8-bit timer with 6-bit prescaler
- Timer 6 : 8-bit timer with 6-bit prescaler
- Timer 7 : 8-bit timer with 6-bit prescaler

• Base timer

1. Clock for the base timer is selectable from sub-clock (32.768kHz crystal oscillation), system clock or programmable prescaler output of timer 0.
2. There can be five separate interrupt sources.

■ High speed clock counter

1. Maximum of 20MHz possible (when using a 10MHz main clock).
2. Real-time output.

■ Serial interface

- SIO0 : 8-bit synchronous serial interface
 1. LSB first/MSB first-function available
 2. An internal 8-bit baud-rate generator (maximum transmit clock period 4/3 tCYC)
 3. Consecutive automatic data communication (1 to 256 bits)
- SIO1 : 8-bit asynchronous/synchronous serial interface
 - Mode 0 : Synchronous 8-bit serial I_O (2-wire or 3-wire, transmit clock 2 to 512 tCYC)
 - Mode 1 : Asynchronous serial I_O (half duplex, 8 data bits, 1 stop bit, baud-rate 8 to 2048 tCYC)
 - Mode 2 : Bus mode 1 (start bit, 8 data bits, transmit clock 2 to 512 tCYC)
 - Mode 3 : Bus mode 2 (start detection, 8 data bits, stop detection)
- SIO2 : 8-bit synchronous serial interface
 1. LSB-first
 2. Internal 8-bit baud-rate generator (maximum transmit clock period 4/3 tCYC)
 3. Consecutive automatic data communication (1 to 32 bytes)

■AD converter

- 12-channel × 8-bit AD converter

■PWM

- 2 channel × synchronous variable 12 bit PWM

■Parallel interface

- RS, RD, WR, CS0 to CS2 outputs (polarity can be toggled)
- Read/write possible in 1 tCYC

■Remote receiver circuit (share with P73/INT3/T0IN terminal)

- Noise rejection function (The filtering time of the noise rejection filter (1 tCYC/32 tCYC /128 tCYC) can be switched by program.)

■Watchdog timer

- External RC circuit is required.
- Interrupt or system reset is activated when the timer overflows.

■Interrupts

- 21-source and 10-vectored interrupt function :
 1. Three interrupt priorities, low (L), high (H) and highest (X) are supported with multi-level nesting possible. During interrupt handling, an equal or lower level interrupt request is refused.
 2. If interrupt requests for two or more vector addresses occur at once, the higher level interrupt takes precedence. In the case of equal priority levels, the vector with the lowest address takes precedence.

No.	Vector	Selectable Level	Interrupt Signal
1	00003H	X or L	INT0
2	0000BH	X or L	INT1
3	00013H	H or L	INT2/T0L/INT4
4	0001BH	H or L	INT3/INT5/Base timer
5	00023H	H or L	T0H
6	0002BH	H or L	T1L/T1H
7	00033H	H or L	SIO0
8	0003BH	H or L	SIO1/SIO2
9	00043H	H or L	ADC/T6/T7
10	0004BH	H or L	Port 0/T4/T5/PWM0, PWM1

- Priority Level : X > H > L
- For equal priority levels, vector with lowest address takes precedence.

■Subroutine stack levels

- A maximum of 2048 levels (set stack inside RAM)

■Multiplication and division

- 16-bits × 8-bits (5 instruction-cycle times)
- 24-bits × 16-bits (12 instruction-cycle times)
- 16-bits ÷ 8-bits (8 instruction-cycle times)
- 24-bits ÷ 16-bits (12 instruction-cycle times)

■Oscillation circuits

- Built-in RC oscillation circuit used for the system clock
- CF oscillation circuit used for the system clock
- Crystal oscillation circuit used for the system clock

■System clock divider

- Operable on the lowest power consumption
- Minimum instruction cycle time 300ns, 600ns, 1.2μs, 4.8μs, 9.6μs, 19.2μs, 38.4μs, 76.8μs can be switched by program (when using 10MHz main clock)

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■ Standby function

• HALT mode

The HALT mode stops program execution while the peripheral circuits keep operating and minimizes power consumption. This operation mode can be released by a system reset or an interrupt request.

• HOLD mode

The HOLD mode stops program execution and all oscillation circuits : CF, RC and Crystal oscillations. This mode can be released by the following conditions.

1. Supply "L" level to the reset terminal (RES)
2. Supply the selected level to at least one of INT0, INT1, INT2, INT4, INT5.
3. Supply an interrupt condition to Port 0.

• X'tal HOLD mode

The X'tal HOLD mode stops program execution and all peripheral circuits except for the base timer.

The crystal oscillator maintains its state at HOLD mode inception. This mode can be released by the following conditions.

1. Supply "L" level to the reset terminal ($\overline{\text{RES}}$).
2. Supply the selected level to at least one of INT0, INT1, INT2, INT4, INT5
3. Supply an interrupt condition to Port 0.
4. Supply an interrupt condition to the base timer circuit.

■ Shipping form

- QFP80E
- TQFP80

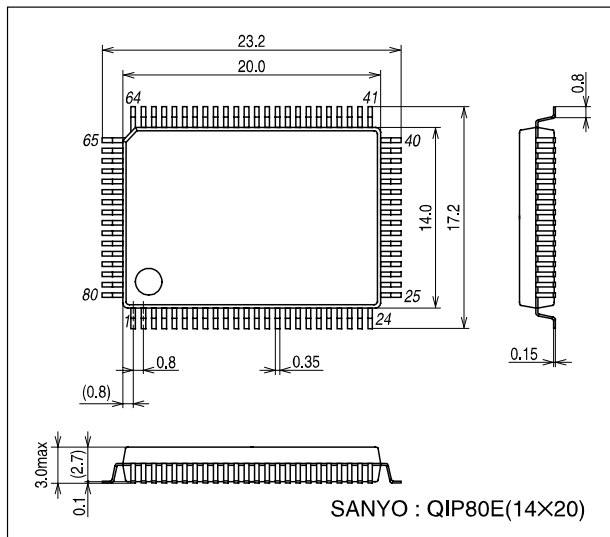
■ Development tools

- Evaluation (EVA) chip : LC876093
- Emulator : EVA62S + ECB876600A + SUB875400 + POD80QFP or POD80SQFP
- Flash ROM writer adapter : W87F54256Q (QIP80E), W87F54256SQ (TQFP80)

Package Dimensions

unit : mm

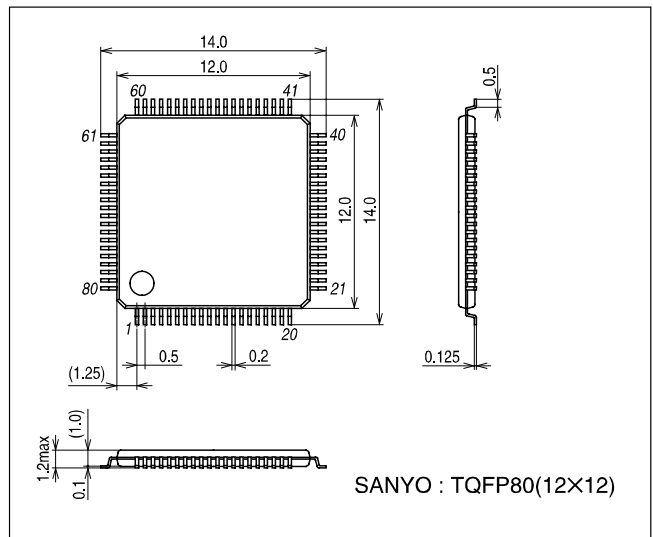
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Package Dimensions

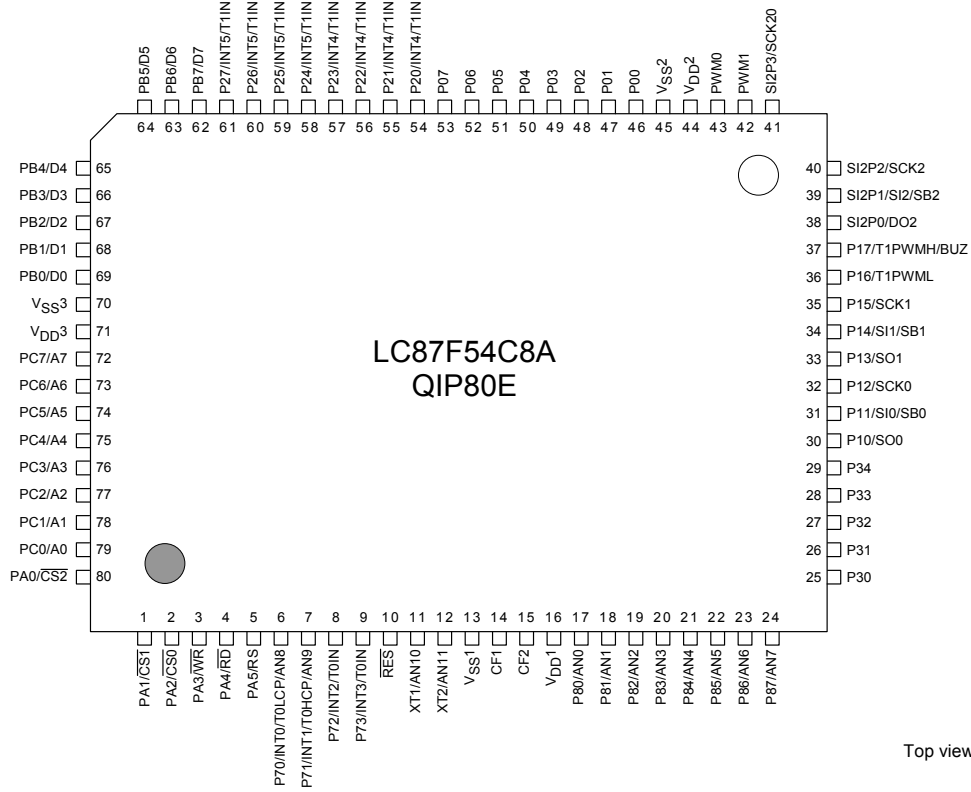
unit : mm

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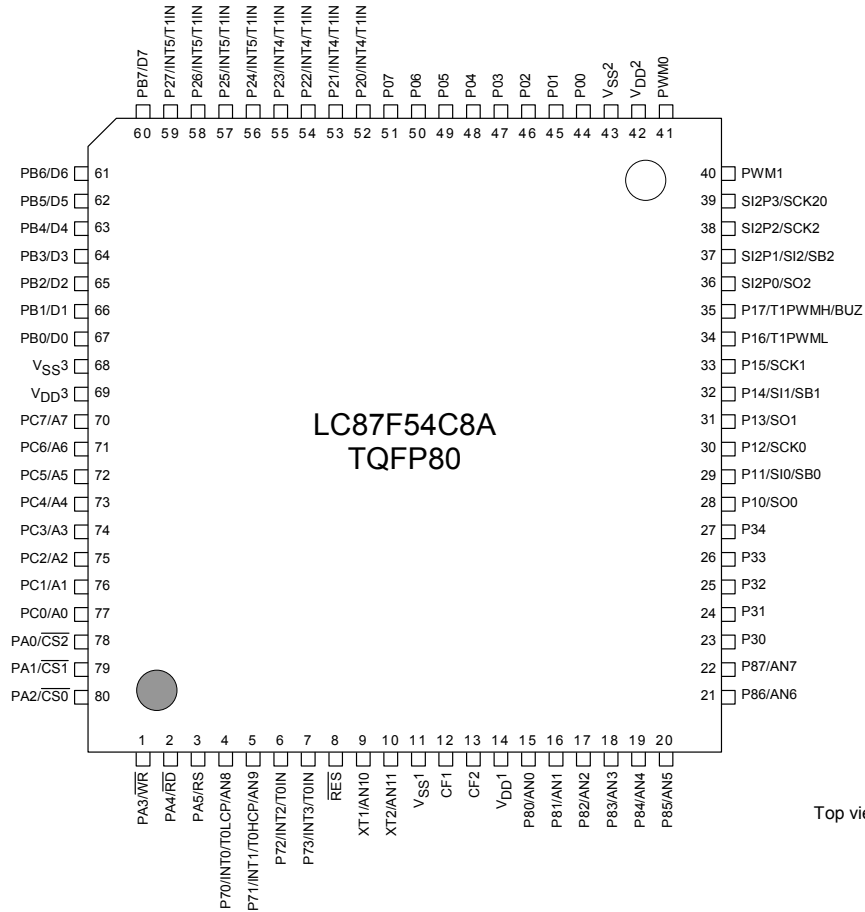


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Pin Assignment



Top view



Top view

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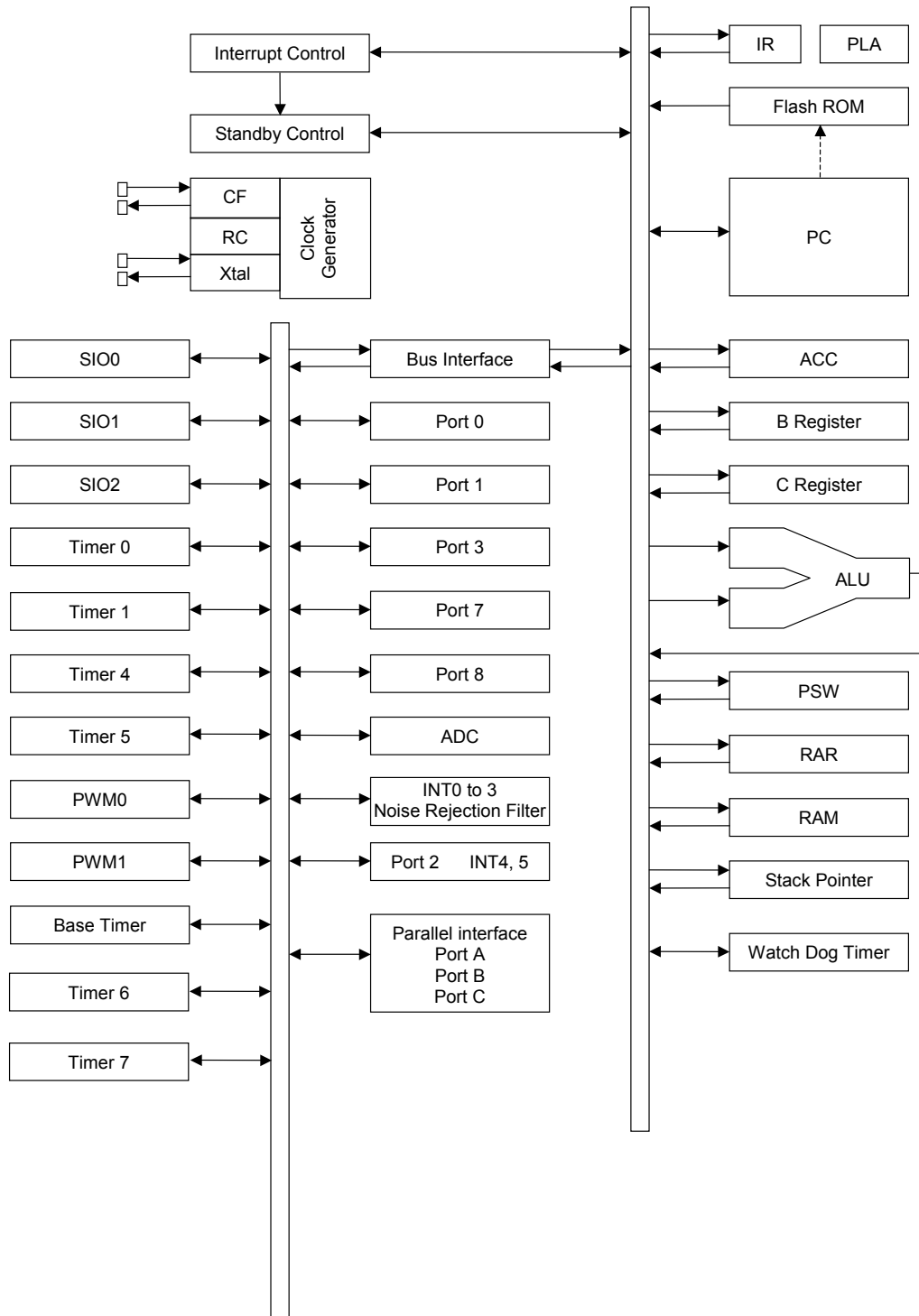
PAD Coordinate Values

QIP	NAME	TQFP
1	PA1/ $\overline{CS1}$	79
2	PA2/ $\overline{CS0}$	80
3	PA3/ \overline{WR}	1
4	PA4/ \overline{RD}	2
5	PA5/ \overline{RS}	3
6	P70/INT0/T0LCP/AN8	4
7	P71/INT1/T0HCP/AN9	5
8	P72/INT2/T0IN	6
9	P73/INT3/T0IN	7
10	\overline{RES}	8
11	XT1/AN10	9
12	XT2/AN11	10
13	V _{SS1}	11
14	CF1	12
15	CF2	13
16	V _{DD1}	14
17	P80/AN0	15
18	P81/AN1	16
19	P82/AN2	17
20	P83/AN3	18
21	P84/AN4	19
22	P85/AN5	20
23	P86/AN6	21
24	P87/AN7	22
25	P30	23
26	P31	24
27	P32	25
28	P33	26
29	P34	27
30	P10/SO0	28
31	P11/SI0/SB0	29
32	P12/SCK0	30
33	P13/SO1	31
34	P14/SI1/SB1	32
35	P15/SCK1	33
36	P16/T1PWML	34
37	P17/T1PVMH/BUZ	35
38	SI2P0/SO2	36
39	SI2P1/SI2/SB2	37
40	SI2P2/SCK2	38

QIP	NAME	TQFP
41	SI2P3/SCK20	39
42	PWM1	40
43	PWM0	41
44	V _{DD2}	42
45	V _{SS2}	43
46	P00	44
47	P01	45
48	P02	46
49	P03	47
50	P04	48
51	P05	49
52	P06	50
53	P07	51
54	P20/INT4/T1IN	52
55	P21/INT4/T1IN	53
56	P22/INT4/T1IN	54
57	P23/INT4/T1IN	55
58	P24/INT5/T1IN	56
59	P25/INT5/T1IN	57
60	P26/INT5/T1IN	58
61	P27/INT5/T1IN	59
62	PB7/D7	60
63	PB6/D6	61
64	PB5/D5	62
65	PB4/D4	63
66	PB3/D3	64
67	PB2/D2	65
68	PB1/D1	66
69	PB0/D0	67
70	V _{SS3}	68
71	V _{DD3}	69
72	PC7/A7	70
73	PC6/A6	71
74	PC5/A5	72
75	PC4/A4	73
76	PC3/A3	74
77	PC2/A2	75
78	PC1/A1	76
79	PC0/A0	77
80	PA0/ $\overline{CS2}$	78

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System Block Diagram



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Pin Description

Pin name	I/O	Function	Option																														
V _{SS} 1, V _{SS} 2, V _{SS} 3	-	Power terminal (-)	No																														
V _{DD} 1, V _{DD} 2, V _{DD} 3	-	Power terminal (+)	No																														
Port 0 P00 to P07	I/O	<ul style="list-style-type: none"> 8-bit input/output port Data direction programmable in nibble units Pull-up resistor provided/not provided (specified in nibble units) HOLD release input Port 0 interrupt input 	Yes																														
Port 1 P10 to P17	I/O	<ul style="list-style-type: none"> 8-bit input/output port Data direction programmable for each bit individually Pull-up resistor provided/not provided (specified by bit) Other functions <ul style="list-style-type: none"> P10 : SIO0 data output P11 : SIO0 data input, bus input/output P12 : SIO0 clock input/output P13 : SIO1 data output P14 : SIO1 data input, bus input/output P15 : SIO1 clock input/output P16 : Timer 1 PWML output P17 : Timer 1 PWMH output/Buzzer output 	Yes																														
Port 2 P20 to P27	I/O	<ul style="list-style-type: none"> 8-bit input/output port Data direction programmable for each bit individually Pull-up resistor provided/not provided (specified by bit) Other functions <ul style="list-style-type: none"> P20 to P23 : INT4 input/HOLD release input/Timer 1 event input/Timer 0L capture input/Timer 0H capture input P24 to P27 : INT5 input/HOLD release input/Timer 1 event input/Timer 0L capture input/Timer 0H capture input Interrupt detection style <table border="1" style="margin-left: 20px;"> <thead> <tr> <th></th> <th>Rising</th> <th>Falling</th> <th>Rising/ falling</th> <th>H level</th> <th>L level</th> </tr> </thead> <tbody> <tr> <td>INT4</td> <td>enable</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>disable</td> </tr> <tr> <td>INT5</td> <td>enable</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>disable</td> </tr> </tbody> </table> 		Rising	Falling	Rising/ falling	H level	L level	INT4	enable	enable	enable	disable	disable	INT5	enable	enable	enable	disable	disable	Yes												
	Rising	Falling	Rising/ falling	H level	L level																												
INT4	enable	enable	enable	disable	disable																												
INT5	enable	enable	enable	disable	disable																												
Port 3 P30 to P34	I/O	<ul style="list-style-type: none"> 5-bit input/output port Data direction programmable for each bit individually Pull-up resistor provided/not provided (specified by bit) 	Yes																														
Port 7 P70 to P73	I/O	<ul style="list-style-type: none"> 4-bit input/output port Data direction programmable for each bit individually Pull-up resistor provided/not provided (specified by bit) Other functions <ul style="list-style-type: none"> P70 : INT0 input/HOLD release input/Timer 0L capture input/Output for watchdog timer P71 : INT1 input/HOLD release input/Timer 0H capture input P72 : INT2 input/HOLD release input/Timer 0 event input/Timer 0L capture input P73 : INT3 input with noise filter/Timer 0 event input/Timer 0H capture input Interrupt detection style <table border="1" style="margin-left: 20px;"> <thead> <tr> <th></th> <th>Rising</th> <th>Falling</th> <th>Rising/ falling</th> <th>H level</th> <th>L level</th> </tr> </thead> <tbody> <tr> <td>INT0</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>enable</td> <td>enable</td> </tr> <tr> <td>INT1</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>enable</td> <td>enable</td> </tr> <tr> <td>INT2</td> <td>enable</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>disable</td> </tr> <tr> <td>INT3</td> <td>enable</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>disable</td> </tr> </tbody> </table> <p>• AD converter input port : AN8 (P70), AN9 (P71)</p>		Rising	Falling	Rising/ falling	H level	L level	INT0	enable	enable	disable	enable	enable	INT1	enable	enable	disable	enable	enable	INT2	enable	enable	enable	disable	disable	INT3	enable	enable	enable	disable	disable	No
	Rising	Falling	Rising/ falling	H level	L level																												
INT0	enable	enable	disable	enable	enable																												
INT1	enable	enable	disable	enable	enable																												
INT2	enable	enable	enable	disable	disable																												
INT3	enable	enable	enable	disable	disable																												

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Pin name	I/O	Function	Option
Port 8 P80 to P87	I/O	<ul style="list-style-type: none"> • 8-bit input/output port • Data direction programmable for each bit individually • Other functions P80 to P87 : AD converter input port	No
Port A PA0 to PA5	I/O	<ul style="list-style-type: none"> • 6-bit input/output port • Data direction programmable for each bit individually • Pull-up resistor provided/not provided (specified by bit) • Other functions PA0 : Parallel interface output $\overline{CS2}$ PA1 : Parallel interface output $\overline{CS1}$ PA2 : Parallel interface output $\overline{CS0}$ PA3 : Parallel interface output \overline{WR} PA4 : Parallel interface output \overline{RD} PA5 : Parallel interface output RS	Yes
Port B PB0 to PB7	I/O	<ul style="list-style-type: none"> • 8-bit input/output port • Data direction programmable for each bit individually • Pull-up resistor provided/not provided (specified by bit) • Other functions PB0 to PB7 : Parallel interface data input/output, address output	Yes
Port C PC0 to PC7	I/O	<ul style="list-style-type: none"> • 8-bit input/output port • Data direction programmable for each bit individually • Pull-up resistor provided/not provided (specified by bit) • Other functions PC0 to PC7 : Parallel interface address output	Yes
SIO2 Port SI2P0 to SI2P3	I/O	<ul style="list-style-type: none"> • 4-bit input/output port • Data direction programmable for each bit individually • Other functions SI2P0 : SIO2 data output SI2P1 : SIO2 data input, bus input/output SI2P2 : SIO2 clock input/output SI2P3 : SIO2 clock output	No
PWM0	O	PWM0 output port	No
PWM1	O	PWM1 output port	No
\overline{RES}	I	Reset terminal	No
XT1	I	<ul style="list-style-type: none"> • Input terminal for 32.768kHz X'tal oscillation • Other function AN10 : AD converter input port General input port When not in use, connect terminal to V_{DD1} .	No
XT2	I/O	<ul style="list-style-type: none"> • Output terminal for 32.768kHz X'tal oscillation • Other function AN11 : AD converter input port General input port When not in use, set as oscillation and leave terminal open	No
CF1	I	Input terminal for ceramic resonator	No
CF2	O	Output terminal for ceramic resonator	No

Port Output Configuration

Output configuration and pull-up resistor options are shown in the following table.
Input is possible even when a port is in output mode.

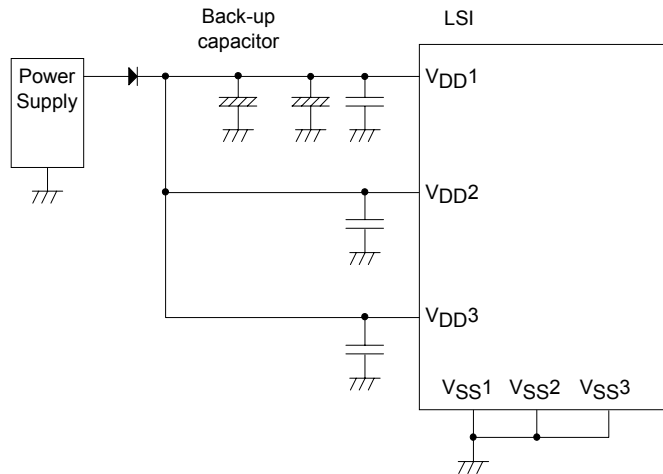
Terminal	Option applies to :	Option	Output Format	Pull-up resistor
P00 to P07	each bit	1	CMOS	Programmable (Note 1)
		2	Nch-open drain	None
P10 to P17 P20 to P27 P30 to P36	each bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
PA0 to PA5 PB0 to PB7(*) PC0 to PC7	each bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P70	-	None	Nch-open drain	Programmable
P71 to P73	-	None	CMOS	Programmable
P80 to P87	-	None	Nch-open drain	None
SI2P0, SI2P2 SI2P3 PWM0, PWM1	-	None	CMOS	None
SI2P1	-	None	CMOS (When used as general port) Nch-open drain (When used for SIO2 data)	None
XT1	-	None	Input only	None
XT2	-	None	Output for 32.768kHz crystal oscillation	None

Note 1 : Programmable pull-up resistor of Port 0 is specified in nibble units (P00 to P03, P04 to P07).

(*) When in parallel interface mode, PB0 to PB7 output format is CMOS, regardless of any selected option.

Note : To reduce V_{DD} signal noise and to increase the duration of the backup battery supply, V_{SS1}, V_{SS2} and V_{SS3} should connect to each other and they should also be grounded.

Example 1 : During backup in hold mode, port output "H" level is supplied from the back-up capacitor.

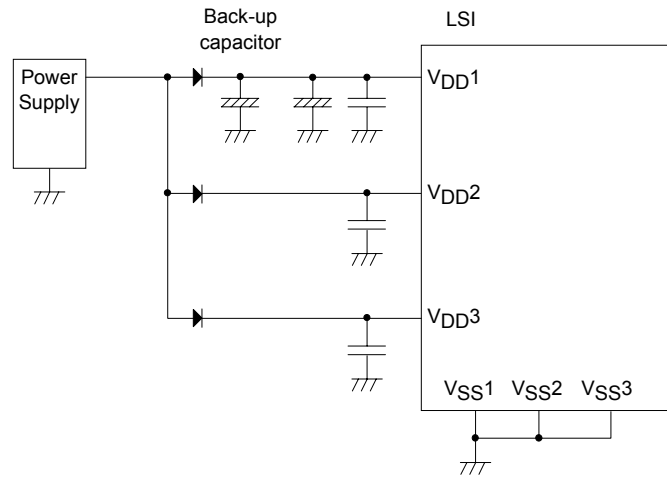


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Example 2 : During backup in hold mode, output is not held high and its value is unsettled.



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Absolute Maximum Ratings / $T_a = 25^\circ\text{C}$, $V_{SS1} = V_{SS2} = V_{SS3} = 0\text{V}$

Parameter	Symbol	Pins	Conditions	V_{DD} [V]	Limits			unit	
					min	typ	max		
Supply voltage	V_{DD} max	V_{DD1} , V_{DD2} , V_{DD3}	$V_{DD1} = V_{DD2} = V_{DD3}$		-0.3		+6.5	V	
Input voltage	$V_I(1)$	XT1, XT2, CF1			-0.3		$V_{DD}+0.3$		
Output voltage	$V_O(1)$	PWM0, PWM1			-0.3		$V_{DD}+0.3$		
Input/Output voltage	$V_{IO}(1)$	<ul style="list-style-type: none"> • Ports 0, 1, 2 • Ports 3, 7, 8 • Ports A, B, C • SI2P00 to SI2P03 • PWM0, PWM1 			-0.3		$V_{DD}+0.3$		
High level output current	Peak output current	IOPH(1)	<ul style="list-style-type: none"> • Ports 0, 1, 2, 3 • Ports A, B, C • SI2P00 to SI2P03 • PWM0, PWM1 	<ul style="list-style-type: none"> • CMOS output • For each pin. 			-10	mA	
		IOPH(2)	P71 to P73	For each pin.			-5		
	Total output current	Σ IOAH(1)	P71 to P73	Total of all pins					-5
		Σ IOAH(2)	<ul style="list-style-type: none"> • Port 1 • PWM0, PWM1 • Port 3 • SI2P00 to SI2P03 	Total of all pins					-30
		Σ IOAH(3)	Ports 0, 2	Total of all pins					-20
		Σ IOAH(4)	Port B	Total of all pins					-20
		Σ IOAH(5)	Ports A, C	Total of all pins					-20
Low level output current	Peak output current	IOPL(1)	<ul style="list-style-type: none"> • P02 to P07 • Ports 1, 2, 3 • Ports A, B, C • SI2P00 to SI2P03 • PWM0, PWM1 	For each pin.				20	
		IOPL(2)	P00, P01	For each pin.				30	
		IOPL(3)	Ports 7, 8	For each pin.				5	
	Total output current	Σ IOAL(1)	Port 7	Total of all pins				15	
		Σ IOAL(2)	Port 8	Total of all pins				15	
		Σ IOAL(3)	<ul style="list-style-type: none"> • Port 1 • PWM0, PWM1 • Port 3 • SI2P00 to SI2P03 	Total of all pins				50	
		Σ IOAL(4)	Ports 0, 2	Total of all pins				70	
		Σ IOAL(5)	Port B	Total of all pins				40	
		Σ IOAL(6)	Ports A, C	Total of all pins				40	
	Maximum power consumption	Pd max	QIP80E	$T_a = -20$ to $+70^\circ\text{C}$				395	mW
TQFP80							343		
Operating temperature range	Topr				-20		70	$^\circ\text{C}$	
Storage temperature range	Tstg				-55		125		

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Recommended Operating Range / $T_a = -20^{\circ}\text{C}$ to $+70^{\circ}\text{C}$, $V_{SS1} = V_{SS2} = V_{SS3} = 0\text{V}$

Parameter	Symbol	Pins	Conditions	Limits				unit
				V_{DD} [V]	min	typ	max	
Operating supply voltage range	$V_{DD}(1)$	$V_{DD1} = V_{DD2} = V_{DD3}$	$0.294\mu\text{s} \leq t_{CYC} \leq 200\mu\text{s}$		4.5		5.5	V
			$0.588\mu\text{s} \leq t_{CYC} \leq 200\mu\text{s}$ Except for on-board rewriting		2.5		5.5	
HOLD voltage	VHD	$V_{DD1} = V_{DD2} = V_{DD3}$	RAM and register data are kept in HOLD mode.		2.0		5.5	
Input high voltage	$V_{IH}(1)$	<ul style="list-style-type: none"> • Ports 1, 2 • SI2P00 to 03 • P71 to P73 • P70 port input/interrupt 		2.5 to 5.5	$0.3V_{DD} + 0.7$		V_{DD}	
	$V_{IH}(2)$	<ul style="list-style-type: none"> • Ports 0, 8, 3 • Ports A, B, C 		2.5 to 5.5	$0.3V_{DD} + 0.7$		V_{DD}	
	$V_{IH}(3)$	Port 70 Watchdog timer		2.5 to 5.5	$0.9V_{DD}$		V_{DD}	
	$V_{IH}(4)$	XT1, XT2, CF1, $\overline{\text{RES}}$		2.5 to 5.5	$0.75V_{DD}$		V_{DD}	
Input low voltage	$V_{IL}(1)$	<ul style="list-style-type: none"> • Ports 1, 2 • SI2P00 to 03 • P71 to P73 • P70 port input/interrupt 		2.5 to 5.5	V_{SS}		$0.1V_{DD} + 0.4$	
	$V_{IL}(2)$	<ul style="list-style-type: none"> • Ports 0, 8, 3 • Ports A, B 		2.5 to 5.5	V_{SS}		$0.15V_{DD} + 0.4$	
	$V_{IL}(3)$	Port 70 Watchdog timer		2.5 to 5.5	V_{SS}		$0.8V_{DD} - 1.0$	
	$V_{IL}(4)$	XT1, XT2, CF1, $\overline{\text{RES}}$		2.5 to 5.5	V_{SS}		$0.25V_{DD}$	
Operation cycle time	t_{CYC}			4.5 to 5.5	0.294		200	μs
			Except for on-board rewriting	2.5 to 5.5	0.588		200	
External system clock frequency	FEXCF(1)	CF1	<ul style="list-style-type: none"> • Leave CF2 pin open • System clock divider set to 1/1 • External clock DUTY = $50 \pm 5\%$ 	4.5 to 5.5	0.1		10	MHz
			<ul style="list-style-type: none"> • Leave CF2 pin open • System clock divider set to 1/1 • External clock DUTY = $50 \pm 5\%$ 	2.5 to 5.5	0.1		5	
			<ul style="list-style-type: none"> • Leave CF2 pin open • System clock divider set to 1/2 	4.5 to 5.5	0.2		20.4	
			<ul style="list-style-type: none"> • Leave CF2 pin open • System clock divider set to 1/2 	2.5 to 5.5	0.1		10	
Oscillation frequency range (Note1)	$F_{mCF}(1)$	CF1, CF2	10MHz ceramic resonator oscillation Refer to figure 1	4.5 to 5.5		10		kHz
	$F_{mCF}(2)$	CF1, CF2	5MHz ceramic resonator oscillation Refer to figure 1	2.5 to 5.5		5		
	F_{mRC}		RC oscillation	2.5 to 5.5	0.3		2.0	
	$F_{sX'tal}$	XT1, XT2	32.768kHz crystal resonator oscillation Refer to figure 2	2.5 to 5.5		32.768		

Note 1 : The oscillation parameters are shown on Tables 1 and 2.

Note 2 : $V_{DD} \geq 4.5\text{V}$ is required for on-board flash ROM rewriting.

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Electrical Characteristics / Ta = -20°C to +70°C, VSS1 = VSS2 = VSS3 = 0V

Parameter	Symbol	Pins	Conditions	VDD [V]	Limits			unit	
					min	typ	max		
Input high current	I _{IH} (1)	<ul style="list-style-type: none"> • Ports 0, 1, 2 • Ports 3, 7, 8 • Ports A, B, C • SI2P00 to SI2P03 • $\overline{\text{RES}}$ • PWM0, PWM1 	<ul style="list-style-type: none"> • Output disable • Pull-up resistor OFF • V_{IN} = V_{DD} (including the off-leak current of the output Tr.) 	2.5 to 5.5			1	μA	
	I _{IH} (2)	XT1, XT2	<ul style="list-style-type: none"> • Using as an input port • V_{IN} = V_{DD} 	2.5 to 5.5			1		
	I _{IH} (3)	CF1	V _{IN} = V _{DD}	2.5 to 5.5			15		
Input low current	I _{IL} (1)	<ul style="list-style-type: none"> • Ports 0, 1, 2 • Ports 3, 7, 8 • Ports A, B, C • SI2P00 to SI2P03 • $\overline{\text{RES}}$ • PWM0, PWM1 	<ul style="list-style-type: none"> • Output disable • Pull-up resistor OFF • V_{IN} = V_{SS} (including the off-leak current of the output Tr.) 	2.5 to 5.5		-1		μA	
	I _{IL} (2)	XT1, XT2	<ul style="list-style-type: none"> • Using as an input port • V_{IN} = V_{SS} 	2.5 to 5.5		-1			
	I _{IL} (3)	CF1	V _{IN} = V _{SS}	2.5 to 5.5		-15			
Output high voltage	V _{OH} (1)	<ul style="list-style-type: none"> • Ports 0, 1, 2, 3 • Ports B, C 	I _{OH} = -1.0mA	4.5 to 5.5	V _{DD} -1			V	
	V _{OH} (2)	<ul style="list-style-type: none"> • SI2P00 to SI2P03 • PWM0, PWM1 	I _{OH} = -0.1mA	2.5 to 5.5	V _{DD} -0.5				
	V _{OH} (3)	Port A	I _{OH} = -5.0mA	4.5 to 5.5	V _{DD} -1				
	V _{OH} (4)		I _{OH} = -0.4mA	2.5 to 5.5	V _{DD} -0.5				
	V _{OH} (5)	Ports 71, 72, 73	I _{OH} = -0.4mA	4.5 to 5.5	V _{DD} -1				
Output low voltage	V _{OL} (1)	<ul style="list-style-type: none"> • Ports 0, 1, 2, 3 	I _{OL} = 10mA	4.5 to 5.5			1.5	V	
	V _{OL} (2)	<ul style="list-style-type: none"> • Ports B, C 	I _{OL} = 1.6mA	4.5 to 5.5			0.4		
	V _{OL} (3)	<ul style="list-style-type: none"> • SI2P00 to SI2P03 • PWM0, PWM1 	I _{OL} = 1mA	2.5 to 5.5			0.4		
	V _{OL} (4)	P00, P01	I _{OL} = 30mA	4.5 to 5.5			1.5		
	V _{OL} (5)	Ports 7, 8	I _{OL} = 1mA	2.5 to 5.5			0.4		
	V _{OL} (6)		I _{OL} = 1mA	2.5 to 5.5			0.4		
	V _{OL} (7)	Port A	I _{OL} = 15mA	4.5 to 5.5			1.5		
	V _{OL} (8)		I _{OL} = 2mA	2.5 to 5.5			0.4		
Pull-up resistor	R _{pu}	<ul style="list-style-type: none"> • Ports 0, 1, 2, 3 • Port 7 • Ports A, B, C 	V _{OH} = 0.9V _{DD}	2.5 to 5.5		15	40	70	kΩ
Hysteresis voltage	V _{HIS}	<ul style="list-style-type: none"> • $\overline{\text{RES}}$ • Port 1 • Port 2 • Port 7 • SIP00 to SIP03 		2.5 to 5.5			0.1V _{DD}		V
Pin capacitance	CP	All pins	<ul style="list-style-type: none"> • All pins except the measured terminal : V_{IN} = V_{SS} • f = 1MHz • Ta = 25°C 	2.5 to 5.5			10		pF

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Serial Input/Output Characteristics / $T_a = -20^{\circ}\text{C}$ to $+70^{\circ}\text{C}$, $V_{SS1} = V_{SS2} = V_{SS3} = 0\text{V}$

Parameter	Symbol	Pins	Conditions	V_{DD} [V]	Limits						
					min	typ	max	unit			
Serial clock	Input clock	Cycle	SCK0 (P12), SI2P2	Refer to figure 6	2.5 to 5.5	2			tCYC		
		Low level pulse width				tSCKL(1)	1				
						tSCKLA(1)	1				
		High level pulse width				tSCKH(1)	1				
						tSCKHA(1)	4 (SIO0) 5 (SIO2)				
	Output clock	SCK1 (P15)	Cycle	SCK0 (P12), SI2P2 SI2P3	Refer to figure 6	2.5 to 5.5	2			tSCK	
			Low level pulse width				tSCKL(2)	1			
							tSCKLA(2)	1			
			High level pulse width				tSCKH(2)	1			
							tSCKHA(2)	4/3			
								1/2			
Serial input	SCK1 (P15)	Cycle	SCK0 (P12), SI2P2 SI2P3	• CMOS output • Refer to figure 6	2.5 to 5.5	2			tCYC		
		Low level pulse width				tSCKL(3)	1/2				
						tSCKLA(3)	3/4				
		High level pulse width				tSCKH(3)	1				
						tSCKHA(3)	1/2				
							2				
Serial output	SCK1 (P15)	Cycle	SCK0 (P12), SI2P2 SI2P3	• CMOS output • Refer to figure 6	2.5 to 5.5	2			tSCK		
		Low level pulse width				tSCKL(4)	1/2				
						tSCKLA(4)	1/2				
		High level pulse width				tSCKH(4)	1/2				
						tSCKHA(4)	1/2				
							1/2				
Serial input	Data set-up time	tsDI	SB0 (P11), SB1 (P14), SI2P1 SIO, SI1	• Data set-up to SIOCLK • Data hold from SIOCLK • Refer to figure 6	2.5 to 5.5	0.03			μs		
	Data hold time	thDI				0.03					
Serial output	Output delay time	tdD0	SO0 (P10), SO1 (P13), SB0 (O11), SB1 (P14), SI2P0, SI2P1	• Data hold from SIOCLK • Time delay from SIOCLK trailing edge to the SO data change in the open drain • Refer to figure 6	2.5 to 5.5			1/3tCYC +0.05	μs		

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Parallel Input/Output Characteristics / Ta = -20°C to +70°C, VSS1 = VSS2 = VSS3 = 0V

Note : If Port A terminals will be used as RS, \overline{WR} , \overline{RD} or \overline{CS} , then it should be set to CMOS format by option data.
Refer to figures 8 and 9 for parallel output timing.

Parameter	Symbol	Pins	Conditions	V _{DD} [V]	Limits			
					min	typ	max	unit
Write cycle, Read cycle	tC(1)			2.5 to 5.5		1		tCYC
Address set-up time	tsA(1)	\overline{WR} (PA3), PB0 to PB7 \overline{RD} (PA4), PC0 to PC7	From address set-up until control signal changes	2.5 to 5.5	1/3tCYC -30ns			tCYC & ns
	tsA(2)	\overline{RD} (PA4), PC0 to PC7		2.5 to 5.5	2/3tCYC -30ns			
Address hold time	thA(1)	\overline{RD} (PA4), PC0 to PC7	From change of \overline{RD} until address change	2.5 to 5.5	1/6tCYC			
	thA(2)	\overline{WR} (PA3), PC0 to PC7	From change of \overline{WR} until address change	2.5 to 5.5	5			ns
RS set-up time	tsRS(1)	\overline{WR} (PA3), RS(PA5), \overline{CS} (PAX)	From change of RS, \overline{CS} until change in \overline{WR}	2.5 to 5.5	1/6tCYC -15ns			tCYC & ns
	tsRS(2)	\overline{RD} (PA4), RS(PA5)	From change of RS until change in \overline{RD}	2.5 to 5.5	1/6tCYC -15ns			
	tsRS(3)	\overline{RD} (PA4), RS(PA5)		2.5 to 5.5	1/3tCYC -15ns			
\overline{CS} set-up time	tsCS(1)	\overline{RD} (PA4), \overline{CS} (PAX)	From change in \overline{CS} until change in \overline{RD}	2.5 to 5.5	1/3tCYC -15ns			
	tsCS(2)	\overline{WR} (PA3), \overline{CS} (PAX)	From change in \overline{CS} until change in \overline{WR}	2.5 to 5.5	2/3tCYC -15ns			
RS hold time	thRS(1)	\overline{WR} (PA3), RS(PA5)	From change in \overline{WR} until change in RS	2.5 to 5.5	0			ns
	thRS(2)	\overline{RD} (PA4), RS(PA5), \overline{CS} (PAX)	From change in \overline{RD} until change in RS, \overline{CS}	2.5 to 5.5	1/6tCYC			tCYC & ns
	thRS(3)	\overline{RD} (PA4), RS(PA5), \overline{CS} (PAX)		2.5 to 5.5	0			ns
\overline{CS} hold time	thCS(1)	\overline{RD} (PA4), RS(PA5)	From change in \overline{RD} until change in \overline{CS}	2.5 to 5.5	1/6tCYC			tCYC & ns
	thCS(2)	\overline{WR} (PA3), RS(PA5)	From change in \overline{WR} until change in \overline{CS}	2.5 to 5.5	0			ns
\overline{WR} "H" pulse width	tWRH(1)	\overline{WR} (PA3)		2.5 to 5.5	1/6tCYC -5ns	1/6tCYC		tCYC & ns
	tWRH(2)	\overline{WR} (PA3)		2.5 to 5.5	2/3tCYC -5ns	2/3tCYC		
\overline{WR} "L" pulse width	tWRL(1)	\overline{WR} (PA3)		2.5 to 5.5	1/6tCYC -5ns	1/6tCYC		
	tWRL(2)	\overline{WR} (PA3)		2.5 to 5.5	1/3tCYC -5ns	1/3tCYC		
\overline{RD} "H" pulse width	tRDH(1)	\overline{RD} (PA4)		2.5 to 5.5	1/6tCYC -5ns	1/6tCYC		
	tRDH(2)	\overline{RD} (PA4)		2.5 to 5.5	1/3tCYC -5ns	1/3tCYC		
\overline{RD} "L" pulse width	tRDL(1)	\overline{RD} (PA4)		2.5 to 5.5	1/3tCYC -5ns	1/3tCYC		
	tRDL(2)	\overline{RD} (PA4)		2.5 to 5.5	1/2tCYC -5ns	1/2 tCYC		

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Continued from preceding page.

Parameter	Symbol	Pins	Conditions	Limits				
				V _{DD} [V]	min	typ	max	unit
Data write maximum delay	tdDT(1)	\overline{RD} (PA4), PB0 to PB7	The time delay allowed, from \overline{RD} leading edge until input data set-up (Note 1)	2.5 to 5.5			1/6tCYC -15ns	tCYC & ns
	tdDT(2)	\overline{RD} (PA4), PB0 to PB7		2.5 to 5.5			1/3tCYC -15ns	
Input data set-up time	tsDTR(1)	\overline{RD} (PA4), PB0 to PB7	From input data set-up to \overline{RD} leading edge. (Note 2)	2.5 to 5.5	40			ns
Input data hold time	thDTR(1)	\overline{RD} (PA4), PB0 to PB7	From \overline{RD} leading edge until input data hold	2.5 to 5.5	0			
Output data set-up time	tsDTW(1)	\overline{RD} (PA4), PB0 to PB7	From output data set-up until \overline{WR} leading edge	2.5 to 5.5			1/3tCYC -30ns	tCYC & ns
	tsDTW(2)	\overline{RD} (PA4), PB0 to PB7		2.5 to 5.5			1/3tCYC -30ns	
Output data hold time	thDTW(1)	\overline{RD} (PA4), PB0 to PB7	From \overline{WR} leading edge until output data hold	2.5 to 5.5	0			ns
	thDTW(2)	\overline{RD} (PA4), PB0 to PB7		2.5 to 5.5	0			

Note 1 : Time until incorrect data of Low disappears.

Note 2 : Incorrect data of Low is not output in the period between tRDL(1) to tdDT(1).

Pulse Input Conditions / Ta = -20°C to +70°C, VSS1 = VSS2 = VSS3 = 0V

Parameter	Symbol	Pins	Conditions	Limits				
				V _{DD} [V]	min	typ	max	unit
High/low level pulse width	tPIH(1) tPIL(1)	INT0 (P70), INT1 (P71), INT2 (P72) INT4 (P20 to P23) INT5 (P24 to P27)	• Interrupt acceptable • Timer 0 and 1 event input acceptable	2.5 to 5.5	1			tCYC
	tPIH(2) tPIL(2)	INT3 (P73) (The noise rejection clock is selected to 1/1.)	• Interrupt acceptable • Timer 0 event input acceptable	2.5 to 5.5	2			
	tPIH(3) tPIL(3)	INT3 (P73) (The noise rejection clock is selected to 1/32.)	• Interrupt acceptable • Timer 0 event input acceptable	2.5 to 5.5	64			
	tPIH(4) tPIL(4)	INT3 (P73) (The noise rejection clock is selected to 1/128.)	• Interrupt acceptable • Timer 0 event input acceptable	2.5 to 5.5	256			
	tPIL(5)	RES	Reset acceptable	2.5 to 5.5	200			μs

AD Converter Characteristics / Ta = -20°C to +70°C, VSS1 = VSS2 = VSS3 = 0V

Parameter	Symbol	Pins	Conditions	Limits					
				V _{DD} [V]	min	typ	max	unit	
Resolution	N	AN0 (P80)		3.0 to 5.5		8		bit	
Absolute precision	ET	to AN7 (P87)	(Note 2)	3.0 to 5.5			±1.5	LSB	
Conversion time	TCAD	AN8 (P70) AN9 (P71) AN10 (XT1) AN11 (XT2)	AD conversion time = 32 × tCYC (ADCR2 = 0) (Note 3)	3.0 to 5.5			15.10 (tCYC = 0.588μs)	97.92 (tCYC = 3.06μs)	μs
			AD conversion time = 64 × tCYC (ADCR2 = 1) (Note 3)	3.0 to 5.5			15.10 (tCYC = 0.294μs)	97.92 (tCYC = 1.53μs)	
Analog input voltage range	VAIN			3.0 to 5.5	V _{SS}		V _{DD}	V	
Analog port input current	I _{AINH}		VAIN = V _{DD}	3.0 to 5.5			1	μA	
	I _{AINL}		VAIN = V _{SS}	3.0 to 5.5			-1		

Note 2 : Absolute precision excludes the quantizing error (±1/2 LSB).

Note 3 : The conversion time is the time from executing the AD conversion instruction to setting the complete digital conversion value in the register.

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Current Dissipation Characteristics / $T_a = -20^{\circ}\text{C}$ to $+70^{\circ}\text{C}$, $V_{SS1} = V_{SS2} = V_{SS3} = 0\text{V}$

Parameter	Symbol	Pins	Conditions	V_{DD} [V]	Limits			unit
					min	typ	max	
Current drain during basic operation (Note 4)	IDDOP(1)	$V_{DD1} = V_{DD2} = V_{DD3}$	<ul style="list-style-type: none"> FmCF = 10MHz by ceramic resonator FmX'tal = 32.768kHz by crystal oscillation System clock : CF oscillation (10MHz) Internal RC oscillation stops 1/1 divided 	4.5 to 5.5		18	35	mA
	IDDOP(2)		<ul style="list-style-type: none"> CF1 = 20MHz by external clock FmX'tal = 32.768kHz by crystal oscillation System clock : CF1 oscillation (20MHz) Internal RC oscillation stops 1/2 divided 	2.5 to 5.5		18	35	
	IDDOP(3)		<ul style="list-style-type: none"> FmCF = 5MHz by ceramic resonator FmX'tal = 32.768kHz by crystal oscillation System clock : CF oscillation (5MHz) Internal RC oscillation stops 	4.5 to 5.5		9	15	
	IDDOP(4)		<ul style="list-style-type: none"> FmCF = 5MHz by ceramic resonator FmX'tal = 32.768kHz by crystal oscillation System clock : CF oscillation (5MHz) Internal RC oscillation stops 	2.5 to 4.5		6	11	
	IDDOP(5)		<ul style="list-style-type: none"> FmCF = 0Hz (when oscillation stops) FmX'tal = 32.768kHz by crystal oscillation System clock : RC oscillation 	4.5 to 5.5		4	8	
	IDDOP(6)		<ul style="list-style-type: none"> FmCF = 0Hz (when oscillation stops) FmX'tal = 32.768kHz by crystal oscillation System clock : RC oscillation 	2.5 to 4.5		2	5	
	IDDOP(7)		<ul style="list-style-type: none"> FmCF = 0Hz (when oscillation stops) FmX'tal = 32.768kHz by crystal oscillation System clock : X'tal oscillation (32.768kHz) Internal RC oscillation stops 	4.5 to 6.0		80	200	μA
	IDDOP(8)		<ul style="list-style-type: none"> FmCF = 0Hz (when oscillation stops) FmX'tal = 32.768kHz by crystal oscillation System clock : X'tal oscillation (32.768kHz) Internal RC oscillation stops 	2.5 to 4.5		40	150	
Current drain in HALT mode (Note 4)	IDDHALT(1)	$V_{DD1} = V_{DD2} = V_{DD3}$	<ul style="list-style-type: none"> HALT mode FmCF = 10MHz by ceramic resonator FmX'tal = 32.768kHz by crystal oscillation System clock : CF oscillation (10MHz) Internal RC oscillation stops 1/1 divided 	4.5 to 5.5		6	12	mA
	IDDHALT(2)		<ul style="list-style-type: none"> HALT mode CF1 = 20MHz by external clock FmX'tal = 32.768kHz by crystal oscillation System clock : CF1 oscillation (20MHz) Internal RC oscillation stops 1/2 divided 	4.5 to 5.5		7	14	
	IDDHALT(3)		<ul style="list-style-type: none"> HALT mode FmCF = 5MHz by ceramic resonator FmX'tal = 32.768kHz by crystal oscillation System clock : CF oscillation (5MHz) Internal RC oscillation stops 	4.5 to 5.5		3.3	5	
	IDDHALT(4)		<ul style="list-style-type: none"> HALT mode FmCF = 5MHz by ceramic resonator FmX'tal = 32.768kHz by crystal oscillation System clock : CF oscillation (5MHz) Internal RC oscillation stops 	2.5 to 4.5		1.5	3.2	
	IDDHALT(5)		<ul style="list-style-type: none"> HALT mode FmCF = 0Hz (when oscillation stops) FmX'tal = 32.768kHz by crystal oscillation System clock : RC oscillation 	4.5 to 5.5		1	1.5	
	IDDHALT(6)		<ul style="list-style-type: none"> HALT mode FmCF = 0Hz (when oscillation stops) FmX'tal = 32.768kHz by crystal oscillation System clock : RC oscillation 	2.5 to 4.5		0.4	1	
	IDDHALT(7)		<ul style="list-style-type: none"> HALT mode FmCF = 0Hz (when oscillation stops) FmX'tal = 32.768kHz by crystal oscillation System clock : X'tal oscillation (32.768kHz) Internal RC oscillation stops 	4.5 to 5.5		60	150	
	IDDHALT(8)		<ul style="list-style-type: none"> HALT mode FmCF = 0Hz (when oscillation stops) FmX'tal = 32.768kHz by crystal oscillation System clock : X'tal oscillation (32.768kHz) Internal RC oscillation stops 	2.5 to 4.5		20	72	
Current drain during HOLD mode	IDDHOLD(1)	V_{DD1}	<ul style="list-style-type: none"> HOLD mode CF1 = V_{DD} or leave it open (when using external clock) 	4.5 to 5.5		0.05	25	μA
			<ul style="list-style-type: none"> HOLD mode CF1 = V_{DD} or leave it open (when using external clock) 	2.5 to 4.5		0.01	15	
Current drain during time-base clock HOLD mode	IDDHOLD(2)	V_{DD1}	<ul style="list-style-type: none"> Time-base clock HOLD mode CF1 = V_{DD} or leave it open (when using external clock) 	4.5 to 5.5		35	100	μA
			<ul style="list-style-type: none"> Time-base clock HOLD mode CF1 = V_{DD} or leave it open (when using external clock) 	2.5 to 4.5		15	45	

Note 4 : The current of the output transistors and pull-up MOS transistors are excluded.

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F-ROM Write Characteristics / $T_a = +10^{\circ}\text{C}$ to $+55^{\circ}\text{C}$, $V_{SS1} = V_{SS2} = V_{SS3} = 0\text{V}$

Parameter	Symbol	Pins	Conditions	Limits				
				V_{DD} [V]	min	typ	max	unit
On-board writing current	IDDFW(1)	VDD1	<ul style="list-style-type: none"> 128-byte writing Including erase time current 	4.5 to 5.5		30	65	mA
Writing time	tFW(1)		<ul style="list-style-type: none"> 128-byte writing Including data erase time Excluding time to fetch 128 byte data 	4.5 to 5.5		5.0	10.0	mS

Main System Clock Oscillation Circuit Characteristics

The characteristics in the table below is based on the following conditions :

1. Using the standard oscillation evaluation board SANYO has provided.
2. Using the external peripheral parts with the indicated value.
3. The recommended circuit parameters for the peripheral parts are verified by the oscillator manufacturer.

Table 1. Recommended circuit parameters for the main system clock using the ceramic resonator

Frequency	Manufacturer	Oscillator	Recommended circuit parameters			Operating supply voltage range	Oscillation stabilizing time		Note
			C1	C2	Rd1		typ	max	
10MHz	MURATA	CSLS100G53	(15pF)	(15pF)	100Ω	3.0 to 6.0V	0.04ms	0.40ms	Internal C1, C2
	KYOCERA	KBR-10.0M	(24pF)	(24pF)	0Ω	3.5 to 6.0V	0.02ms	0.20ms	
4MHz	MURATA	CSTLS4M00G53B	(30pF)	(30pF)	220Ω	2.5 to 6.0V	0.04ms	0.40ms	Internal C1, C2
	KYOCERA	PBRC4.00HR	(33pF)	(33pF)	1.0kΩ	3.5 to 6.0V	0.02ms	0.20ms	

*The oscillation stabilizing time is a period until the oscillation becomes stable after V_{DD} becomes higher than minimum operating voltage. (Refer to Figure4)

Subsystem Clock Oscillation Circuit Characteristics

The characteristics in the table below is based on the following conditions :

1. Using the standard oscillation evaluation board SANYO has provided.
2. Using the external peripheral parts with the indicated value.
3. The recommended circuit parameters for the peripheral parts are verified by the oscillator manufacturer.

Table 2. Recommended circuit parameters for the subsystem clock using the crystal oscillation

Frequency	Manufacturer	Oscillator	Recommended circuit parameters				Operating supply voltage range	Oscillation stabilizing time		Note
			C3	C4	Rf	Rd2		typ	max	
32.768kHz	SEIKO EPSON	C-002Rx	15pF	15pF	OPEN	300kΩ	2.5 to 6.0V	0.8s	3s	

*The oscillation stabilizing time is the period until the oscillation becomes stable, after executing the instruction which starts the sub-clock oscillator or after releasing a HOLD mode. (Refer to Figure4)

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(Notes) Since the oscillation frequency precision is affected by the circuit pattern, place the oscillation related parts as close to the oscillation pins as possible, using the shortest possible pattern length.

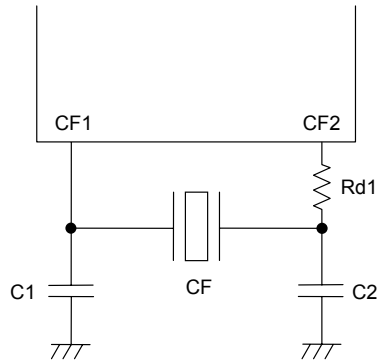


Figure 1 Ceramic oscillation circuit

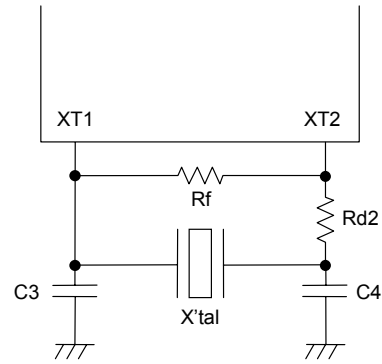


Figure 2 Crystal oscillation circuit

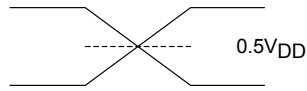
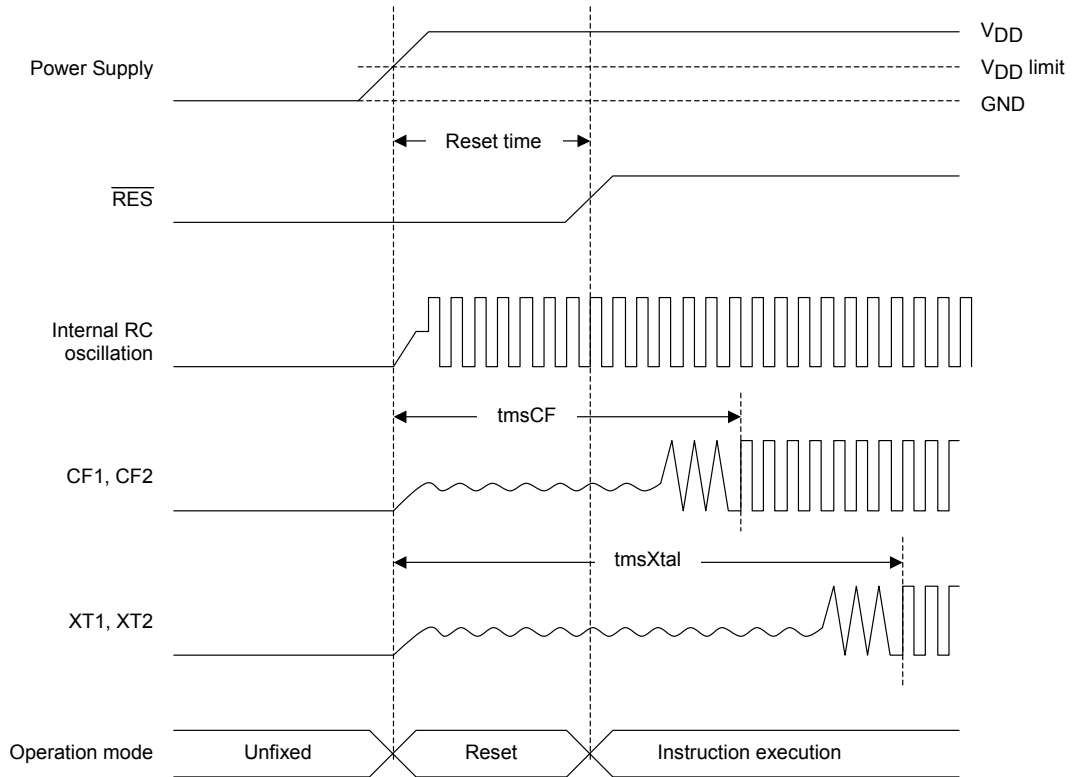
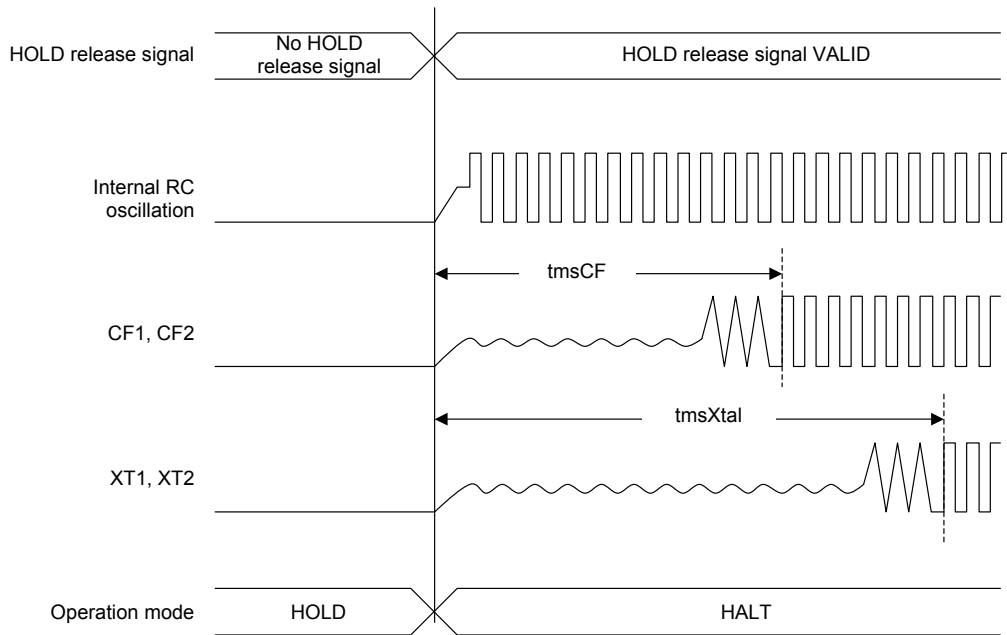


Figure 3 AC timing point

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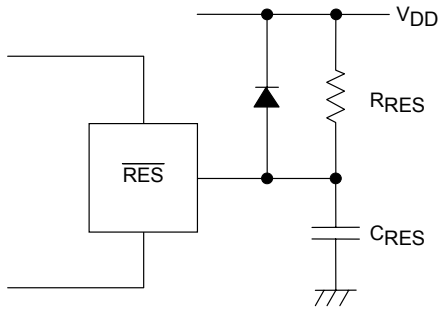


Reset time and oscillation stabilizing time



HOLD release signal and oscillation stabilizing time

Figure 4 Oscillation stabilizing time



(Note)
 Select C_{RES} and R_{RES} value to assure that at least $200\mu s$ reset time is generated after the V_{DD} becomes higher than the minimum operating voltage.

Figure 5 Reset circuit

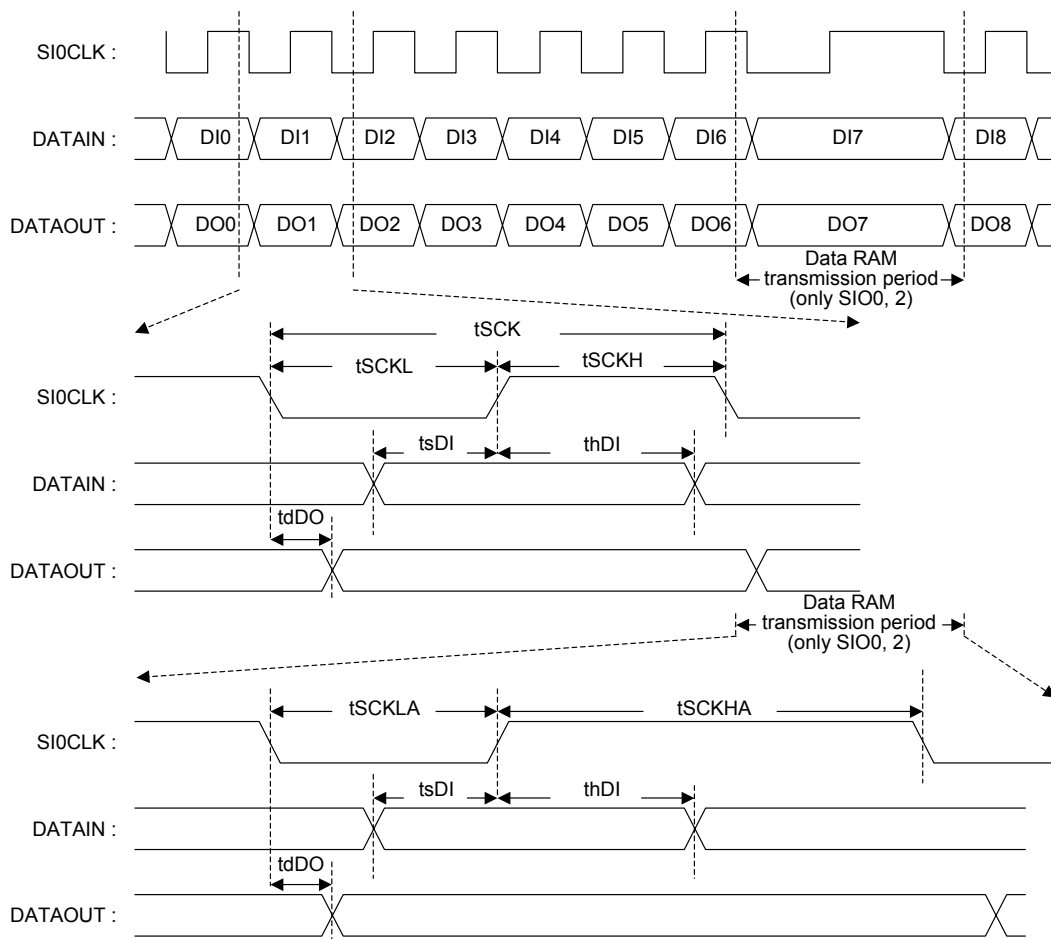


Figure 6 Serial input/output test condition

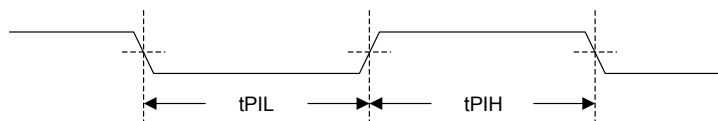
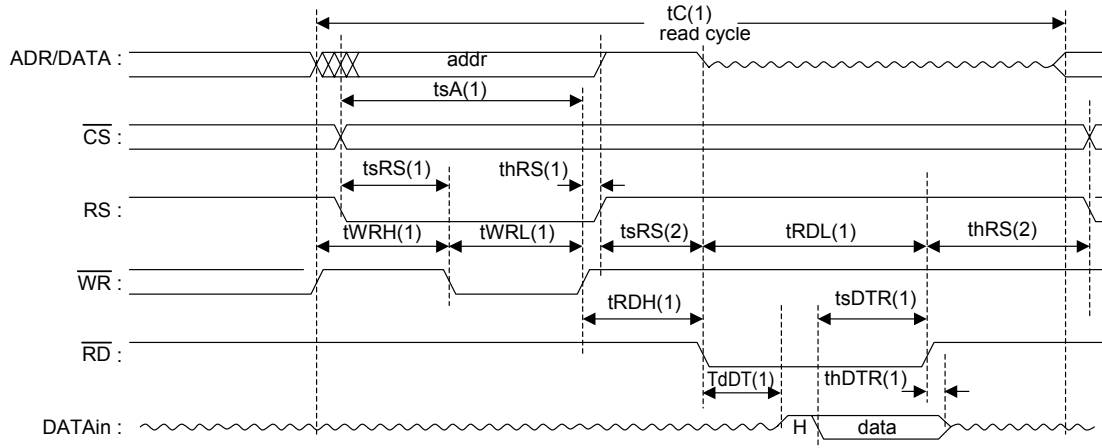


Figure 7 Pulse input timing condition

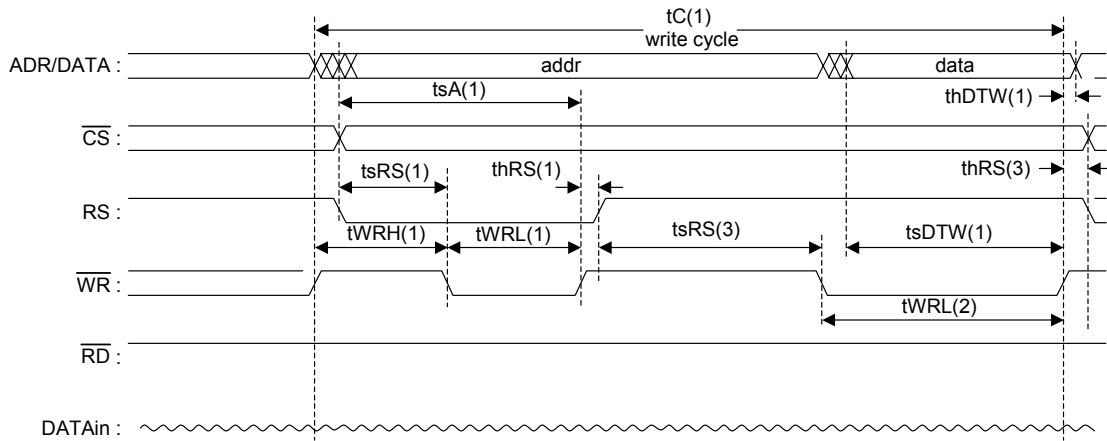
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• Parallel input/output timing waveform : Indirect Setting, Read Mode



Note : If port A terminals will be used as RS, $\overline{\text{WR}}$, $\overline{\text{RD}}$ or $\overline{\text{CS}}$, then it should be set to CMOS format by option data.

• Parallel input/output timing waveform : Indirect Setting, Write Mode

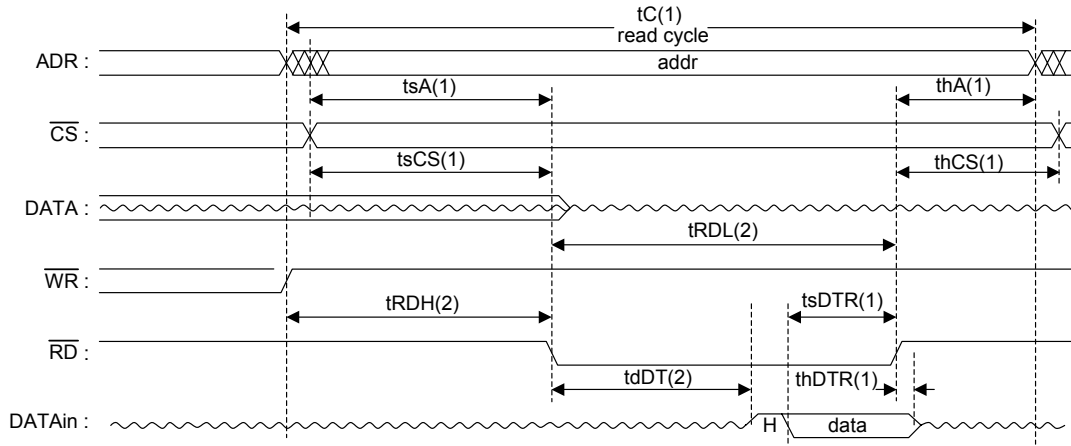


Note : If port A terminals will be used as RS, $\overline{\text{WR}}$, $\overline{\text{RD}}$ or $\overline{\text{CS}}$, then it should be set to CMOS format by option data.

Figure 8 Indirect mode : Parallel Timing Diagram

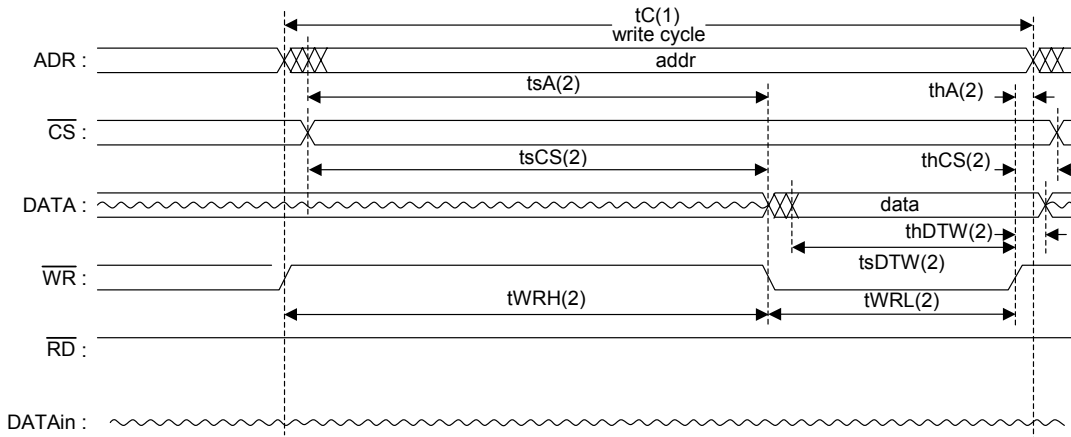
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- Parallel input/output timing waveform : Direct Setting, Read Mode



Note : If port A terminals will be used as RS, \overline{WR} , \overline{RD} or \overline{CS} , then it should be set to CMOS format by option data.

- Parallel input/output timing waveform : Direct Setting, Write Mode



Note : If port A terminals will be used as RS, \overline{WR} , \overline{RD} or \overline{CS} , then it should be set to CMOS format by option data.

Figure 9 Direct Mode : Parallel input/output Timing Diagrams

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