

Standard Variable Output LDO Regulators

300mA Standard Variable Output LDO Regulator


BA3662CP-V5

No.10023EAT05

●Description

The BA3662CP-V5 is low-saturation regulator. The output voltage can be arbitrarily configured using the external resistance. This IC has a built-in over-current protection circuit that prevents the destruction of the IC due to output short circuits and a thermal shutdown circuit that protects the IC from thermal damage due to overloading.

●Features

- 1) Output Current: 300mA
- 2) High Output Voltage Precision : $\pm 2\%$
- 3) Low saturation with PNP output
- 4) Built-in over-current protection circuit that prevents the destruction of the IC due to output short circuits
- 5) Built-in thermal shutdown circuit for protecting the IC from thermal damage due to overloading
- 6) Built-in over-voltage protection circuit that prevents the destruction of the IC due to power supply surges
- 7) TO220CP-V5 packaging

●Applications

Audiovisual equipments, FPDs, televisions, personal computers or any other consumer device

●Absolute Maximum Ratings (Ta=25°C)

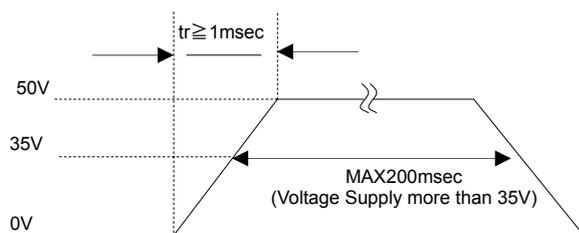
Parameter	Symbol	Ratings	Unit
Supply Voltage ※1	Vcc	-0.3~+35.0	V
Output Control Voltage	V _{CTL}	-0.3~+Vcc	V
Power Dissipation ※2	Pd	2000	mW
Operating Temperature Range	Topr	-40~+125	°C
Storage Temperature Range	Tstg	-55~+150	°C
Maximum Junction Temperature	Tjmax	+150	°C
Peak Supply Voltage ※3	V _{cc peak}	+50	V

※ 1 Not to exceed Pd.

※ 2 TO220CP-V5:Derating in done at 16mW/°C for operating above Ta \geq 25°C.(without heat sink)

※ 3 Applied voltage : 200msec or less (tr \geq 1msec)

NOTE : This product is not designed for protection against radioactive rays.



●Operating conditions (Ta=-40~+125°C)

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage	Vcc	4.0	25.0	V
Output Control Voltage	V _{CTL}	0	Vcc	V
Output Current	I _o	0	0.3	A
Output Voltage	V _o	3.0	15.0	V

●Protect features

Parameter	Symbol	Min.	Typ.	Max.	Unit
Over Voltage protection	Vcc	26	28	30	V

●Electrical characteristics

(Unless otherwise specified, Ta=25°C, Vcc=10V, VCTL=5V, I_o=200mA, R1=2.2kΩ, R2=6.8kΩ)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Shut Down Current	I _{sd}	—	0	10	μA	VCTL=0V
Bias Current	I _b	—	2.5	5.0	mA	VCTL=2V, I _o =0mA
C Terminal Voltage	V _c	1.200	1.225	1.250	V	I _o =50mA
Dropout Voltage	ΔV _d	—	0.3	0.5	V	Vcc=V _o × 0.95
Ripple Rejection	R.R.	45	55	—	dB	f=120Hz, e _{in} *1=1Vrms, I _o =100mA
Line Regulation	Reg.I	—	20	100	mV	Vcc=6→25V
Load Regulation	Reg.L	—	40	80	mV	I _o =5mA→200mA
Temperature Coefficient of Output Voltage	T _{cvo}	—	±0.02	—	%/°C	I _o =5mA, T _j =0~125°C
Short Current	I _{os}	—	0.1	—	A	Vcc=25V, V _o =0V
ON Mode Voltage	V _{thH}	2.0	—	—	V	ACTIVE MODE, I _o =0mA
OFF Mode Voltage	V _{thL}	—	—	0.8	V	OFF MODE, I _o =0mA
Input High Current	I _{CTL}	100	200	300	μA	VCTL=5V, I _o =0mA

* 1 e_{in} : Input Voltage Ripple

●Reference data

BA3662CP-V5(5.0V preset voltage)

(Unless otherwise specified, $T_a=25^\circ\text{C}$, $V_{CC}=10\text{V}$, $V_{CTL}=5\text{V}$, $I_o=200\text{mA}$, $R_1=2.2\text{k}\Omega$, $R_2=6.8\text{k}\Omega$)

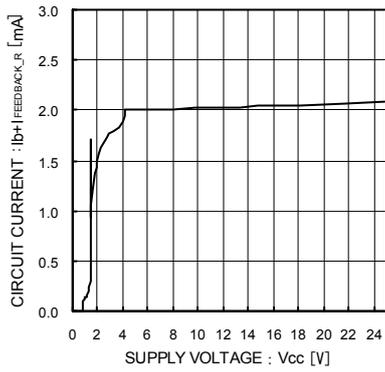


Fig.1 Circuit Current

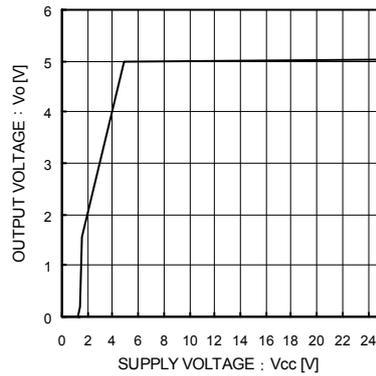


Fig.2 Line Regulation

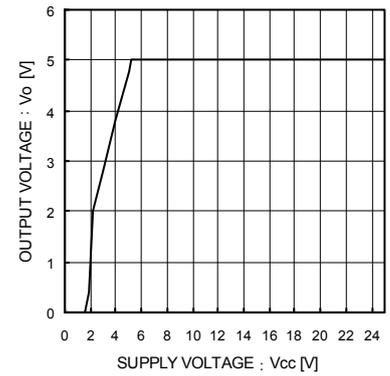


Fig.3 Line Regulation
($I_o=200\text{mA}$)

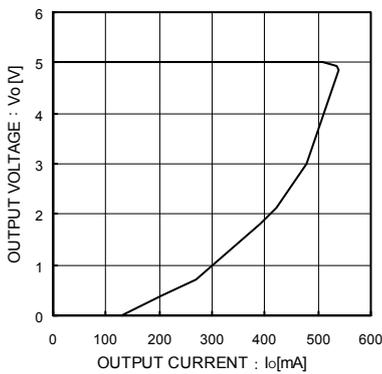


Fig.4 Load Regulation

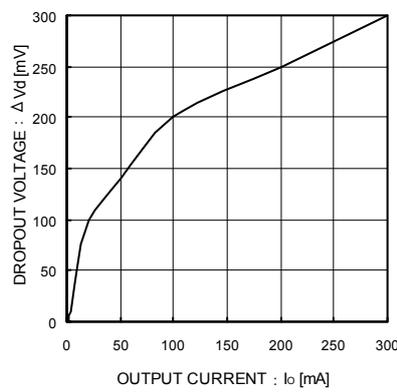


Fig.5 Dropout Voltage $I_o-\Delta V_d$ Characteristics
($V_{CC}=4.75\text{V}$)

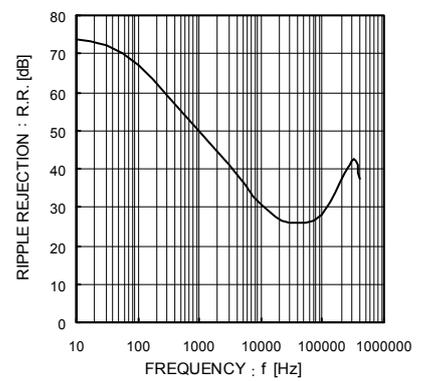


Fig.6 Ripple Rejection
($I_o=100\text{mA}$)

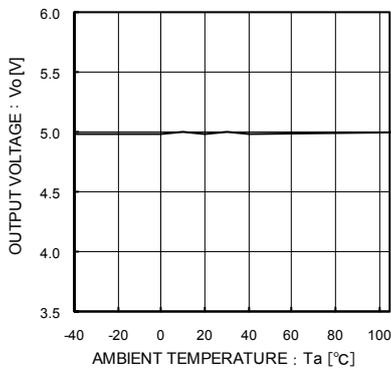


Fig.7 Output Voltage

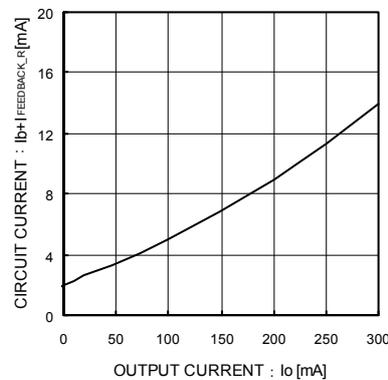


Fig.8 Circuit Current ($I_o=0\text{mA}\rightarrow 300\text{mA}$)
($I_{FEEDBACK_R}=555\mu\text{A}$)

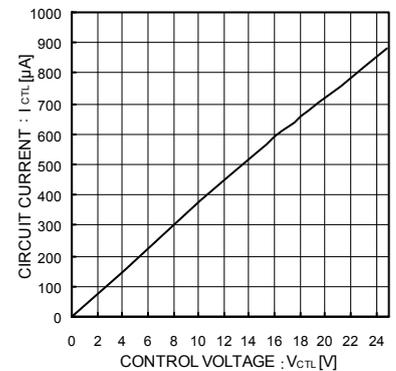


Fig.9 CTL Voltage vs CTL Current

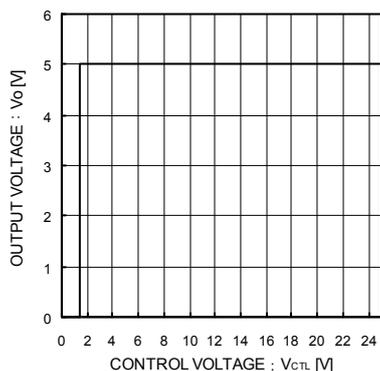


Fig.10 CTL Voltage vs Output Voltage

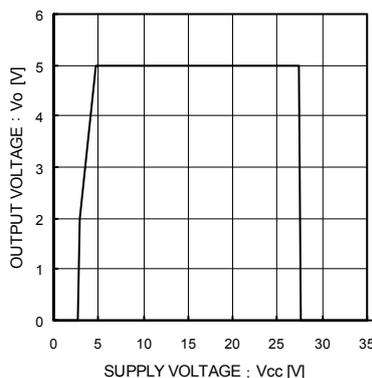


Fig.11 Overvoltage Operating
($I_o = 200\text{mA}$)

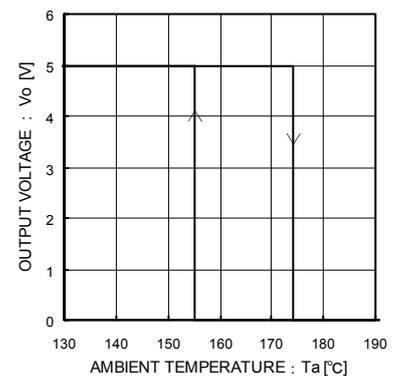
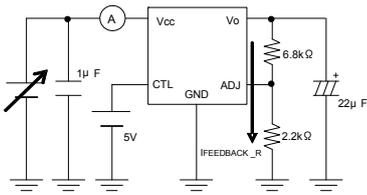
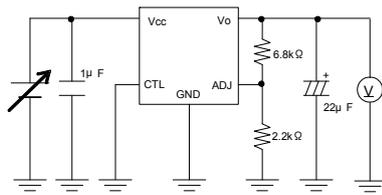


Fig.12 Thermal Shutdown
Circuit Characteristics

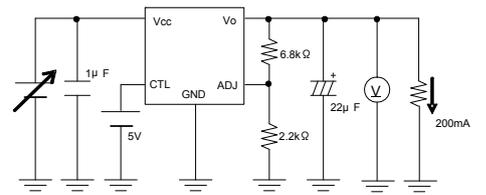
● Measurement Circuit for Reference Data



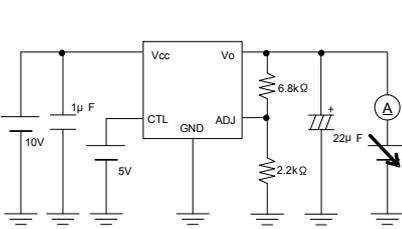
Measurement Circuit of Fig.1



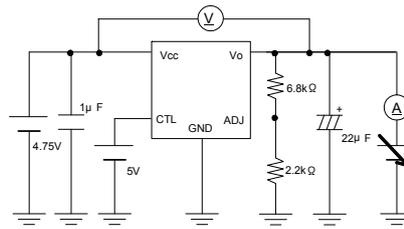
Measurement Circuit of Fig.2



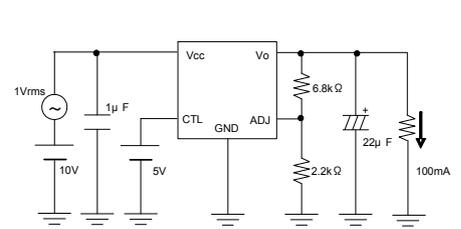
Measurement Circuit of Fig.3



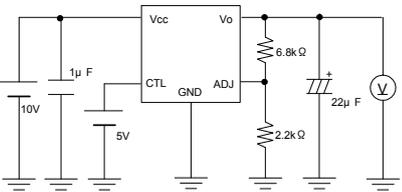
Measurement Circuit of Fig.4



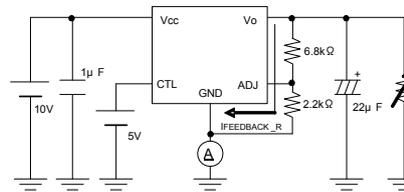
Measurement Circuit of Fig.5



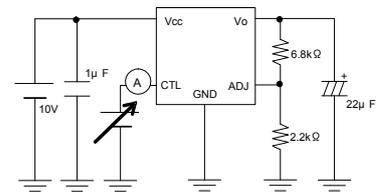
Measurement Circuit of Fig.6



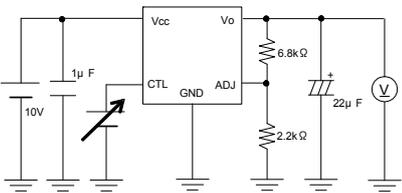
Measurement Circuit of Fig.7



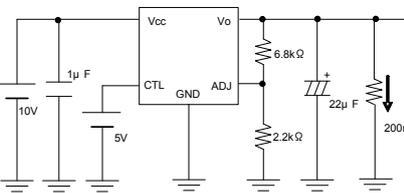
Measurement Circuit of Fig.8



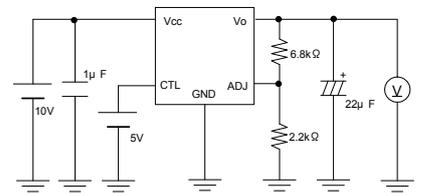
Measurement Circuit of Fig.9



Measurement Circuit of Fig.10



Measurement Circuit of Fig.11



Measurement Circuit of Fig.12

●Block Diagrams

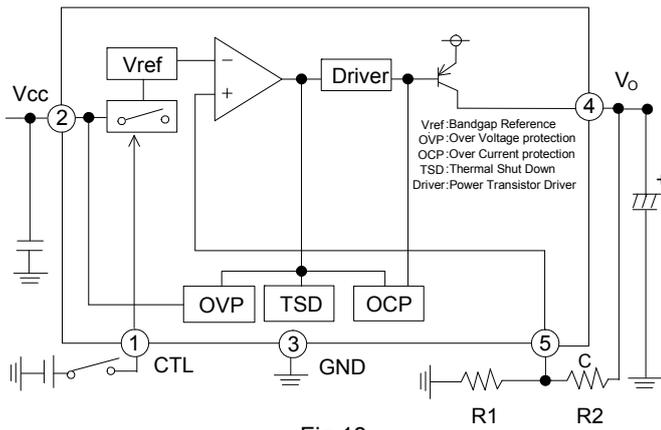
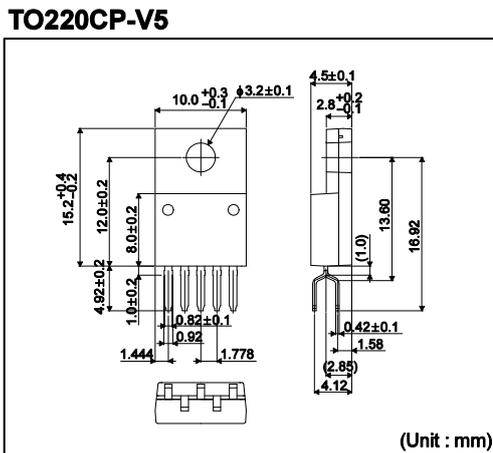


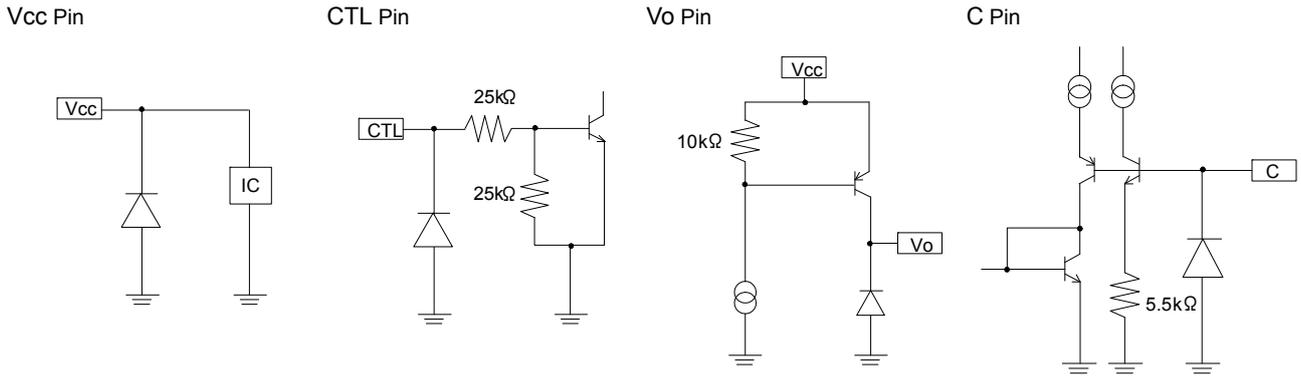
Fig.13

Pin No.	Pin Name	Function
1	CTL	Output Control Pin
2	Vcc	Power Supply Pin
3	GND	GND
4	Vo	Output Pin
5	C	Adjustable Pin

●Top View <Package dimension>



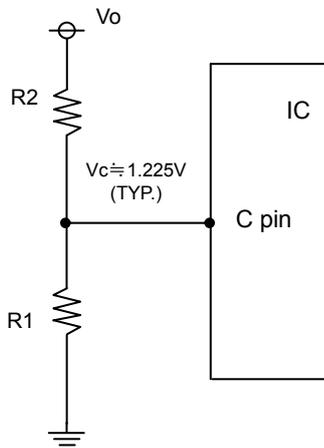
●Input / Output equivalent circuit diagrams



●Output voltage configuration method

Please connect resistors R1 and R2 (which determines the output voltage) as shown in Fig.14.

Please be aware that the offset due to the current that flows from the C terminal becomes large when resistors with large values are used. The use of resistors with R1=2kΩ to 15kΩ is recommended.



$$V_o \doteq V_c \times (R_1 + R_2) / R_1$$

Fig.14

●Thermal design

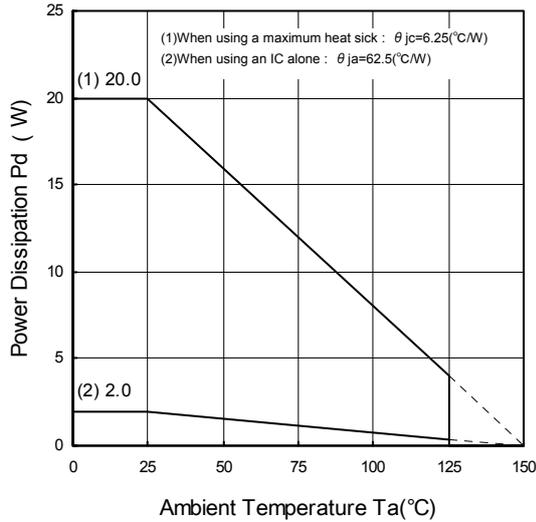


Fig.15

When using at temperatures over Ta=25°C, please refer to the heat reducing characteristics shown in Fig.15. The IC characteristics are closely related to the temperature at which the IC is used, so it is necessary to operate the IC at temperatures less than the maximum junction temperature Tjmax.

Fig.15 shows the acceptable loss and heat reducing characteristics of the TO220CP-V5 package. Even when the ambient temperature Ta is a normal temperature (25°C), the chip (junction) temperature Tj may be quite high so please operate the IC at temperatures less than the acceptable loss Pd.

The calculation method for power consumption Pc(W) is as follows.

$$Pc=(V_{cc}-V_o) \times I_o+V_{cc} \times I_b$$

$$\text{Acceptable loss } Pd \geq Pc$$

Solving this for load current Io in order to operate within the acceptable loss,

$$I_o \leq \frac{Pd - V_{cc} \times I_b}{V_{cc} - V_o}$$

- Vcc: Input voltage
- Vo: Output voltage
- Io: Load current
- Ib: Circuit current
- Ishort: Short current

(Please refer to Figs.8 for Ib.)

It is then possible to find the maximum load current IoMax with respect to the applied voltage Vcc at the time of thermal design.

Calculation Example)

When Ta=85°C, Vcc=10V, Vo=5V

$$I_o \leq \frac{1.04 - 10 \times I_b}{5}$$

$$I_o \leq 192\text{mA} \quad (I_b: 8\text{mA})$$

$$\left[\begin{array}{l} \text{With the IC alone : } \theta_{ja}=62.5^{\circ}\text{C}/\text{W} \rightarrow -16\text{mW}/^{\circ}\text{C} \\ 25^{\circ}\text{C}=2.0\text{W} \rightarrow 85^{\circ}\text{C}=1.04\text{W} \end{array} \right]$$

Please refer to the above information and keep thermal designs within the scope of acceptable loss for all operating temperature ranges. The power consumption Pc of the IC when there is a short circuit (short between Vo and GND) is :

$$Pc=V_{cc} \times (I_b+I_{short}) \quad (\text{Please refer to Fig.4 for } I_{short}.)$$

●Notes for use

1. Absolute maximum ratings
Use of the IC in excess of absolute maximum ratings (such as the input voltage or operating temperature range) may result in damage to the IC. Assumptions should not be made regarding the state of the IC (e.g., short mode or open mode) when such damage is suffered. If operational values are expected to exceed the maximum ratings for the device, consider adding protective circuitry (such as fuses) to eliminate the risk of damaging the IC.
2. Electrical characteristics described in these specifications may vary, depending on temperature, supply voltage, external circuits and other conditions. Therefore, be sure to check all relevant factors, including transient characteristics.
3. GND potential
The potential of the GND pin must be the minimum potential in the system in all operating conditions. Ensure that no pins are at a voltage below the GND at any time, regardless of transient characteristics.
4. Ground wiring pattern
When using both small-signal and large-current GND traces, the two ground traces should be routed separately but connected to a single ground potential within the application in order to avoid variations in the small-signal ground caused by large currents. Also ensure that the GND traces of external components do not cause variations on GND voltage. The power supply and ground lines must be as short and thick as possible to reduce line impedance.
5. Inter-pin shorts and mounting errors
Use caution when orienting and positioning the IC for mounting on printed circuit boards. Improper mounting may result in damage to the IC. Shorts between output pins or between output pins and the power supply or GND pins (caused by poor soldering or foreign objects) may result in damage to the IC.
6. Operation in strong electromagnetic fields
Using this product in strong electromagnetic fields may cause IC malfunction. Caution should be exercised in applications where strong electromagnetic fields may be present.
7. Testing on application boards
When testing the IC on an application board, connecting a capacitor directly to a low-impedance pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from a jig or fixture during the evaluation process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.
8. Thermal consideration
Use a thermal design that allows for a sufficient margin in light of the Pd in actual operating conditions. Consider Pc that does not exceed Pd in actual operating conditions. ($P_d \geq P_c$)

T_{jmax} : Maximum junction temperature=150[°C], θ_{ja} : Thermal resistance of package-ambience[°C/W], P_c : Power dissipation [W], V_o : Output Voltage,	T_a : Peripheral temperature[°C] , P_d : Package Power dissipation [W], V_{cc} : Input Voltage, I_o : Load,	I_b : Bias Current
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Package Power dissipation	: $P_d (W) = (T_{jmax} - T_a) / \theta_{ja}$
Power dissipation	: $P_c (W) = (V_{cc} - V_o) \times I_o + V_{cc} \times I_b$
9. Vcc pin
Insert a capacitor(capacitor $\geq 0.33\mu F$ ~) between the Vcc and GND pins. The appropriate capacitance value varies by application. Be sure to allow a sufficient margin for input voltage levels.

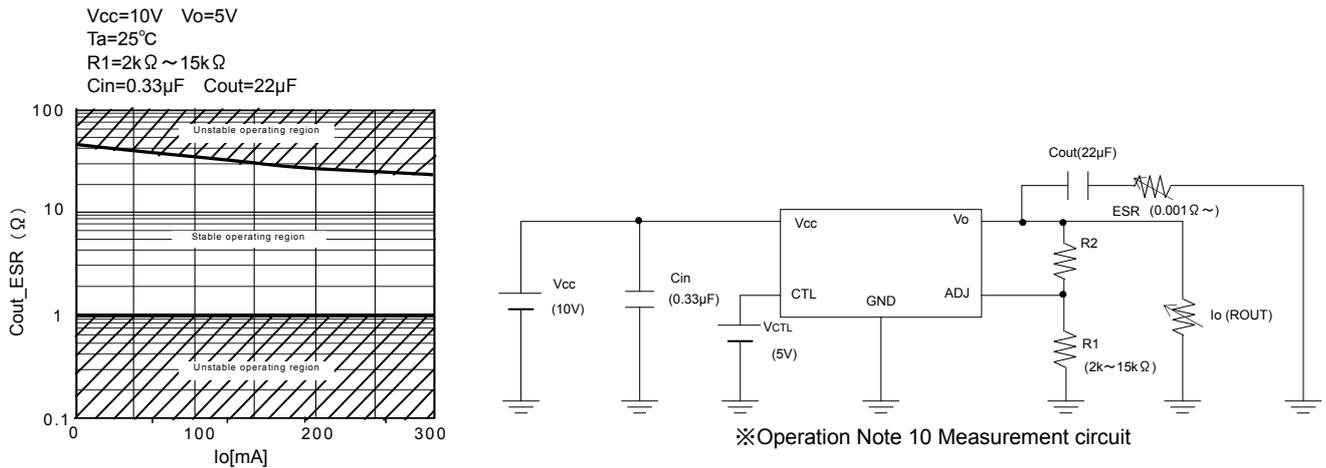
10. Vo Terminal

Please attach an anti-oscillation capacitor between Vo and GND. The capacitance of the capacitor may significantly change due to factors such as temperature changes, which may cause oscillations. Please use a tantalum capacitor or aluminum electrolytic capacitor with favorable characteristics and small external series resistance (ESR) even at low temperatures. The output oscillates regardless of whether the ESR is large or small. Please use the IC within the stable operating region while referring to the ESR characteristics reference data shown in Fig.16. In cases where there are sudden load fluctuations, the large capacitor is recommended. Below figure, it is ESR-to-Io stability Area characteristics, measured by 22 μ F-ceramic-capacitor and resistor connected in series.

This characteristic is not equal value perfectly to 22 μ F-aluminum electrolytic capacitor in order to measurement method.

Note, however, that the stable range suggested in the figure depends on the IC and the resistance load involved, and can vary with the board's wiring impedance, input impedance, and/or load impedance. Therefore, be certain to ascertain the final status of these items for actual use.

Keep capacitor capacitance within a range of 22 μ F~1000 μ F. It is also recommended that a 0.33 μ F bypass capacitor be connected as close to the input pin-GND as location possible. However, in situations such as rapid fluctuation of the input voltage or the load, please check the operation in real application to determine proper capacitance.



11. Over current protection circuit (OCP)

The IC incorporates an integrated over-current protection circuit that operates in accordance with the rated output capacity. This circuit serves to protect the IC from damage when the load becomes shorted. It is also designed to limit output current (without latching) in the event of a large and instantaneous current flow from a large capacitor or other component. These protection circuits are effective in preventing damage due to sudden and unexpected accidents. However, the IC should not be used in applications characterized by the continuous or transitive operation of the protection circuits.

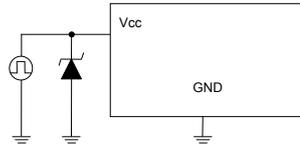
12. Thermal shutdown circuit (TSD)

The IC incorporates a built-in thermal shutdown circuit, which is designed to turn the IC off completely in the event of thermal overload. It is not designed to protect the IC from damage or guarantee its operation. ICs should not be used after this function has activated, or in applications where the operation of this circuit is assumed.

13. Applications or inspection processes where the potential of the Vcc pin or other pins may be reversed from their normal state may cause damage to the IC's internal circuitry or elements. Use an output pin capacitance of 1000 μ F or lower in case Vcc is shorted with the GND pin while the external capacitor is charged. Insert a diode in series with Vcc to prevent reverse current flow, or insert bypass diodes between Vcc and each pin.

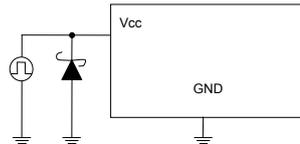
14. Positive voltage surges on VCC pin

A power zener diode should be inserted between VCC and GND for protection against voltage surges of more than 50V on the VCC pin.



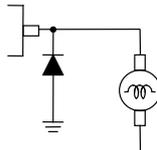
15. Negative voltage surges on VCC pin

A schottky barrier diode should be inserted between VCC and GND for protection against voltages lower than GND on the VCC pin.



16. Output protection diode

Loads with large inductance components may cause reverse current flow during startup or shutdown. In such cases, a protection diode should be inserted on the output to protect the IC.



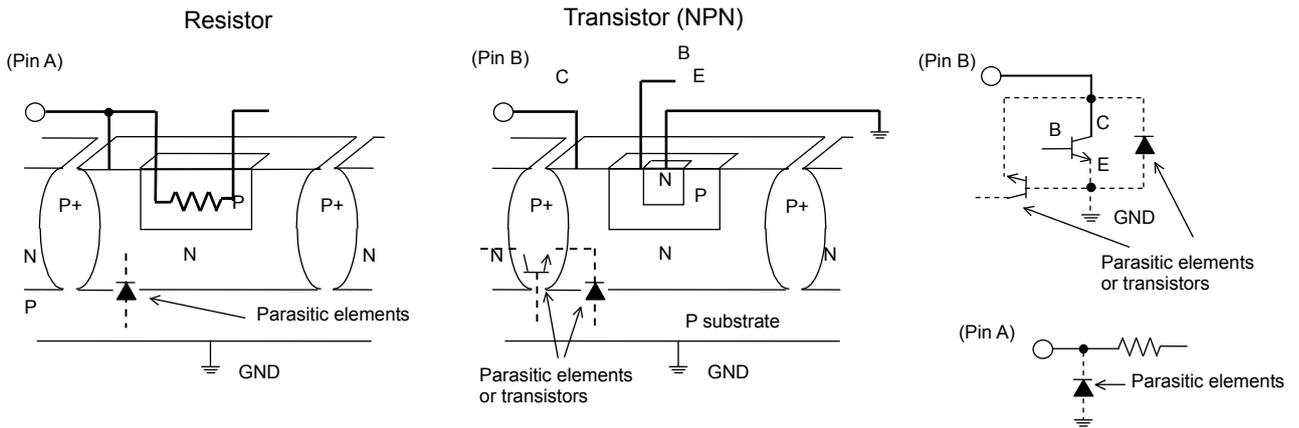
17. Regarding input pins of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. PN junctions are formed at the intersection of these P layers with the N layers of other elements, creating parasitic diodes and/or transistors. For example (refer to the figure below):

○When GND > Pin A and GND > Pin B, the PN junction operates as a parasitic diode

○When GND > Pin B, the PN junction operates as a parasitic transistor

Parasitic diodes occur inevitably in the structure of the IC, and the operation of these parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

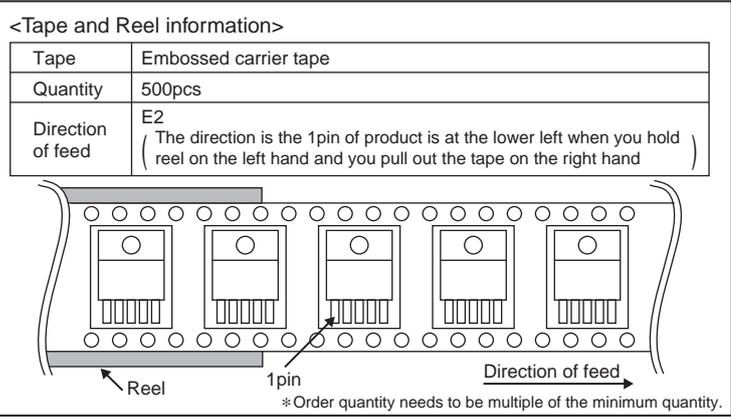
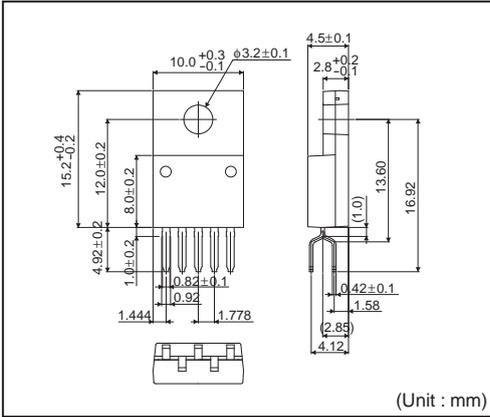


Example of Simple Monolithic IC Architecture

●Ordering part number

B	A	3	6	6	2	C	P	-	V	5	E	2
Part No.		Part No.				Package CP-V5: TO220CP-V5				Packaging and forming specification E2: Embossed tape and reel		

TO220CP-V5



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