

DATA SHEET

BLF278 VHF push-pull power MOS transistor

Product Specification
Supersedes data of October 1992

1996 Oct 21

VHF push-pull power MOS transistor

BLF278

FEATURES

- High power gain
- Easy power control
- Good thermal stability
- Gold metallization ensures excellent reliability.

APPLICATIONS

- Broadcast transmitters in the VHF frequency range.

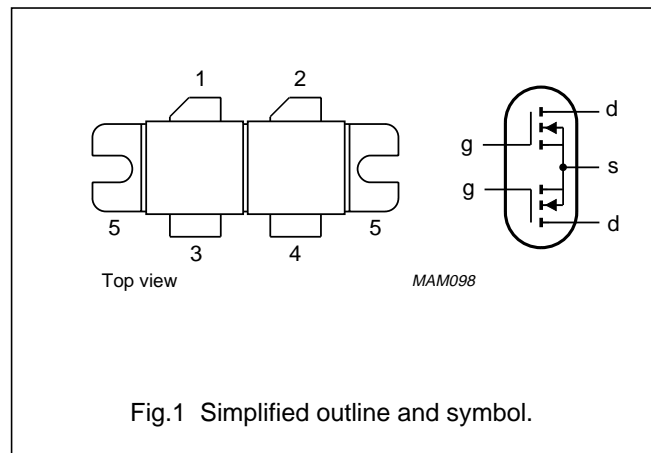
DESCRIPTION

Dual push-pull silicon N-channel enhancement mode vertical D-MOS transistor encapsulated in a 4-lead, SOT262A1 balanced flange package with two ceramic caps. The mounting flange provides the common source connection for the transistors.

PINNING - SOT262A1

PIN	SYMBOL	DESCRIPTION
1	d ₁	drain 1
2	d ₂	drain 2
3	g ₁	gate 1
4	g ₂	gate 2
5	s	source

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.



QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a push-pull common source test circuit.

MODE OF OPERATION	f (MHz)	V _{DS} (V)	P _L (W)	G _p (dB)	η _D (%)
CW, class-B	108	50	300	>20	>60
CW, class-C	108	50	300	typ. 18	typ. 80
CW, class-AB	225	50	250	>14 typ. 16	>50 typ. 55

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO discs are not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

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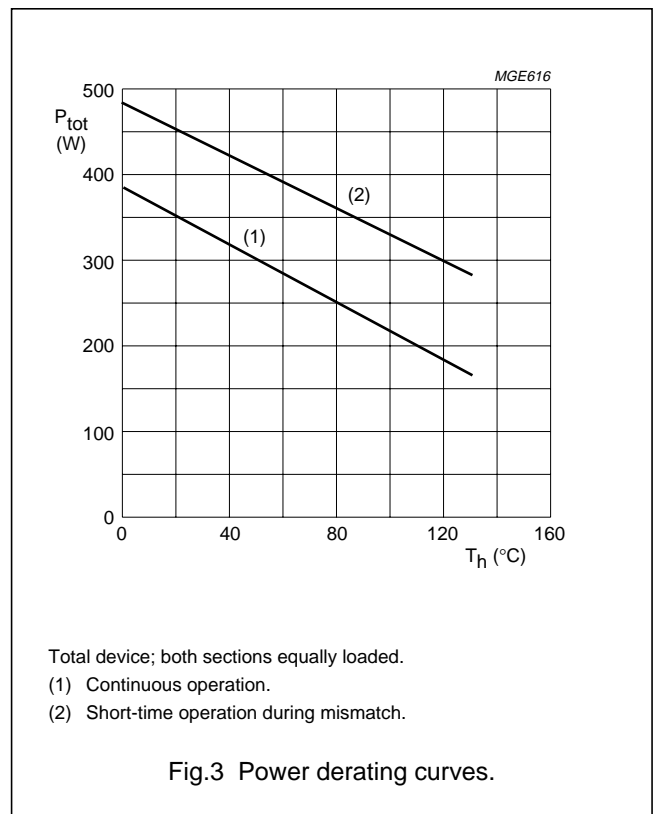
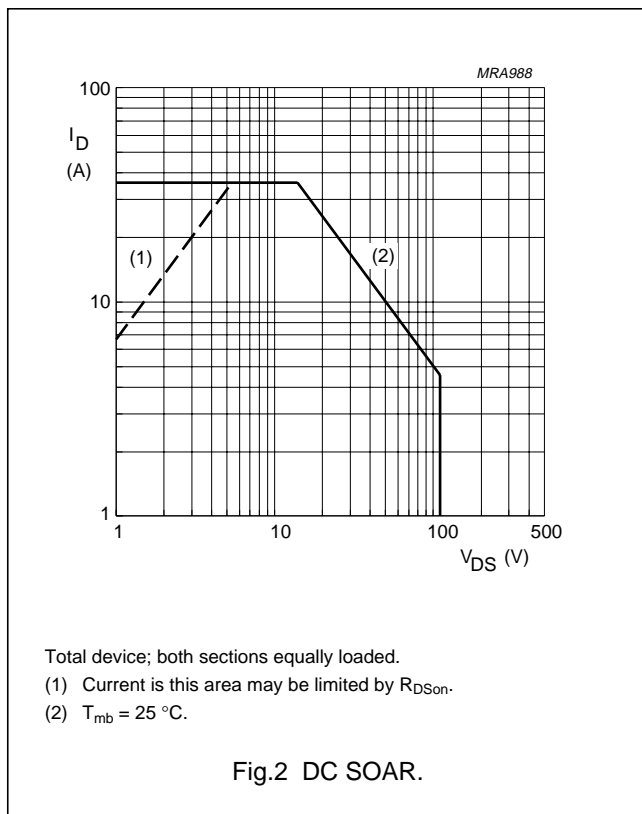
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per transistor section					
V_{DS}	drain-source voltage		–	110	V
V_{GS}	gate-source voltage		–	±20	V
I_D	drain current (DC)		–	18	A
P_{tot}	total power dissipation	up to $T_{mb} = 25\text{ °C}$ total device; both sections equally loaded	–	500	W
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	200	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-mb}$	thermal resistance from junction to mounting base	total device; both sections equally loaded.	max. 0.35	K/W
$R_{th\ mb-h}$	thermal resistance from mounting base to heatsink	total device; both sections equally loaded.	max. 0.15	K/W



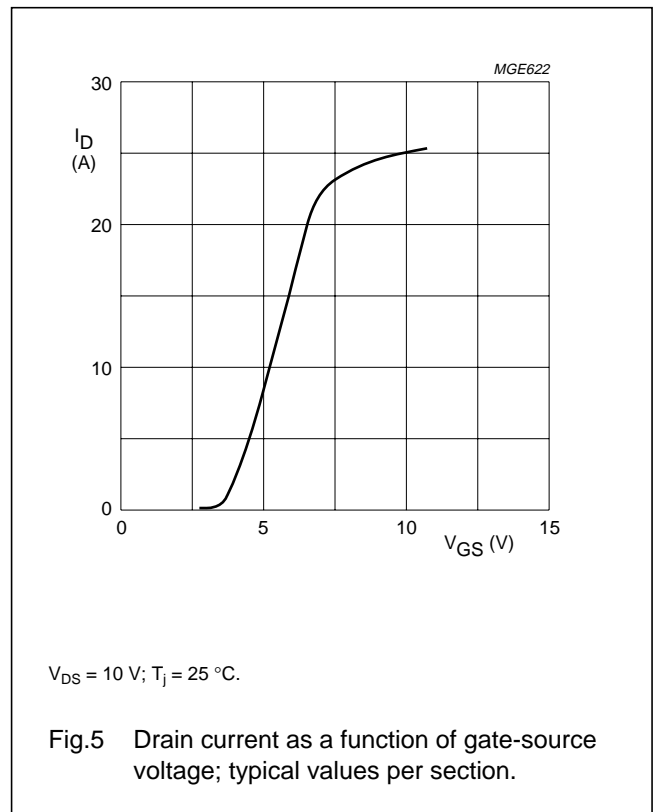
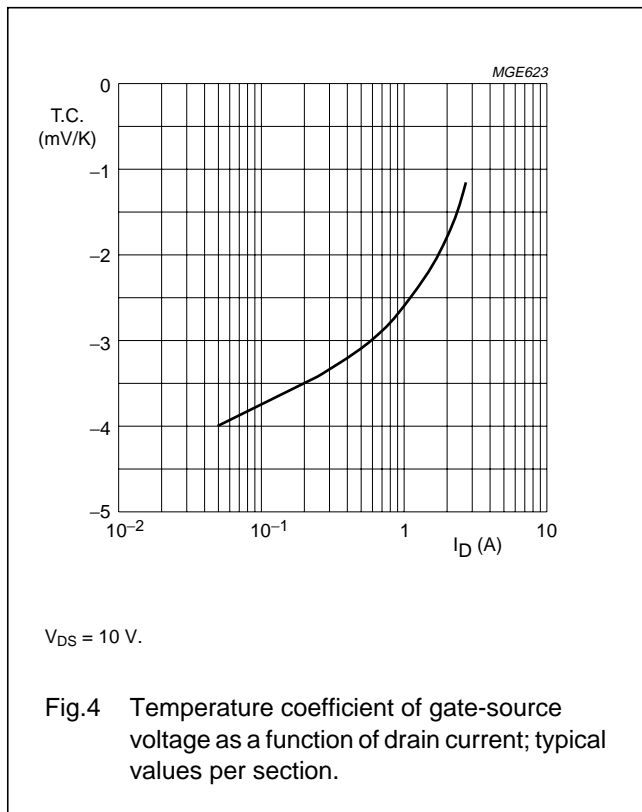
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CHARACTERISTICS

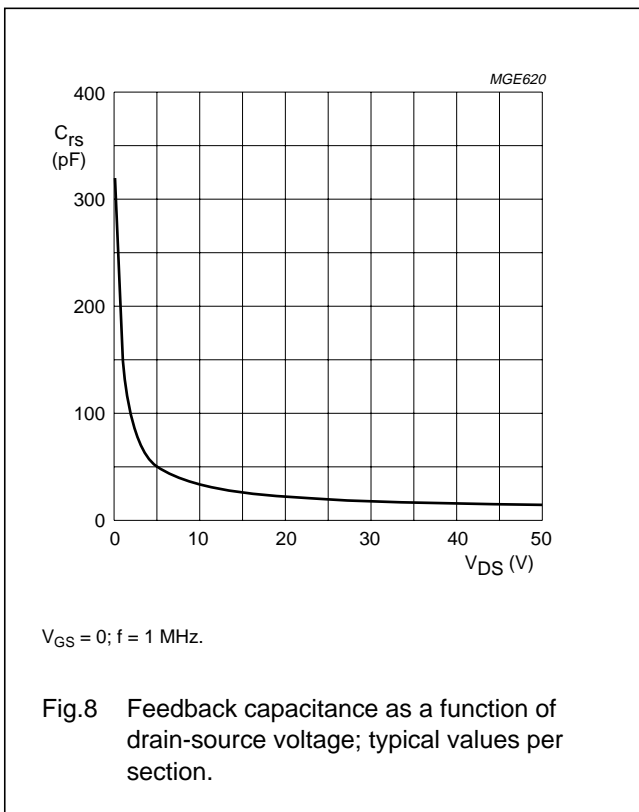
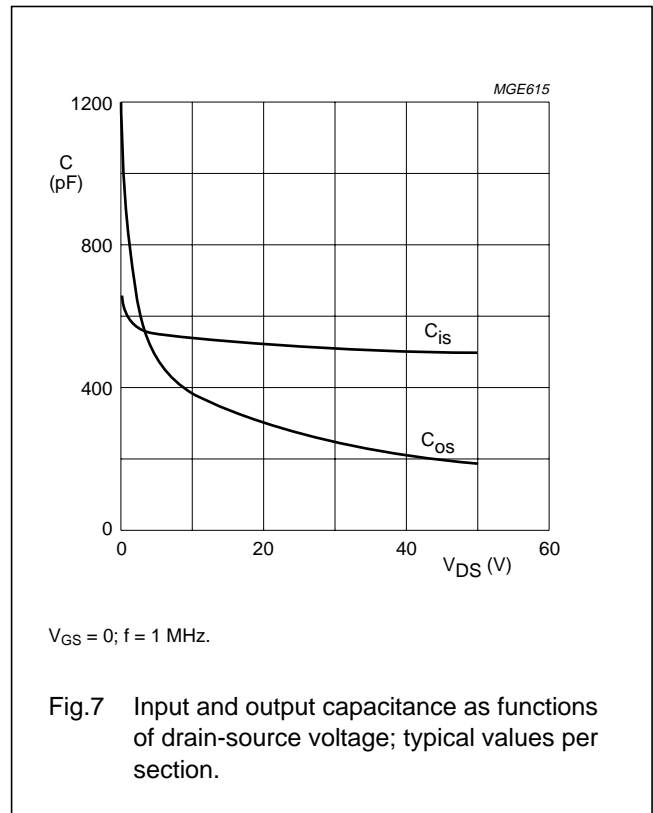
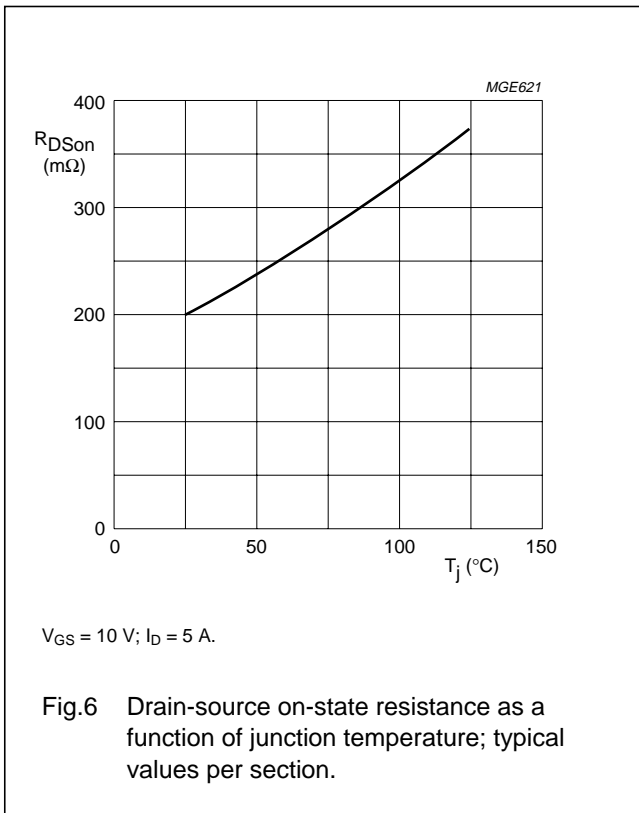
$T_j = 25\text{ }^\circ\text{C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per transistor section						
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0; I_D = 50\text{ mA}$	110	–	–	V
I_{DSS}	drain-source leakage current	$V_{GS} = 0; V_{DS} = 50\text{ V}$	–	–	2.5	mA
I_{GSS}	gate-source leakage current	$V_{GS} = \pm 20\text{ V}; V_{DS} = 0$	–	–	1	μA
V_{GSth}	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 50\text{ mA}$	2	–	4.5	V
ΔV_{GS}	gate-source voltage difference of both sections	$V_{DS} = 10\text{ V}; I_D = 50\text{ mA}$	–	–	100	mV
g_{fs}	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 5\text{ A}$	4.5	6.2	–	S
g_{fs1}/g_{fs2}	forward transconductance ratio of both sections	$V_{DS} = 10\text{ V}; I_D = 5\text{ A}$	0.9	–	1.1	
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 5\text{ A}$	–	0.2	0.3	Ω
I_{DSX}	drain cut-off current	$V_{GS} = 10\text{ V}; V_{DS} = 10\text{ V}$	–	25	–	A
C_{is}	input capacitance	$V_{GS} = 0; V_{DS} = 50\text{ V}; f = 1\text{ MHz}$	–	480	–	pF
C_{os}	output capacitance	$V_{GS} = 0; V_{DS} = 50\text{ V}; f = 1\text{ MHz}$	–	190	–	pF
C_{rs}	feedback capacitance	$V_{GS} = 0; V_{DS} = 50\text{ V}; f = 1\text{ MHz}$	–	14	–	pF
C_{d-f}	drain-flange capacitance		–	5.4	–	pF



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APPLICATION INFORMATION**Class-B operation**

RF performance in CW operation in a common source push-pull test circuit. $T_h = 25\text{ }^\circ\text{C}$; $R_{th\text{ mb-h}} = 0.15\text{ K/W}$ unless otherwise specified. $R_{GS} = 4\text{ }\Omega$ per section; optimum load impedance per section = $3.2 + j4.3\text{ }\Omega$ ($V_{DS} = 50\text{ V}$).

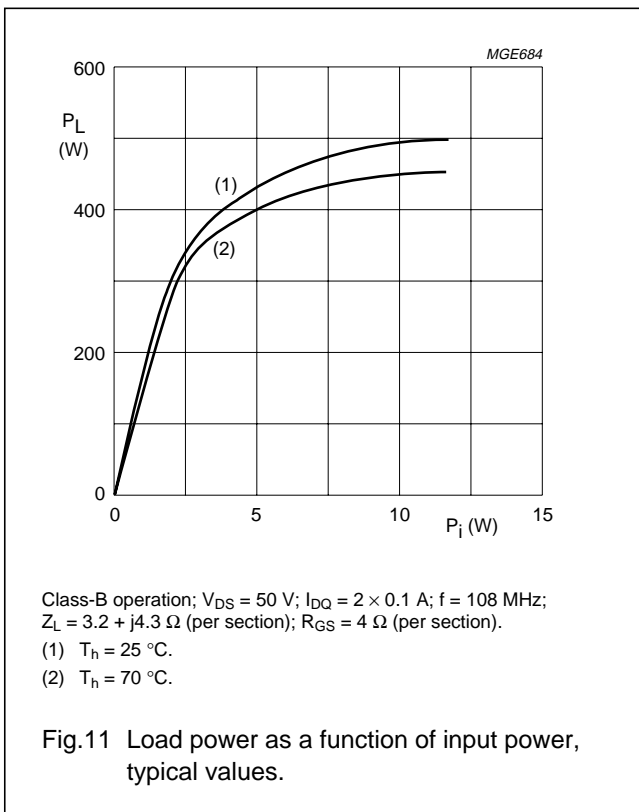
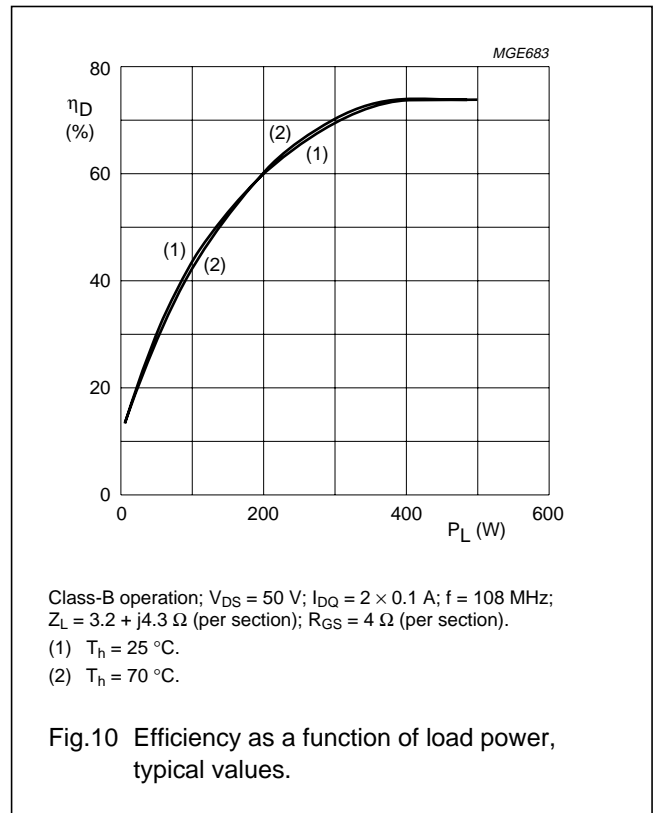
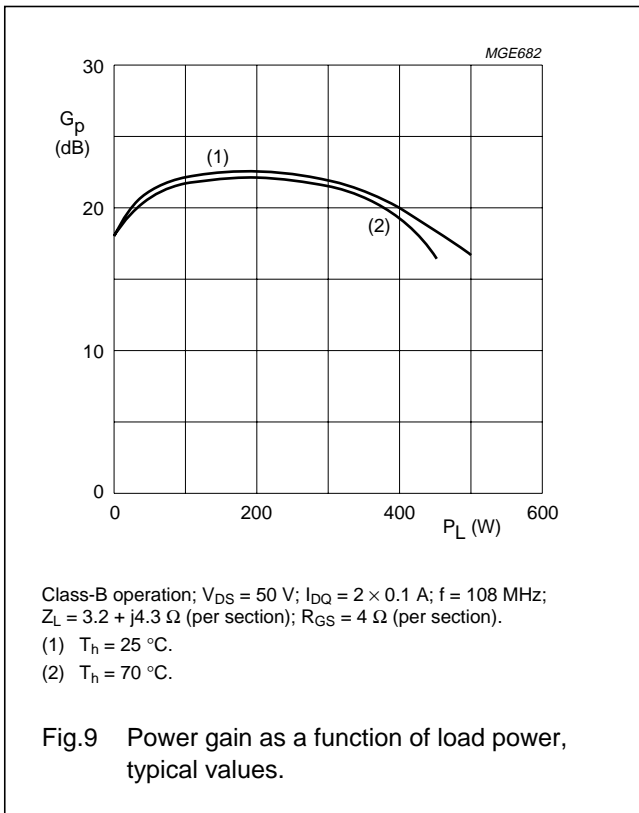
MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (A)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	108	50	2×0.1	300	>20 typ. 22	>60 typ. 70
CW, class-C	108	50	$V_{GS} = 0$	300	typ. 18	typ. 80

Ruggedness in class-B operation

The BLF278 is capable of withstanding a load mismatch corresponding to $V_{SWR} = 7 : 1$ through all phases under the conditions: $V_{DS} = 50\text{ V}$; $f = 108\text{ MHz}$ at rated load power.

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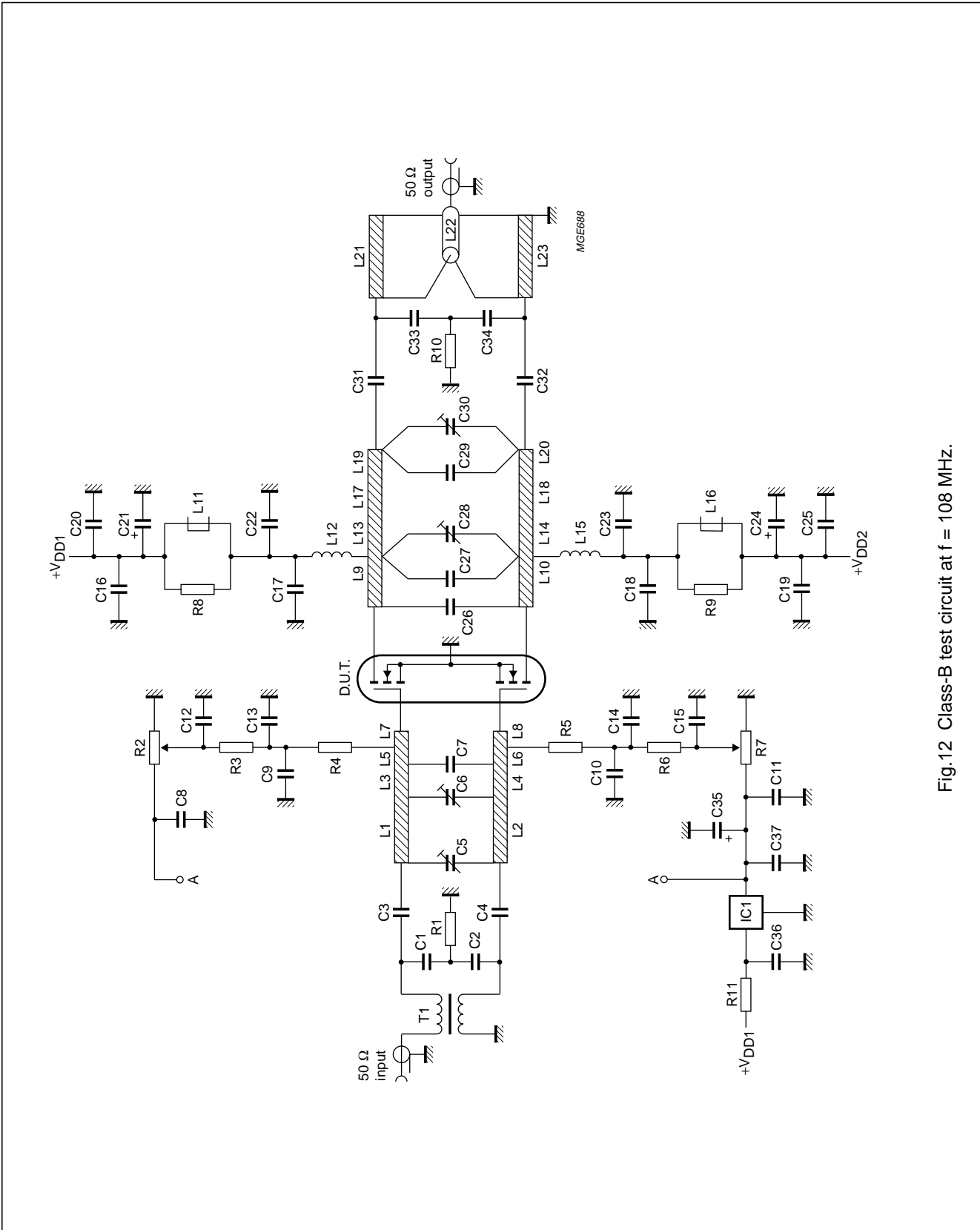


Fig.12 Class-B test circuit at f = 108 MHz.

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List of components (see Figs 12 and 13).

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C2, C33, C34	multilayer ceramic chip capacitor; note 1	22 pF, 500 V		
C3, C4	multilayer ceramic chip capacitor; note 1	100 pF + 68 pF in parallel, 500 V		
C5, C6, C28	film dielectric trimmer	5 to 60 pF		2222 809 08003
C7	multilayer ceramic chip capacitor; note 1	2 × 100 pF + 1 × 120 pF in parallel, 500 V		
C8, C11, C12, C15, C16, C19, C36	multilayer ceramic chip capacitor	100 nF, 500 V		2222 852 47104
C9, C10, C13, C14, C20, C25	multilayer ceramic chip capacitor; note 1	1 nF, 500 V		
C17, C18, C22, C23	multilayer ceramic chip capacitor; note 1	470 pF, 500 V		
C21, C24, C35	electrolytic capacitor	10 µF, 63 V		
C26	multilayer ceramic chip capacitor; note 1	2 × 15 pF + 1 × 18 pF in parallel, 500 V		
C27	multilayer ceramic chip capacitor; note 1	3 × 15 pF in parallel, 500 V		
C29	multilayer ceramic chip capacitor; note 1	2 × 18 pF + 1 × 15 pF in parallel, 500 V		
C30	film dielectric trimmer	2 to 18 pF		2222 809 09006
C31, C32	multilayer ceramic chip capacitor; note 1	3 × 43 pF in parallel, 500 V		
L1, L2	stripline; note 2	43 Ω	length 57.5 mm width 6 mm	
L3, L4	stripline; note 2	43 Ω	length 29.5 mm width 6 mm	
L5, L6	stripline; note 2	43 Ω	length 14 mm width 6 mm	
L7, L8	stripline; note 2	43 Ω	length 6 mm width 6 mm	
L9, L10	stripline; note 2	43 Ω	length 17.5 mm width 6 mm	
L11, L16	2 × grade 3B Ferroxcube wideband HF chokes in parallel			4312 020 36642
L12, L15	4 turns enamelled 2 mm copper wire	85 nH	length 13.5 mm int. dia. 10 mm leads 2 × 7 mm	
L13, L14	stripline; note 2	43 Ω	length 19.5 mm width 6 mm	

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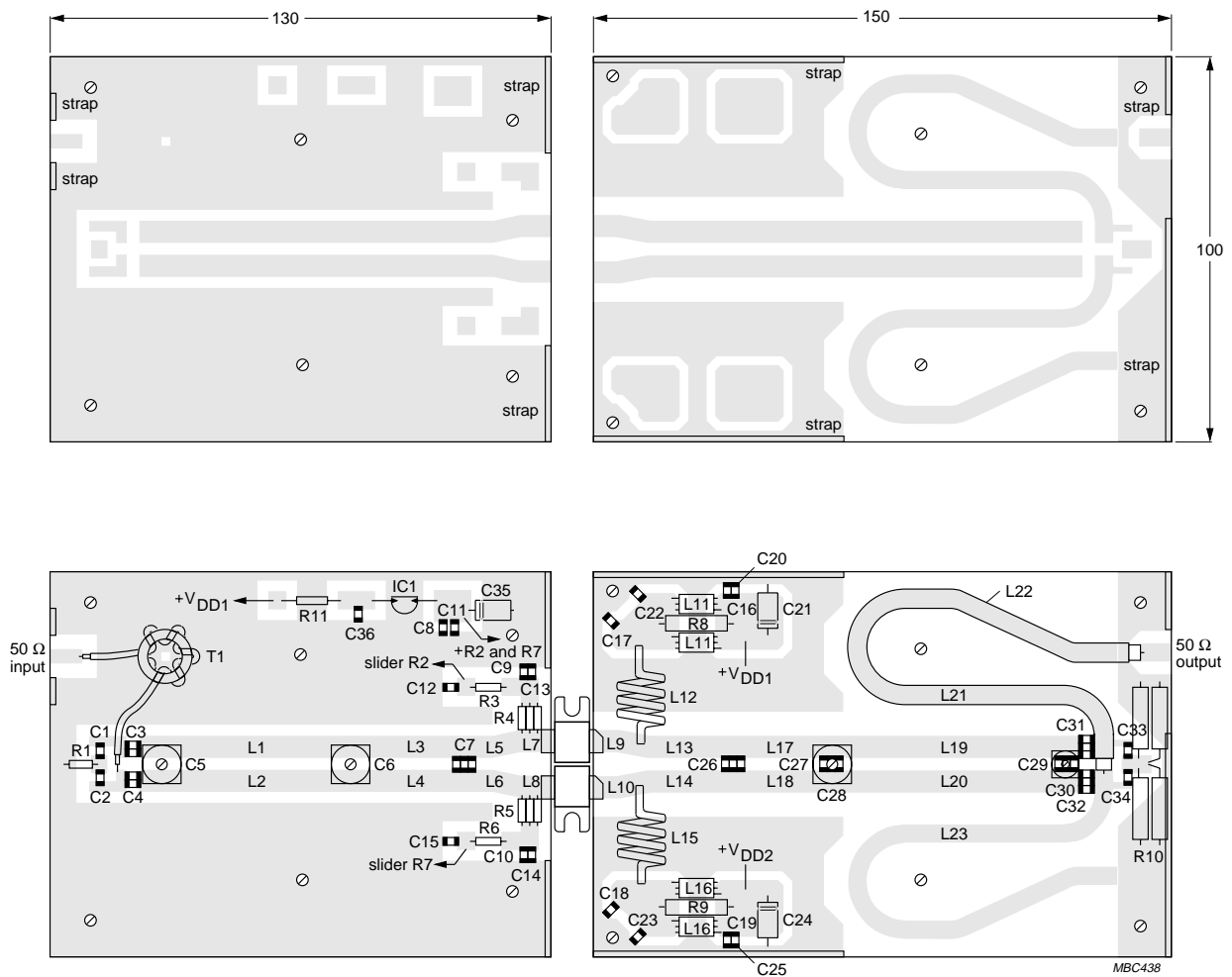
COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
L17, L18	stripline; note 2	43 Ω	length 24.5 mm width 6 mm	
L19, L20	stripline; note 2	43 Ω	length 66 mm width 6 mm	
L21, L23	stripline; note 2	50 Ω	length 160 mm width 4.8 mm	
L22	semi-rigid cable; note 3	50 Ω	ext. dia. 3.6 mm outer conductor length 160 mm	
R1	metal film resistor	10 Ω , 0.4 W		
R2, R7	10 turn potentiometer	50 k Ω		
R3, R6	metal film resistor	3 \times 12.1 Ω in parallel, 0.4 W		
R4, R5	metal film resistor	10 Ω ; 0.4 W		
R8, R9	metal film resistor	10 Ω \pm 5%, 1 W		
R10	metal film resistor	4 \times 10 Ω in parallel, 1 W		
R11	metal film resistor	5.11 k Ω , 1 W		
IC1	voltage regulator 78L05			
T1	1:1 Balun; 7 turns type 4C6 50 Ω coaxial cable wound around toroid		14 \times 9 \times 5 mm	4322 020 90770

Notes

- American Technical Ceramics capacitor, type 100B or capacitor of same quality.
- L1 to L10, L13, L14, L17 to L21 and L23 are striplines on a double copper-clad printed-circuit board, with fibre-glass PTFE dielectric ($\epsilon_r = 2.2$), thickness $\frac{1}{16}$ inch; thickness of copper sheet $2 \times 35 \mu\text{m}$.
- L22 is soldered on to stripline L21.

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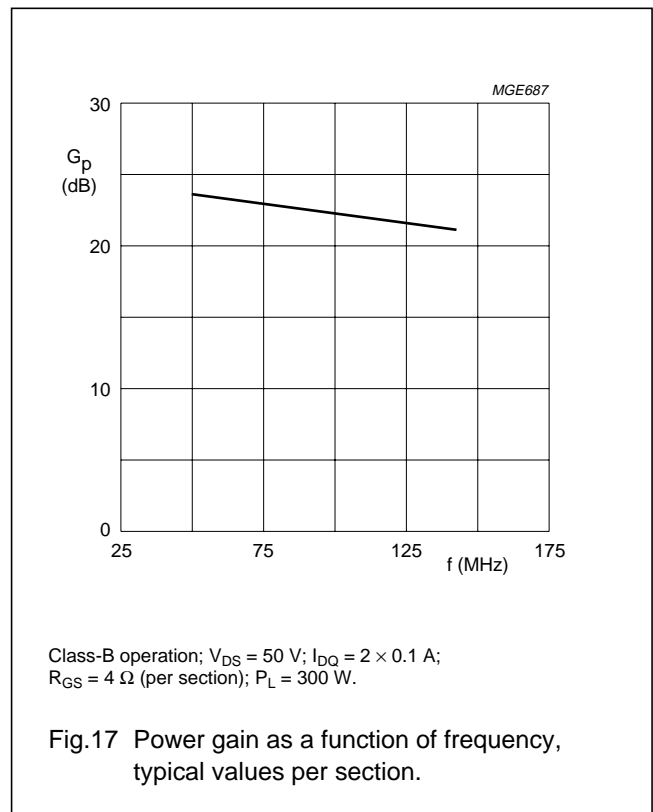
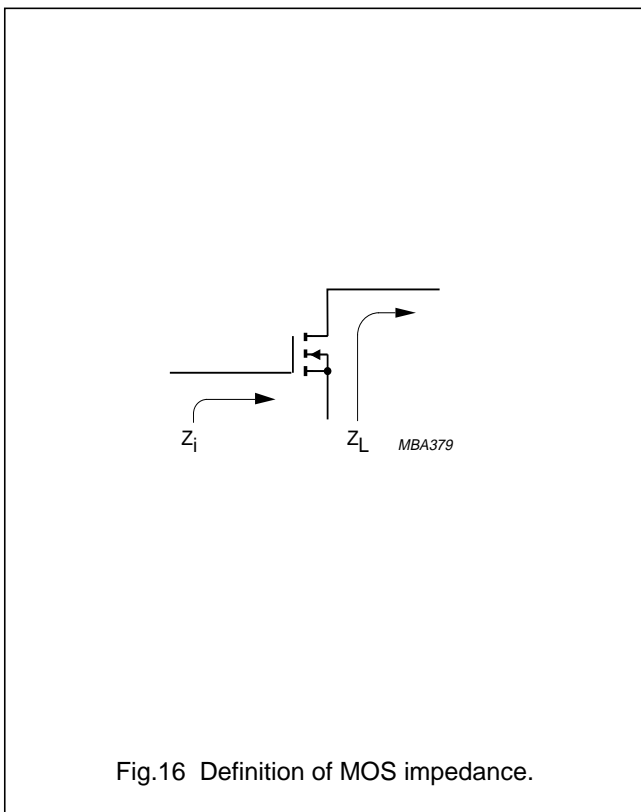
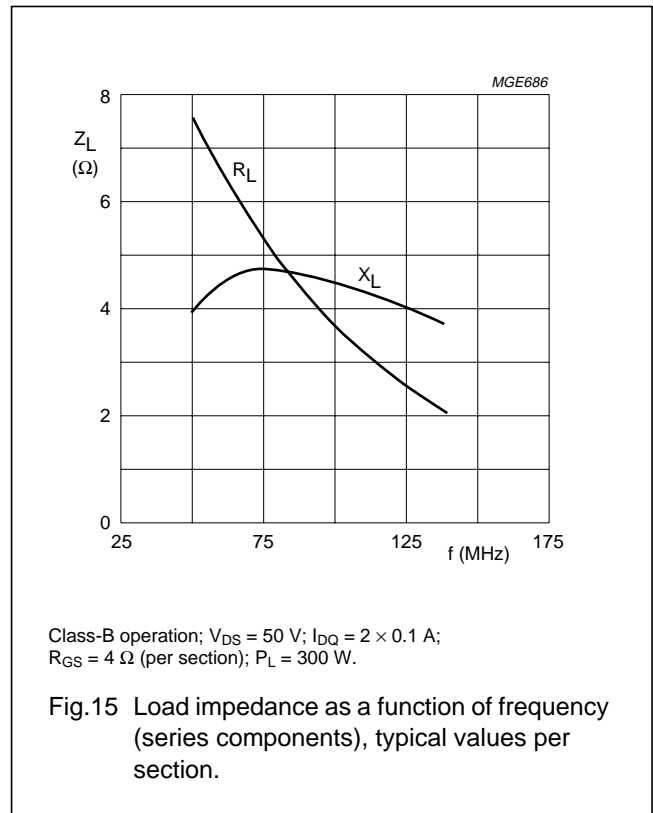
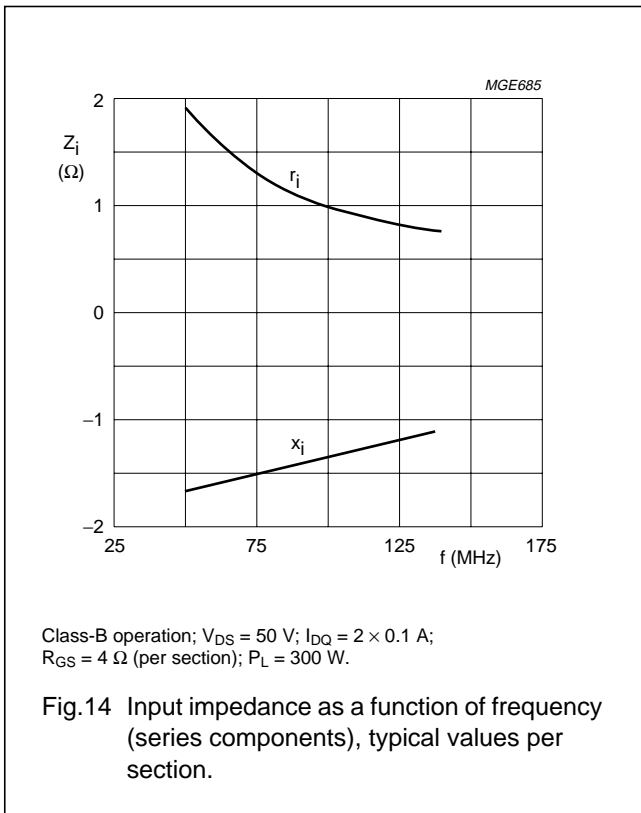
Dimensions in mm.

The circuit and components are situated on one side of the PTFE fibre-glass board, the other side being fully metallized to serve as an earth. Earth connections are made by means of copper straps for a direct contact between upper and lower sheets.

Fig.13 Printed-circuit board and component layout for 108 MHz class-B test circuit.

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Class-AB operation

RF performance in CW operation in a common source push-pull test circuit. $T_h = 25\text{ }^\circ\text{C}$; $R_{th\text{ mb-h}} = 0.15\text{ K/W}$ unless otherwise specified. $R_{GS} = 2.8\ \Omega$ per section; optimum load impedance per section = $0.74 + j2\ \Omega$; ($V_{DS} = 50\text{ V}$).

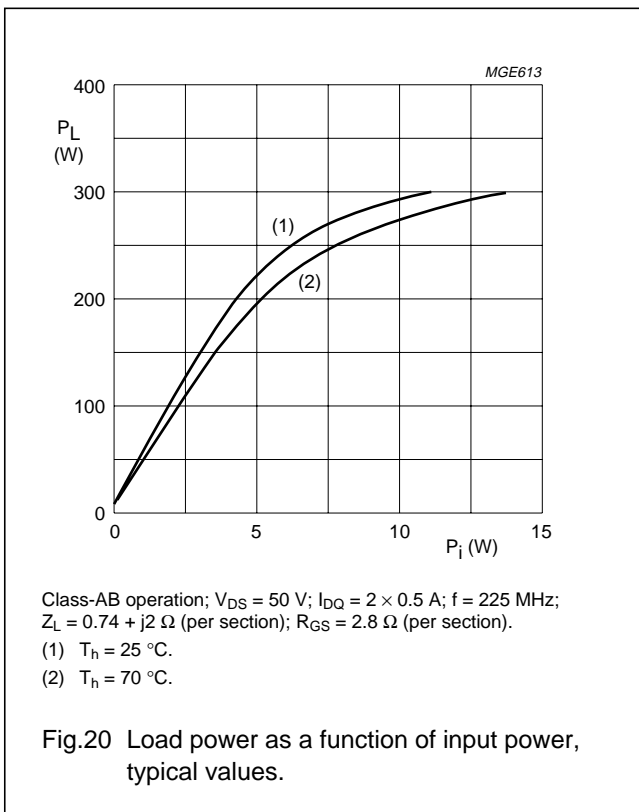
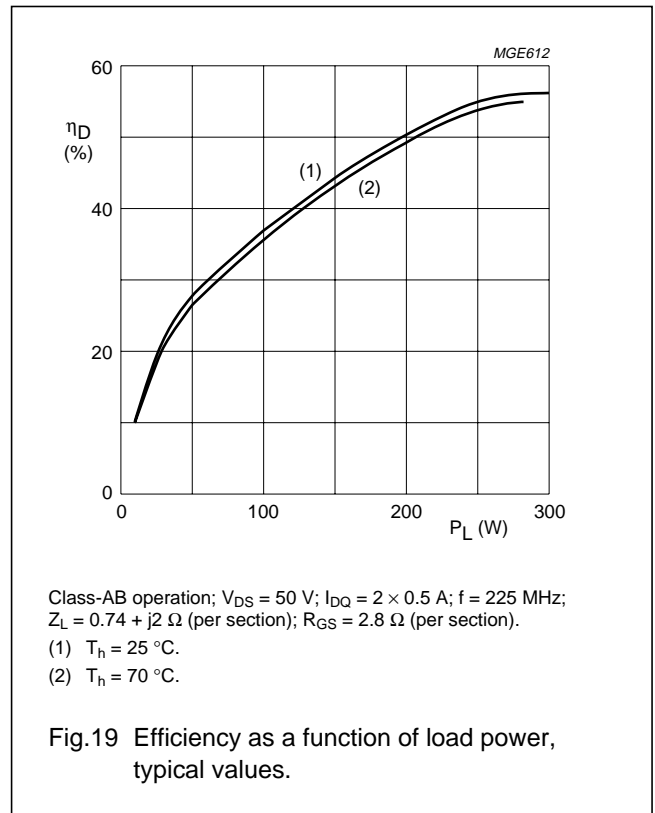
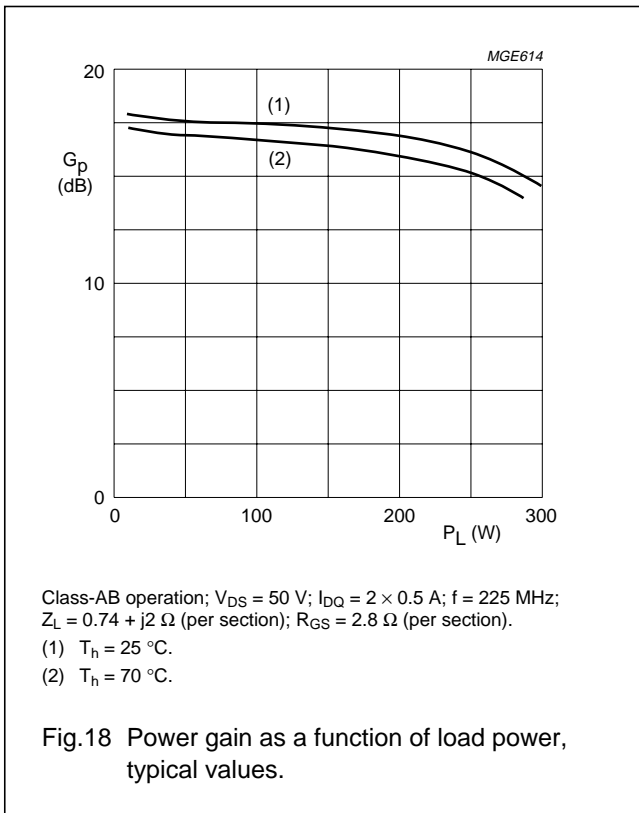
MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (A)	P_L (W)	G_p (dB)	η_D (%)
CW, class-AB	225	50	2×0.5	250	>14 typ. 16	>50 typ. 55

Ruggedness in class-AB operation

The BLF278 is capable of withstanding a load mismatch corresponding to $V_{SWR} = 7 : 1$ through all phases under the conditions: $V_{DS} = 50\text{ V}$; $f = 225\text{ MHz}$ at rated output power.

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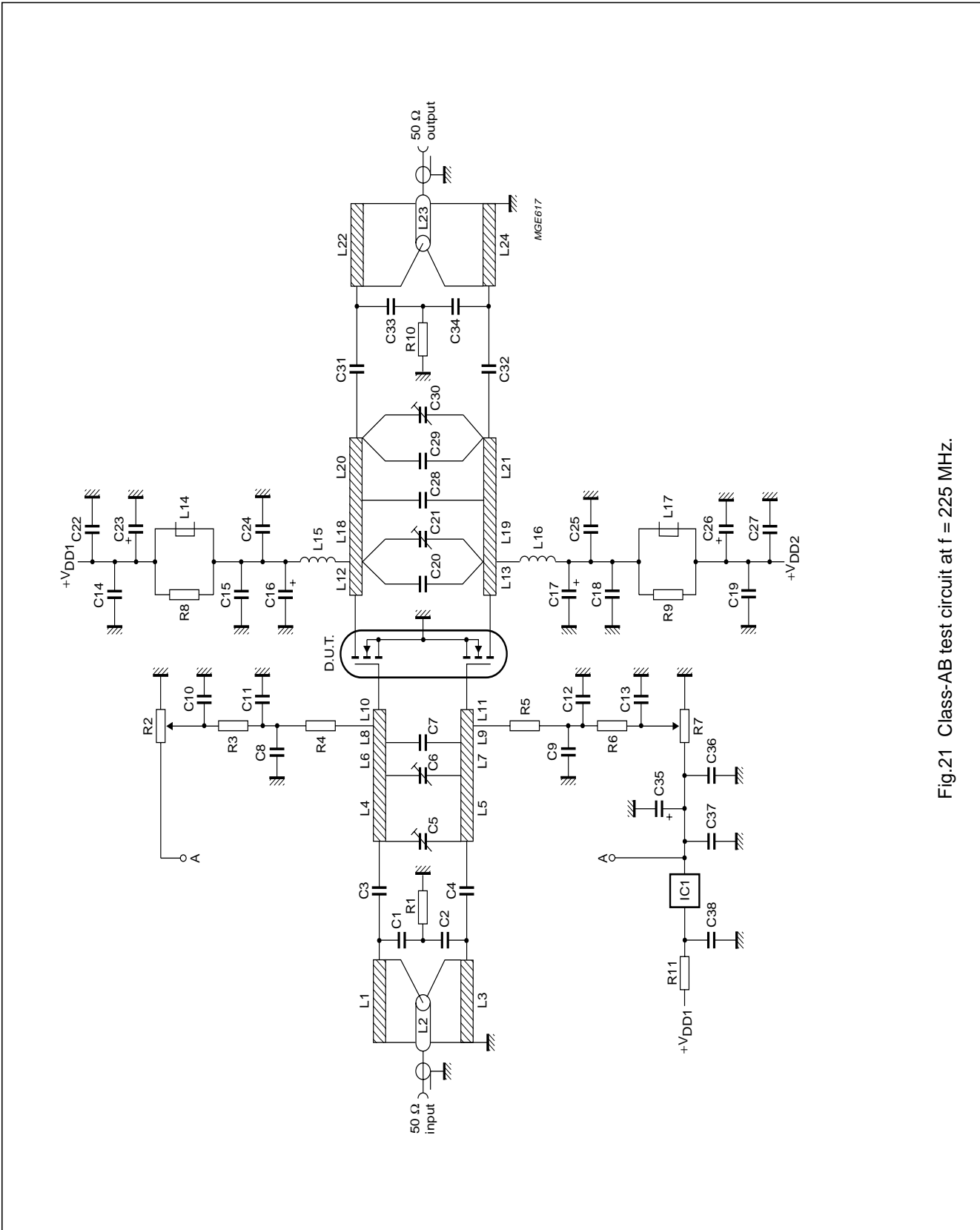


Fig.21 Class-AB test circuit at f = 225 MHz.

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List of components (see Figs 21 and 22).

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C2	multilayer ceramic chip capacitor; note 1	27 pF, 500 V		
C3, C4, C31, C32	multilayer ceramic chip capacitor; note 1	3 × 18 pF in parallel, 500 V		
C5	film dielectric trimmer	4 to 40 pF		2222 809 08002
C6, C30	film dielectric trimmer	2 to 18 pF		2222 809 09006
C7	multilayer ceramic chip capacitor; note 1	100 pF, 500 V		
C8, C9, C15, C18	MKT film capacitor	1 μF, 63 V		2222 371 11105
C10, C13, C14, C19, C36	multilayer ceramic chip capacitor	100 nF, 50 V		2222 852 47104
C11, C12	multilayer ceramic chip capacitor; note 1	2 × 1 nF in parallel, 500 V		
C16, C17	electrolytic capacitor	220 μF, 63 V		
C20	multilayer ceramic chip capacitor; note 1	3 × 33 pF in parallel, 500 V		
C21	film dielectric trimmer	2 to 9 pF		2222 809 09005
C22, C27, C37, C38	multilayer ceramic chip capacitor; note 1	1 nF, 500 V		
C23, C26, C35	electrolytic capacitor	10 μF, 63 V		
C24, C25	multilayer ceramic chip capacitor; note 1	2 × 470 pF in parallel, 500 V		
C28	multilayer ceramic chip capacitor; note 1	2 × 10 pF + 1 × 18 pF in parallel, 500 V		
C29	multilayer ceramic chip capacitor; note 1	2 × 5.6 pF in parallel, 500 V		
C33, C34	multilayer ceramic chip capacitor; note 1	5.6 pF, 500 V		
L1, L3, L22, L24	stripline; note 2	50 Ω	length 80 mm width 4.8 mm	
L2, L23	semi-rigid cable; note 3	50 Ω	ext. dia. 3.6 mm outer conductor length 80 mm	
L4, L5	stripline; note 2	43 Ω	length 24 mm width 6 mm	
L6, L7	stripline; note 2	43 Ω	length 14.5 mm width 6 mm	
L8, L9	stripline; note 2	43 Ω	length 4.4 mm width 6 mm	
L10, L11	stripline; note 2	43 Ω	length 3.2 mm width 6 mm	
L12, L13	stripline; note 2	43 Ω	length 15 mm width 6 mm	

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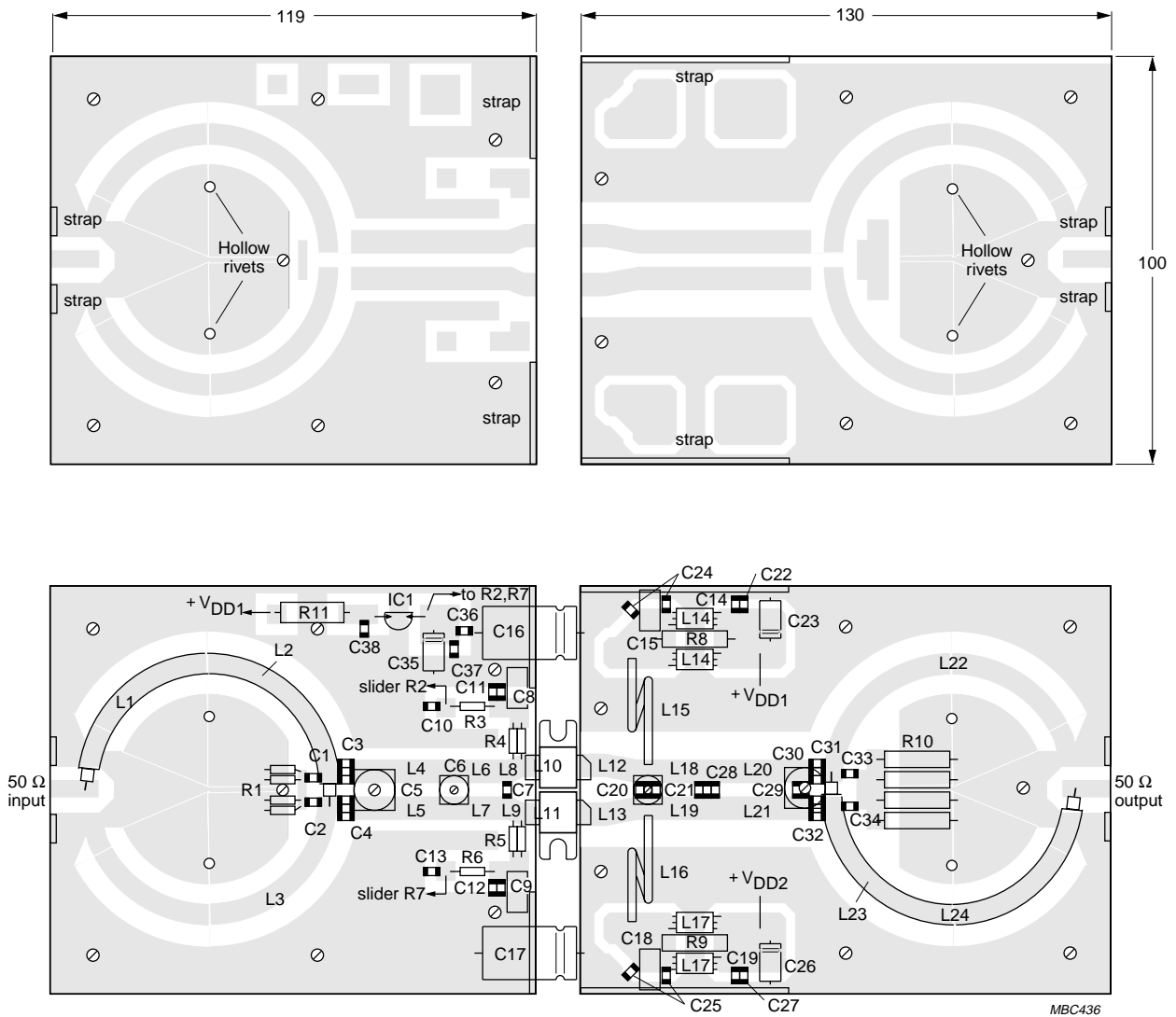
COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
L14, L17	2 × grade 3B Ferroxcube wideband HF chokes in parallel			4312 020 36642
L15, L16	1 $\frac{3}{4}$ turns enamelled 2 mm copper wire	40 nH	int. dia. 10 mm leads 2 × 7 mm space 1 mm	
L18, L19	stripline; note 2	43 Ω	length 13 mm width 6 mm	
L20, L21	stripline; note 2	43 Ω	length 29.5 mm width 6 mm	
R1	metal film resistor	10 Ω, 0.4 W		
R2, R7	10 turns potentiometer	50 kΩ		
R3, R6	metal film resistor	1 kΩ, 0.4 W		
R4, R5	metal film resistor	2 × 5.62 Ω, in parallel, 0.4 W		
R8, R9	metal film resistor	10 Ω ±5%, 1 W		
R10	metal film resistor	4 × 42.2 Ω in parallel, 1 W		
R11	metal film resistor	5.11 kΩ, 1 W		
IC1	voltage regulator 78L05			

Notes

1. American Technical Ceramics capacitor, type 100B or other capacitor of the same quality.
2. L1, L3 to L13, L18 to L22 and L24 are microstriplines on a double copper-clad printed-circuit board, with fibre-glass reinforced PTFE dielectric ($\epsilon_r = 2.2$), thickness $\frac{1}{16}$ inch; thickness of copper sheet 2 × 35 µm.
3. L2 and L23 are soldered on to striplines L1 and L24 respectively.

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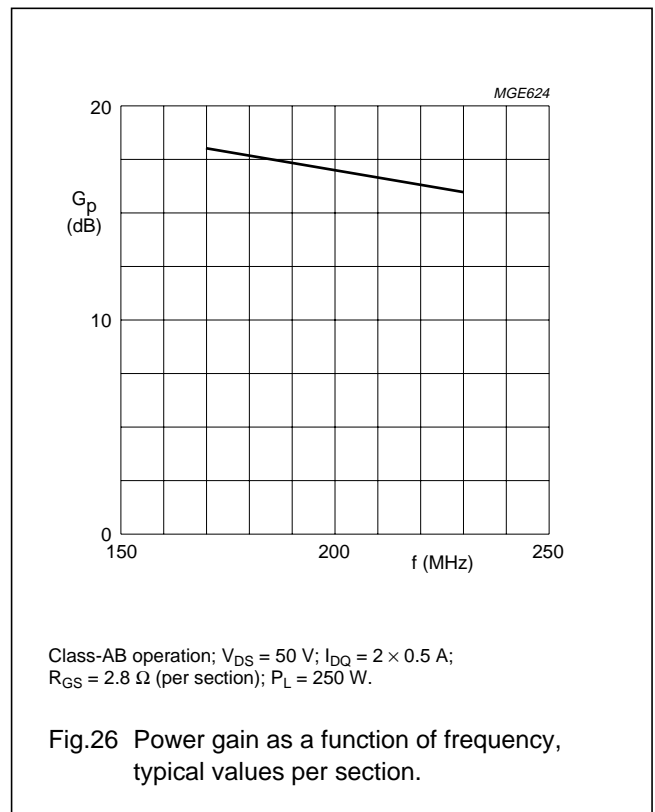
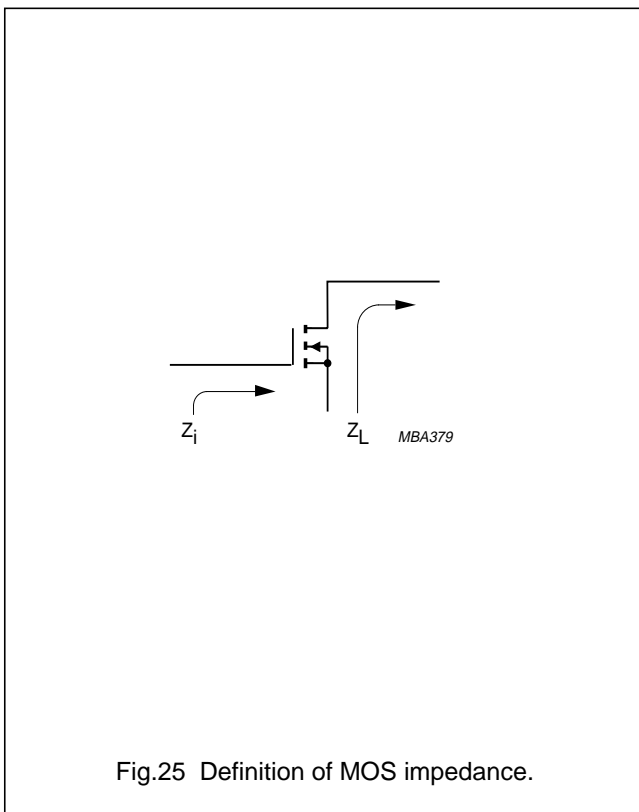
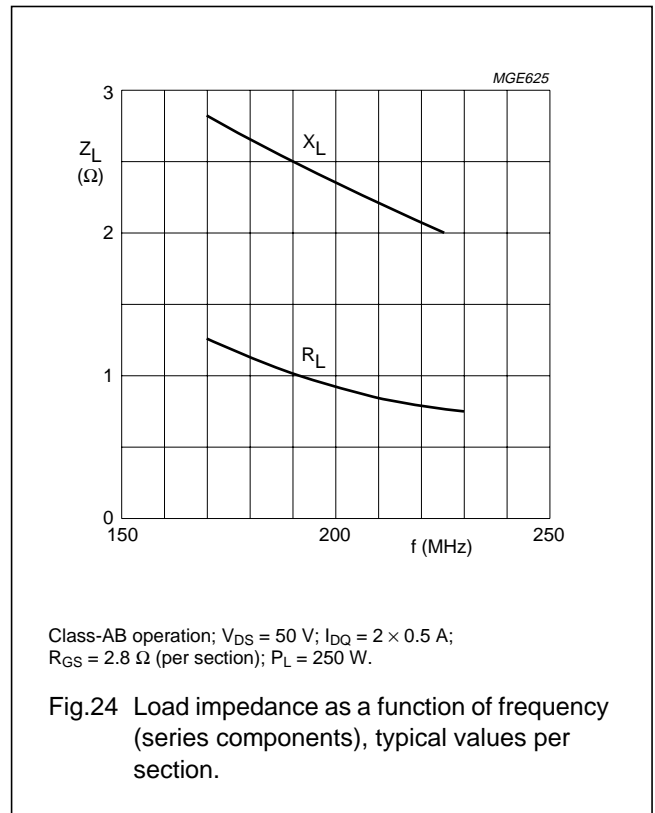
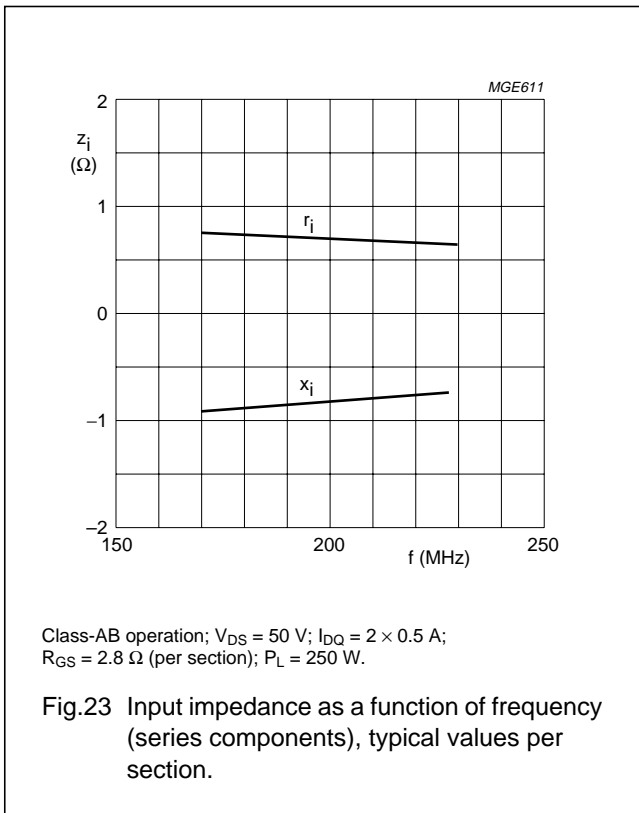
Dimensions in mm.

The circuit and components are situated on one side of the PTFE fibre-glass board, the other side being fully metallized to serve as an earth. Earth connections are made by means of copper straps for a direct contact between upper and lower sheets.

Fig.22 Printed-circuit board and component layout for 225 MHz class-AB test circuit.

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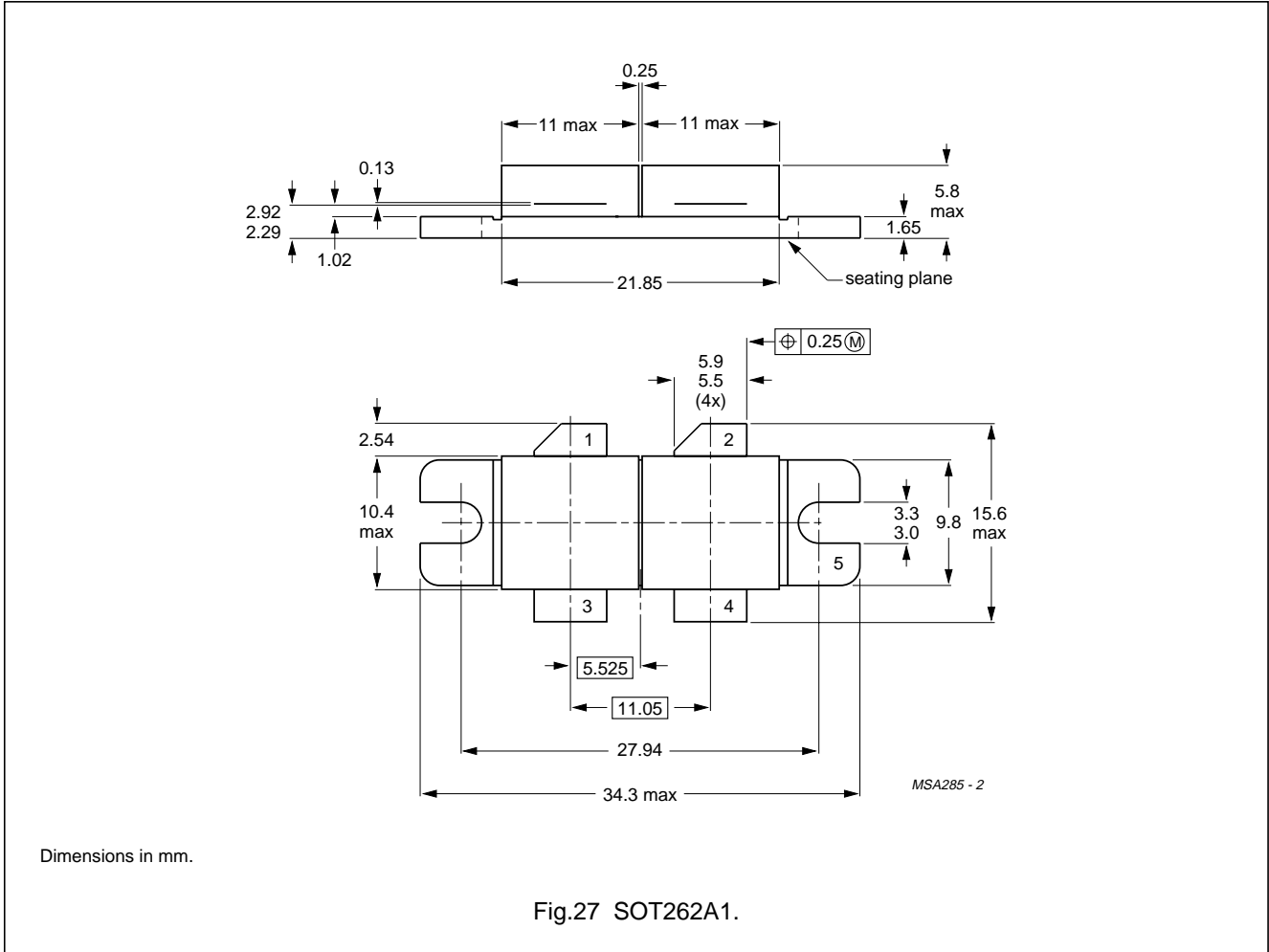
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PACKAGE OUTLINE



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DEFINITIONS

Data Sheet Status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.