PRELIMINARY

NEC

MOS Integrated Circuit

μPD481850

8Mb Synchronous Graphics Memory (128Kword x 32bit x 2 Banks)

μPD481850 is a synchronous graphics memory (SGRAM) organized as 128Kwords x 32bit x 2 Bank random access port.

This device can operate up to 100MHz by using synchronous interface. Also, it has 8 column Block Write function and Write per bit function to improve capability in graphics system.

Features

- 131, 072 x 32 I/O x 2 Banks memory
- Synchronous interface (Fully synchronous DRAM with all input signals are latched at rising edge of clock)
  - Pulsed interface
  - Automatic precharge and controlled precharge commands
  - Ping-pong operation between the two internal memory banks
  - up to 100MHz operation frequency
- Byte control using DQM0 to DQM3 signals both in read and write cycle
- 8 column Block Write (BW) function
- Persistent write per bit (WPB) function
- Programmable burst length (1, 2, 4, 8 and full - page)
- Programmable CAS Latency (1, 2 and 3)
- Power Down operation and Clock Suspend operation
- Auto refresh (CBR refresh) or self refresh capability
- 3.3V power Supply
- LVTTL compatible inputs and outputs
- 100pin QFP (14 x 20mm^2), 0.65mm pitch plastic package

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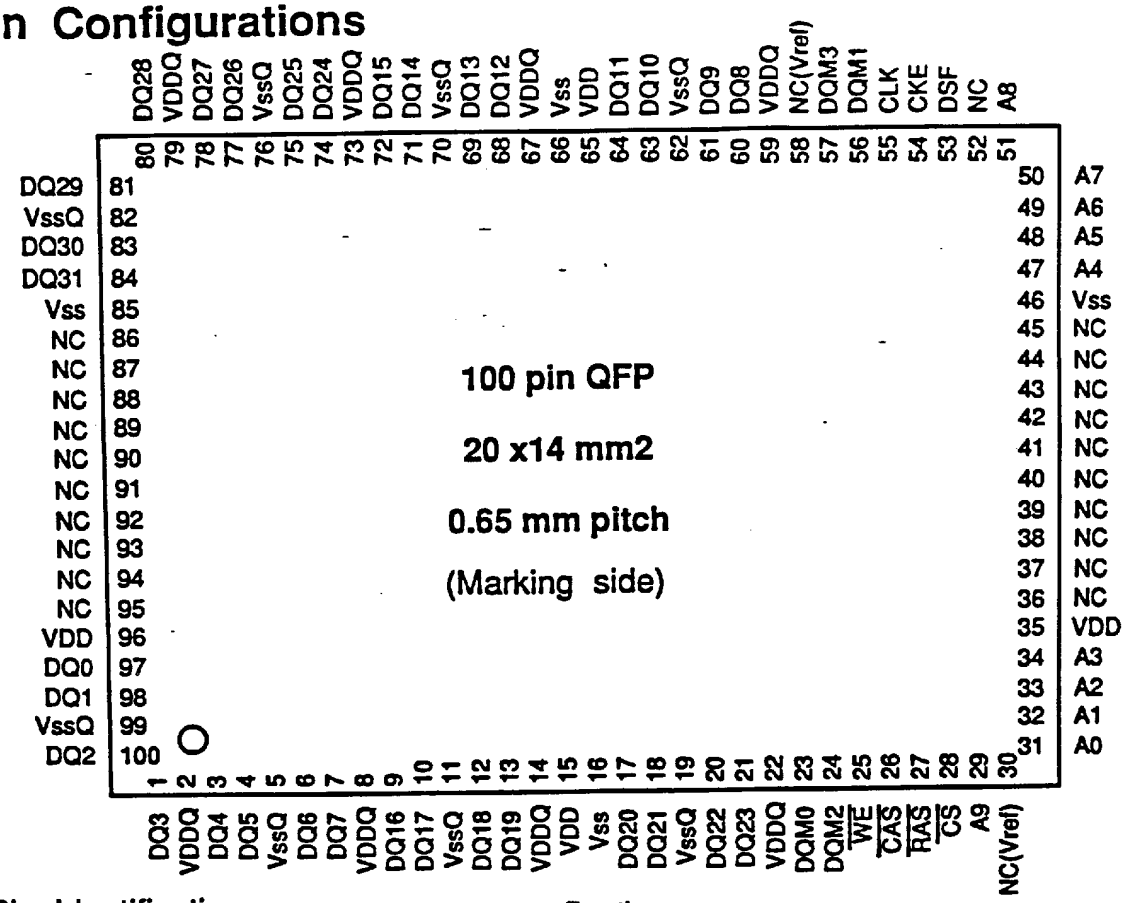
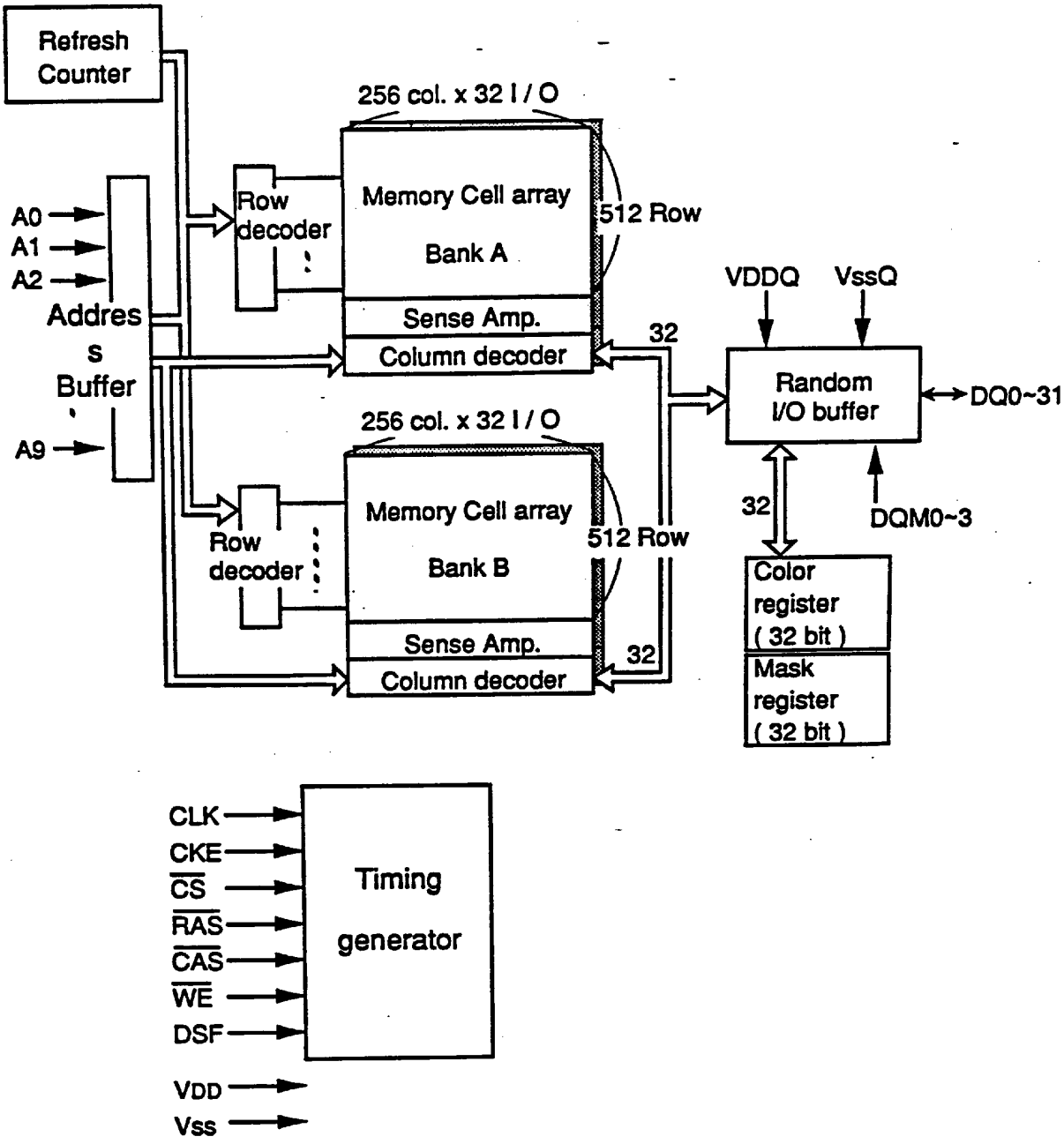
Pin Configurations



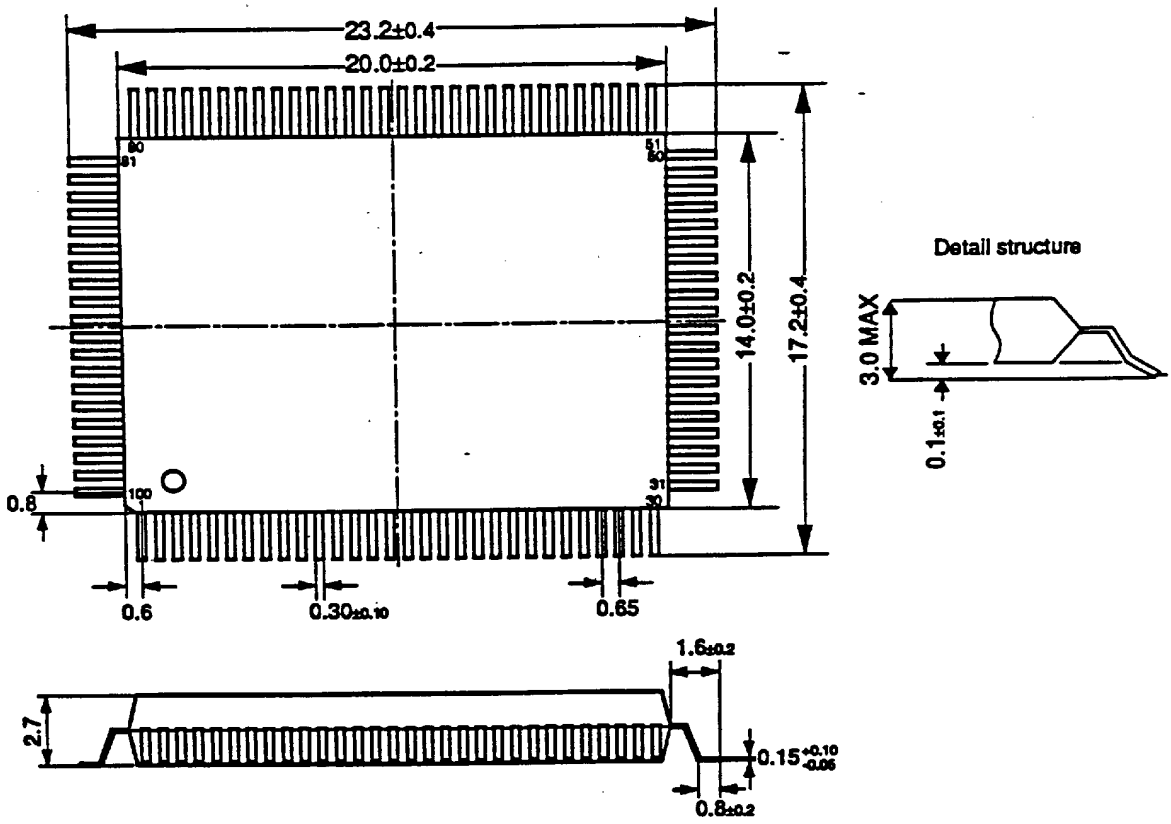
Pin Identification

Symbol	Function
A0 - A9	Address inputs
A0 - A8	Row address inputs
A0 - A7	Column address inputs
A9	Bank select
DQ0 - DQ31	Data inputs / outputs
$\overline{CS}$	Chip select
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
DQM0 - DQM3	DQ mask enable
DSF	Special function enable
CKE	Clock enable
CLK	System clock input
VDD	Supply voltage
Vss	Ground
VDDQ	Supply voltage for DQ
VssQ	Ground for DQ
NC	No Conection

Block Diagram



Package Outline



Signal Description

Name	I / O	Function
CLK	I	The positive edge of the clock input internally, thus allowing data to remain on the output for several clock cycles.
CKE	I	Clock enable disables the clock internally, thus allowing data to remain on the output for several clock cycles. Clock enable is also used as part of the input command to specify self - refresh.
$\overline{CS}$	I	Chip select indicated that the command on the input lines is for this device. If chip select is inactive, the input command will be ignored.
$\overline{RAS}$	I	$\overline{RAS}$ is part of the input command to the SGRAM. See truth table for details.
$\overline{CAS}$	I	$\overline{CAS}$ is part of the input command to the SGRAM. See truth table for details.
$\overline{WE}$	I	Write enable is part of the input command. See truth table for details.
DSF	I	DSF is part of the input command to the SGRAM. If DSF is inactive, SGRAM operates as same as SDRAM.
A0-A9	I	Address bits A0-A8 are row address when active command is activated. Address bits A0-A7 are column address when $\overline{CAS}$ is active. Address bit A8, when $\overline{CAS}$ is active, enables / disables auto precharge. Address bit A9 selects which of the two memory banks is to be used.

Name	I / O	Function
DQ0-DQ31	I/O	Data input / output lines transfer data between the memory array and the system bus. These are also input mask bits for Write-per-bit. When Block-Write command is activated, column address mask signals are input from these pins.
DQM0-DQM3	I	Data output mask turns off the output buffers during a read. During a write, DQM active prevents a write to the current memory location. DQM0 corresponds to the lowest byte (DQ0-7), DQM1 corresponds to DQ8-15, DQM2 corresponds to DQ16-23, and DQM2 corresponds to DQ24-31.

Commands

Mode register set command

($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DSF = Low)

μPD481850 has mode register that define how the device operates. In this command, A0 - A9 are data input pins.
After power-on, the mode register set command must be executed to initialize the device.
The mode register can be set only when both banks are in idle status.
During the two cycles following this command, μPD481850 cannot accept any other commands.

Row active command

($\overline{CS}$, $\overline{RAS}$, DSF = Low, $\overline{CAS}$, $\overline{WE}$ = High)

μPD481850 has two banks, each with 512 rows.
This command activates the bank selected by A9 (BS) and row address selected by A0 - A8.
The command corresponds to a conventional DRAM's falling $\overline{RAS}$ signal.

Row active command with WPB enable

($\overline{CS}$, $\overline{RAS}$ = Low, $\overline{CAS}$, $\overline{WE}$, DSF = High)

This command is same as Row active command except WPB enable.
After this command, write per bit function is available. Mask register's data is used as WPB data.

Precharge command

($\overline{CS}$, $\overline{RAS}$, $\overline{WE}$, DSF = Low, $\overline{CAS}$ = High)

This command begins precharge operation of the bank selected by A9(BS) and A8.
When A8 is high, both banks are precharged, regardless of A9. When A8 is Low, only the bank selected by A9 is precharged. A9 low selects bank A and A9 high selects bank B.
After this command, μPD481850 can't accept the active command to the precharging bank tRP (precharge to active command period).
The command corresponds to a conventional DRAM's rising $\overline{RAS}$ signal.

Column address and Write command

($\overline{CS}$, $\overline{CAS}$, $\overline{WE}$, DSF = Low, $\overline{RAS}$ = High)

If the mode register is in the burst write mode, this command sets the burst start address given by the column address to begin the burst write operation. The first write data must be input with this write operation. The first write data in burst mode can input with this command with subsequent data on following clocks.

Column address and Read command

($\overline{CS}$, $\overline{CAS}$, DSF = Low, $\overline{RAS}$, $\overline{WE}$ = High)

This command sets the burst start address given by the column address.
Read data is available after $\overline{CAS}$ Latency requirements have been met.

CBR(Auto) refresh command

($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, DSF = Low, CKE, $\overline{WE}$ = High)

This command is a request to begin the CBR refresh operation. The refresh address and the bank select address are generated internally.
Before executing CBR refresh, both banks must be precharged.
After this cycle, both banks will be in the idle (prechage) state and ready for a row active command.
During tRC period (from refresh command to refresh or active command), μPD481850 cannot accept any other command.

Self - refresh Entry command

($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, DSF, CKE = Low, $\overline{WE}$ = High)

After the command execution, self refresh operation continues while CKE remains low.
When CKE goes high, the μPD481850 exits the self-refresh mode.
During self-refresh mode, refresh interval and refresh operation are preformed internally, so there is no need for external control.
Before executing self-refresh, both banks must be precharged.

Burst stop command

($\overline{CS}$, $\overline{WE}$, DSF = Low, $\overline{RAS}$, $\overline{CAS}$, = High)

This command is stop the current burst operation.
During read cycles, burst data stops after $\overline{CAS}$ Latency requirements have been met.

No Operation

($\overline{CS}$, $\overline{DSF}$ = Low, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ = High)

This command is not a execution command. No operations begin or terminate by this command.

Special register set command

($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ = Low, DSF = High)

Color and Mask register is set by this command.
During the two cycles following this command, μPD481850 cannot accept any other commands.

Column address and Masked Block write command

($\overline{CS}$, $\overline{CAS}$, $\overline{WE}$ = Low, $\overline{RAS}$, DSF = High)

This command activates 8 column Block write function. This command assumed as burst length=1.
Write data comes from color register, column address mask data is input from DQ.

COMMAND TRUTH TABLE

Operation	CKE n-1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	ADD A9	ADD A8	ADD A7-A0	Mnemonic
Device Deselect	H	X	H	X	X	X	X	X	X	X	DESEL
No Operation	H	X	L	H	H	H	L	X	X	X	NOP
Burst Termination	H	X	L	H	H	L	L	X	X	X	STOP
Column Address and Read Command	H	X	L	H	L	H	L	BA	L	Col.	READ
Read and Auto Precharge	H	X	L	H	L	H	L	BA	H	Col.	READA
Column Address and Write Command	H	X	L	H	L	L	L	BA	L	Col.	WRITE
Write and Auto Precharge	H	X	L	H	L	L	L	BA	H	Col.	WRITEA
Column Address and Masked Block Write	H	X	L	H	L	L	H	BA	L	Col.	BW
Masked Block Write and Auto Precharge	H	X	L	H	L	L	H	BA	H	Col.	BWA
Row Address and Bank Activate	H	X	L	L	H	H	L	BA	Row Add.		ACT
Row address and Bank Activate WPB enable	H	X	L	L	H	H	H	BA	Row Add.		ACTWPB
Single Bank Deactivate/Precharge	H	X	L	L	H	L	L	BA	L	X	PRE
Precharge All Banks	H	X	L	L	H	L	L	X	H	X	PALL
Mode Register Set	H	X	L	L	L	L	L	OP.CODE			MRS
Special Register Set	H	X	L	L	L	L	H	OP. CODE			SRS

DQM TRUTH TABLE

Operation	CKE n-1	CKE n	DQM 3-0	Mnemonic
Data Write/Output Enable	H	X	L	ENBL
Data Mask/Output Disable	H	X	H	MASK

CKE TRUTH TABLE

Current State	CKE n-1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	ADD	Function	Mnemonic
Activating	H	L	X	X	X	X	X	X	Clock Suspend Mode Entry	
Any	L	L	X	X	X	X	X	X	Clock Suspend	
Clock Suspend	L	H	X	X	X	X	X	X	Clock Suspend Mode Exit	
IDLE	H	H	L	L	L	H	L	X	CBR Refresh	REF
IDLE	H	L	L	L	L	H	L	X	Self Refresh Entry	SREF
Self Refresh	L	H	H	X	X	X	X	X	Self Refresh Exit	
	L	H	L	H	H	H	X	X		
IDLE	H	L	X	X	X	X	X	X	Power Down Entry	
Power Down	L	H	X	X	X	X	X	X	Power Down Exit	

<Legend> BA : Bank Address
Col : Column address

H : Logic High
L : Logic Low
X : Don't care (High or Low)

SGRAM FUNCTION TRUTH TABLE

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	ADD	COMMAND	ACTION
IDLE	H	X	X	X	X	X	DESEL	NOP
	L	H	H	H	X	X	NOP	NOP
	L	H	H	L	H	X	Undefined	ILLEGAL
	L	H	H	L	L	X	STOP	ILLEGAL 2
	L	H	L	H	H	X	Undefined	ILLEGAL
	L	H	L	H	L	BA,CA,A8	READ/READA	ILLEGAL 2
	L	H	L	L	H	BA,CA,A8	BW/BWA	ILLEGAL 2
	L	H	L	L	L	BA,CA,A8	WRITE/WRITEA	ILLEGAL 2
	L	L	H	H	H	BA,RA	ACTWPB	Row active; Latch Row Address; Use Mask
	L	L	H	H	L	BA,RA	ACT	Row active; Latch Row Address; No Mask
	L	L	H	L	H	X	Undefined	ILLEGAL
	L	L	H	L	L	BA,A8	PRE	NOP 4
	L	L	L	H	H	X	Undefined	ILLEGAL
	L	L	L	H	L	X	REF	Auto Refresh 5
	L	L	L	L	H	Op-code	SRS	Special Register Access 5
	L	L	L	L	L	Op-code	MRS	Mode Register Access 5
ROW ACTIVE	H	X	X	X	X	X	DESEL	NOP
	L	H	H	H	X	X	NOP	NOP
	L	H	H	L	H	X	Undefined	ILLEGAL
	L	H	H	L	L	X	STOP	ILLEGAL 2
	L	H	L	H	H	X	Undefined	ILLEGAL
	L	H	L	H	L	BA,CA,A8	READ/READA	Begin Read; Latch CA; Determine AP
	L	H	L	L	H	BA,CA,A8	BW/BWA	Block Write; Latch CA; Determine AP
	L	H	L	L	L	BA,CA,A8	WRITE/WRITEA	Begin Write; Latch CA; Determine AP
	L	L	H	H	H	BA,RA	ACTWPB	ILLEGAL 2
	L	L	H	H	L	BA,RA	ACT	ILLEGAL 2
	L	L	H	L	H	X	Undefined	ILLEGAL
	L	L	H	L	L	BA,A8	PRE	Precharge
	L	L	L	H	H	X	Undefined	ILLEGAL
	L	L	L	H	L	X	REF	ILLEGAL
	L	L	L	L	H	Op-code	SRS	Special Register Access
	L	L	L	L	L	Op-code	MRS	ILLEGAL

SGRAM FUNCTION TRUTH TABLE (continued)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	ADD	COMMAND	ACTION
READ	H	X	X	X	X	X	DESEL	NOP(Continue Burst to End;=>Row Active)
	L	H	H	H	X	X	NOP	NOP(Continue Burst to End;=>Row Active)
	L	H	H	L	H	X	Undefined	ILLEGAL
	L	H	H	L	L	X	STOP	NOP(Continue Burst to End) or Term Burst(only Full Page);=>Row Active
	L	H	L	H	H	X	Undefined	ILLEGAL
	L	H	L	H	L	BA,CA,A8	READ/READA	Term Burst,New Read; Determine AP 3
	L	H	L	L	H	BA,CA,A8	BW/BWA	Term Burst,Block Write; Determine AP 3
	L	H	L	L	L	BA,CA,A8	WRITE/WRITEA	Term Burst,Start Write; Determine AP 3
	L	L	H	H	H	BA,RA	ACTWPB	ILLEGAL 2
	L	L	H	H	L	BA,RA	ACT	ILLEGAL 2
	L	L	H	L	H	X	Undefined	ILLEGAL
	L	L	H	L	L	BA,A8	PRE	Term Burst,Precharge Timing for Reads
	L	L	L	H	H	X	Undefined	ILLEGAL
	L	L	L	H	L	X	REF	ILLEGAL
	L	L	L	L	H	Op-code	SRS	ILLEGAL
	L	L	L	L	L	Op-code	MRS	ILLEGAL
WRITE	H	X	X	X	X	X	DESEL	NOP(Continue Burst to End;=>Write Recovering)
	L	H	H	H	X	X	NOP	NOP(Continue Burst to End;=>Write Recovering)
	L	H	H	L	H	X	Undefined	ILLEGAL
	L	H	H	L	L	X	STOP	NOP(Continue Burst to End) or Term Burst(only Full Page);=>Row Active
	L	H	L	H	H	X	Undefined	ILLEGAL
	L	H	L	H	L	BA,CA,A8	READ/READA	Term Burst,Start Read; Determine AP 3
	L	H	L	L	H	BA,CA,A8	BW/BWA	Term Burst,Block Write; Determine AP 3
	L	H	L	L	L	BA,CA,A8	WRITE/WRITEA	Term Burst,New Write; Determine AP 3
	L	L	H	H	H	BA,RA	ACTWPB	ILLEGAL 2
	L	L	H	H	L	BA,RA	ACT	ILLEGAL 2
	L	L	H	L	H	X	Undefined	ILLEGAL
	L	L	H	L	L	BA,A8	PRE	Term Burst,Precharge Timing for Writes 3
	L	L	L	H	H	X	Undefined	ILLEGAL
	L	L	L	H	L	X	REF	ILLEGAL
	L	L	L	L	H	Op-code	SRS	ILLEGAL
	L	L	L	L	L	Op-code	MRS	ILLEGAL

SGRAM FUNCTION TRUTH TABLE (continued)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	ADD	COMMAND	ACTION
READ	H	X	X	X	X	X	DESEL	NOP(Continue Burst to End;=>Precharge)
with	L	H	H	H	X	X	NOP	NOP(Continue Burst to End;=>Precharge)
AUTO	L	H	H	L	H	X	Undefined	ILLEGAL
Precharge	L	H	H	L	L	X	STOP	ILLEGAL
	L	H	L	H	H	X	Undefined	ILLEGAL
	L	H	L	H	L	BA,CA,A8	READ/READA	ILLEGAL
	L	H	L	L	H	BA,CA,A8	BW/BWA	ILLEGAL
	L	H	L	L	L	BA,CA,A8	WRITE/WRITEA	ILLEGAL
	L	L	H	H	H	BA,RA	ACTWPB	ILLEGAL 2
	L	L	H	H	L	BA,RA	ACT	ILLEGAL 2
	L	L	H	L	H	X	Undefined	ILLEGAL
	L	L	H	L	L	BA,A8	PRE	ILLEGAL 2
	L	L	L	H	H	X	Undefined	ILLEGAL
	L	L	L	H	L	X	REF	ILLEGAL
	L	L	L	L	H	Op-code	SRS	ILLEGAL
	L	L	L	L	L	Op-code	MRS	ILLEGAL
WRITE	H	X	X	X	X	X	DESEL	NOP(Continue Burst to End;=>Precharge)
with	L	H	H	H	X	X	NOP	NOP(Continue Burst to End;=>Precharge)
AUTO	L	H	H	L	H	X	Undefined	ILLEGAL
Precharge	L	H	H	L	L	X	STOP	ILLEGAL
	L	H	L	H	H	X	Undefined	ILLEGAL
	L	H	L	H	L	BA,CA,A8	READ/READA	ILLEGAL
	L	H	L	L	H	BA,CA,A8	BW/BWA	ILLEGAL
	L	H	L	L	L	BA,CA,A8	WRITE/WRITEA	ILLEGAL
	L	L	H	H	H	BA,RA	ACTWPB	ILLEGAL 2
	L	L	H	H	L	BA,RA	ACT	ILLEGAL 2
	L	L	H	L	H	X	Undefined	ILLEGAL
	L	L	H	L	L	BA,A8	PRE	ILLEGAL 2
	L	L	L	H	H	X	Undefined	ILLEGAL
	L	L	L	H	L	X	REF	ILLEGAL
	L	L	L	L	H	Op-code	SRS	ILLEGAL
	L	L	L	L	L	Op-code	MRS	ILLEGAL
Precharging	H	X	X	X	X	X	DESEL	NOP=>Idle after tRP
	L	H	H	H	X	X	NOP	NOP=>Idle after tRP
	L	H	H	L	H	X	Undefined	ILLEGAL
	L	H	H	L	L	X	STOP	ILLEGAL 2
	L	H	L	H	H	X	Undefined	ILLEGAL
	L	H	L	H	L	BA,CA,A8	READ/READA	ILLEGAL 2
	L	H	L	L	H	BA,CA,A8	BW/BWA	ILLEGAL 2
	L	H	L	L	L	BA,CA,A8	WRITE/WRITEA	ILLEGAL 2
	L	L	H	H	H	BA,RA	ACTWPB	ILLEGAL 2
	L	L	H	H	L	BA,RA	ACT	ILLEGAL 2
	L	L	H	L	H	X	Undefined	ILLEGAL
	L	L	H	L	L	BA,A8	PRE	NOP 4
	L	L	L	H	H	X	Undefined	ILLEGAL
	L	L	L	H	L	X	REF	ILLEGAL
	L	L	L	L	H	Op-code	SRS	Special Register Access
	L	L	L	L	L	Op-code	MRS	ILLEGAL

SGRAM FUNCTION TRUTH TABLE (continued)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	ADD	COMMAND	ACTION
ROW	H	X	X	X	X	X	DESEL	NOP=> Row Active after tRCD
Activating	L	H	H	H	X	X	NOP	NOP=> Row Active after tRCD
	L	H	H	L	H	X	Undefined	ILLEGAL
	L	H	H	L	L	X	STOP	ILLEGAL 2
	L	H	L	H	H	X	Undefined	ILLEGAL
	L	H	L	H	L	BA,CA,A8	READ/READA	ILLEGAL 2
	L	H	L	L	H	BA,CA,A8	BW/BWA	ILLEGAL 2
	L	H	L	L	L	BA,CA,A8	WRITE/WRITEA	ILLEGAL 2
	L	L	H	H	H	BA,RA	ACTWPB	ILLEGAL 2
	L	L	H	H	L	BA,RA	ACT	ILLEGAL 2
	L	L	H	L	H	X	Undefined	ILLEGAL
	L	L	H	L	L	BA,A8	PRE	ILLEGAL 2
	L	L	L	H	H	X	Undefined	ILLEGAL
	L	L	L	H	L	X	REF	ILLEGAL
	L	L	L	L	H	Op-code	SRS	Special Register Access
	L	L	L	L	L	Op-code	MRS	ILLEGAL
WRITE	H	X	X	X	X	X	DESEL	NOP=>Row Active after write recovering time
Recovering	L	H	H	H	X	X	NOP	NOP=>Row Active after write recovering time
	L	H	H	L	H	X	Undefined	ILLEGAL
	L	H	H	L	L	X	STOP	ILLEGAL 2
	L	H	L	H	H	X	Undefined	ILLEGAL
	L	H	L	H	L	BA,CA,A8	READ/READA	Begin Read; Latch CA; Determine AP
	L	H	L	L	H	BA,CA,A8	BW/BWA	Block Write; Latch CA; Determine AP
	L	H	L	L	L	BA,CA,A8	WRITE/WRITEA	Begin Write; Latch CA; Determine AP
	L	L	H	H	H	BA,RA	ACTWPB	ILLEGAL 2
	L	L	H	H	L	BA,RA	ACT	ILLEGAL 2
	L	L	H	L	H	X	Undefined	ILLEGAL
	L	L	H	L	L	BA,A8	PRE	ILLEGAL 2
	L	L	L	H	H	X	Undefined	ILLEGAL
	L	L	L	H	L	X	REF	ILLEGAL
	L	L	L	L	H	Op-code	SRS	Special Register Access
	L	L	L	L	L	Op-code	MRS	ILLEGAL
Refreshing	H	X	X	X	X	X	DESEL	NOP=> Idle after tRC
	L	H	H	H	X	X	NOP	NOP=> Idle after tRC
	L	H	H	L	H	X	Undefined	ILLEGAL
	L	H	H	L	L	X	STOP	ILLEGAL
	L	H	L	H	H	X	Undefined	ILLEGAL
	L	H	L	H	L	BA,CA,A8	READ/READA	ILLEGAL
	L	H	L	L	H	BA,CA,A8	BW/BWA	ILLEGAL
	L	H	L	L	L	BA,CA,A8	WRITE/WRITEA	ILLEGAL
	L	L	H	H	H	BA,RA	ACTWPB	ILLEGAL
	L	L	H	H	L	BA,RA	ACT	ILLEGAL
	L	L	H	L	H	X	Undefined	ILLEGAL
	L	L	H	L	L	BA,A8	PRE	ILLEGAL
	L	L	L	H	H	X	Undefined	ILLEGAL
	L	L	L	H	L	X	REF	ILLEGAL
	L	L	L	L	H	Op-code	SRS	ILLEGAL
	L	L	L	L	L	Op-code	MRS	ILLEGAL

SGRAM FUNCTION TRUTH TABLE (continued)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	ADD	COMMAND	ACTION
Mode	H	X	X	X	X	X	DESEL	NOP
Register	L	H	H	H	X	X	NOP	NOP
Accessing	L	H	H	L	H	X	Undefined	ILLEGAL
	L	H	H	L	L	X	STOP	ILLEGAL
	L	H	L	H	H	X	Undefined	ILLEGAL
	L	H	L	H	L	BA,CA,A8	READ/READA	ILLEGAL
	L	H	L	L	H	BA,CA,A8	BW/BWA	ILLEGAL
	L	H	L	L	L	BA,CA,A8	WRITE/WRITEA	ILLEGAL
	L	L	H	H	H	BA,RA	ACTWPB	ILLEGAL
	L	L	H	H	L	BA,RA	ACT	ILLEGAL
	L	L	H	L	H	X	Undefined	ILLEGAL
	L	L	H	L	L	BA,A8	PRE	ILLEGAL
	L	L	L	H	H	X	Undefined	ILLEGAL
	L	L	L	H	L	X	REF	ILLEGAL
	L	L	L	L	H	Op-code	SRS	ILLEGAL
	L	L	L	L	L	Op-code	MRS	ILLEGAL

ABBREVIATIONS:
BA = Bank Address, RA = Row Address, CA = Column Address
Term = Terminate
AP = Auto Precharge
NOP = No Operation
ILLEGAL = Device operation and/or data-integrity are not guaranteed.

NOTES:
1. All entries assume that CKE was active(HIGH) during the preceding clock cycle and the current clock cycle.
2. Illegal to bank in specified state; function may be legal in the bank indicated by BA, depending on the state of that bank.
3. Must satisfy the "2n-rule", bus contention, bus turn around, and/or write recovery requirements.
4. NOP to bank precharging or in idle state. May precharge bank(s) indicated by BA(and A8).
5.Illegal if any bank is not idle.
6. Legal only if all banks are in idle or row active state.

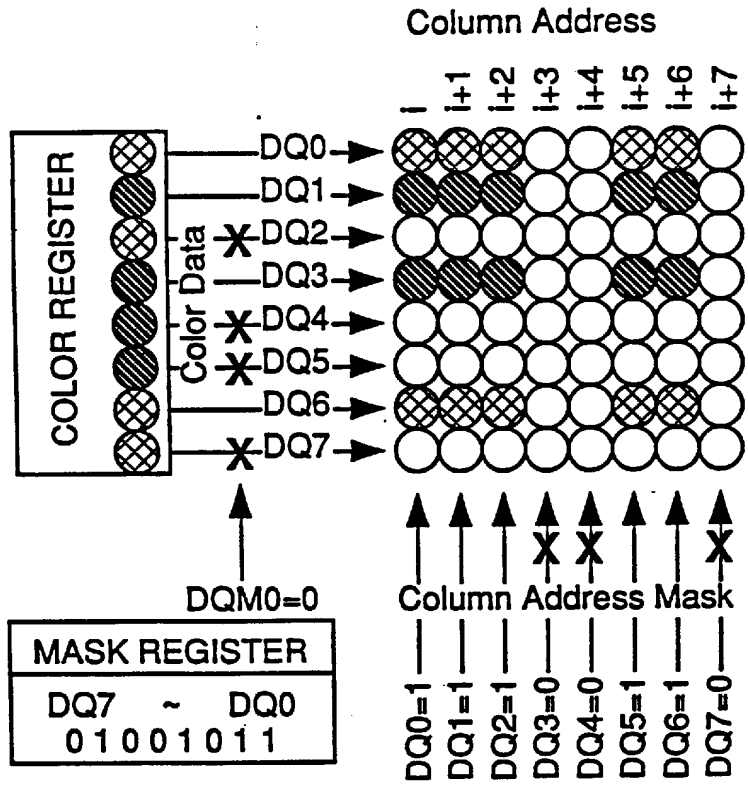
SGRAM FUNCTION TRUTH TABLE FOR CKE

Current State	CKE n-1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	ADD	ACTION
SELF	H	X	X	X	X	X	X	X	INVALID, CLK(n-1)would exit Self Refresh
REFRESH	L	H	H	X	X	X	X	X	Self Refresh Recovery 2
	L	H	L	H	H	X	X	X	Self Refresh Recovery 2
	L	H	L	H	L	X	X	X	ILLEGAL 2
	L	H	L	L	X	X	X	X	ILLEGAL 2
	L	L	X	X	X	X	X	X	Maintain S.R.
SELF	H	H	H	X	X	X	X	X	IDLE after tRC
REFRESH	H	H	L	H	H	H	L	X	IDLE after tRC
Recovery	H	H	L	H	H	H	H	X	ILLEGAL
	H	H	L	H	H	L	X	X	ILLEGAL
	H	H	L	H	L	X	X	X	ILLEGAL
	H	H	L	L	X	X	X	X	ILLEGAL
	H	L	X	X	X	X	X	X	Begin Clock Suspend next cycle 5
	L	H	X	X	X	X	X	X	Exit Clock Suspend next cycle 2
	L	L	X	X	X	X	X	X	Maintain Clock Suspend
Power	H	X	X	X	X	X	X	X	INVALID, CLK(n-1) would exit Power Down
Down	L	H	X	X	X	X	X	X	Exit Power Down -> IDLE 2
	L	L	X	X	X	X	X	X	Maintain Power Down Mode
Both	H	H	H	X	X	X	X	X	Refer to Operations in the Turth Table
Banks	H	H	L	H	X	X	X	X	Refer to Operations in the Turth Table
IDLE	H	H	L	L	H	X	X	X	Refer to Operations in the Turth Table
	H	H	L	L	L	H	H	X	Refer to Operations in the Turth Table
	H	H	L	L	L	H	L	X	Refresh
	H	H	L	L	L	L	X	Op-Code	Refer to Operations in the Turth Table
	H	L	H	X	X	X	X	X	Refer to Operations in the Turth Table
	H	L	L	H	X	X	X	X	Refer to Operations in the Turth Table
	H	L	L	L	H	X	X	X	Refer to Operations in the Turth Table
	H	L	L	L	L	H	H	X	Refer to Operations in the Turth Table
	H	L	L	L	L	H	L	X	Self Refresh 3
	H	L	L	L	L	L	X	Op-Code	Refer to Operations in the Turth Table
	L	X	X	X	X	X	X	X	INVALID, CLK(n-1) would enter Clock Suspend or Power Down
Any State	H	H	X	X	X	X	X	X	Refer to Operations in the Turth Table
other than	H	L	X	X	X	X	X	X	Begin Clock Suspend next cycle. 4
listed	L	H	X	X	X	X	X	X	Exit Clock Suspend next cycle
above.	L	L	X	X	X	X	X	X	Maintain Clock Suspend.

Notes

1. H: High level, L: Low level, X: High or low level(Don't care)
2. CKE Low to High transition will re-enable CLK and other inputs asynchronously. A minimum setup time must be satisfied before any command other than EXIT.
3. Power Down and Self Refresh can be entered only from then Both Banks IDLE State.
4. Must be legal command as defined in Operative command table 1.
5 Illegal if tSREX is not satisfied.

Block Write Function



Write Data

Mask Write, keep original Data

* This diagram show only for DQ0-7. The other DQ is similar as this.

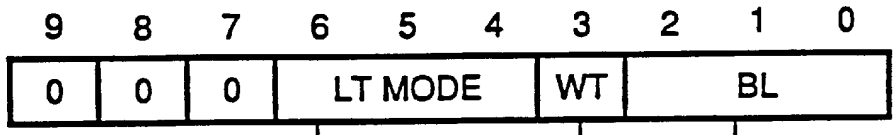
Column Mask

DQ0-7 : Column Mask for DQ0-7
DQ8-15 : Column Mask for DQ8-15
DQ16-23 : Column Mask for DQ16-23
DQ24-31 : Column Mask for DQ24-31

Write per bit

Mask data = Mask Register + DQMi
DQMi is prior than data of Mask Register.

Mode Register

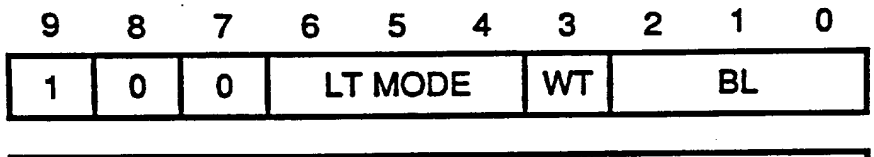


	Bit 2~0	Burst Length WT=0	Burst Length WT=1
Burst Length	000	1	R*
	001	2	R*
	010	4	4
	011	8	8
	100	R*	R*
	101	R*	R*
	110	R*	R*
	111	Full Page	R*

Wrap Type	0	Sequential
	1	Interleave

	Bit 6~4	CAS Latency
Latency Mode	000	R*
	001	1
	010	2
	011	3
	1xx	R*

(R* : Reserved)



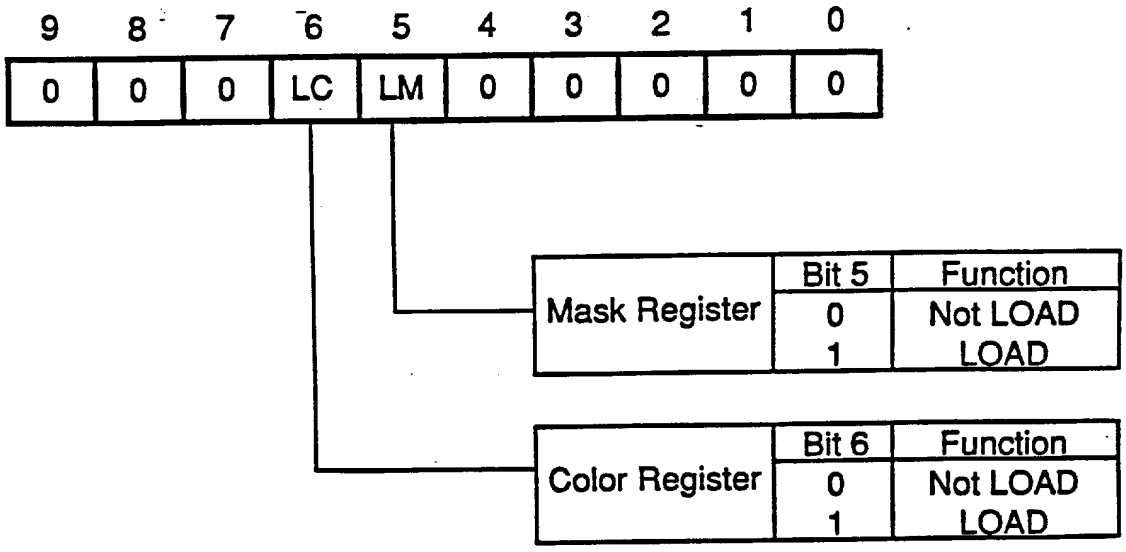
Burst Read and Single Write (for write through cache)

JEDEC Standard Test Set (Refresh counter test)

Vender Specific

V=Valid
X=Don't care

Special Register



Note : If LC and LM are both high (1), data of Mask and Color register will be unknown.

Auto precharge

During a read or write command cycle, A8 controls whether auto precharge is selected. A8 high in the read or write command (Read with Auto precharge command or Write with Auto precharge command), auto precharge is selected and begins after the burst access automatically.

In write cycle, the t_{DAL} must be satisfied to assert the next activate command to the bank begin precharged. And it is not necessary to know when the precharge starts.

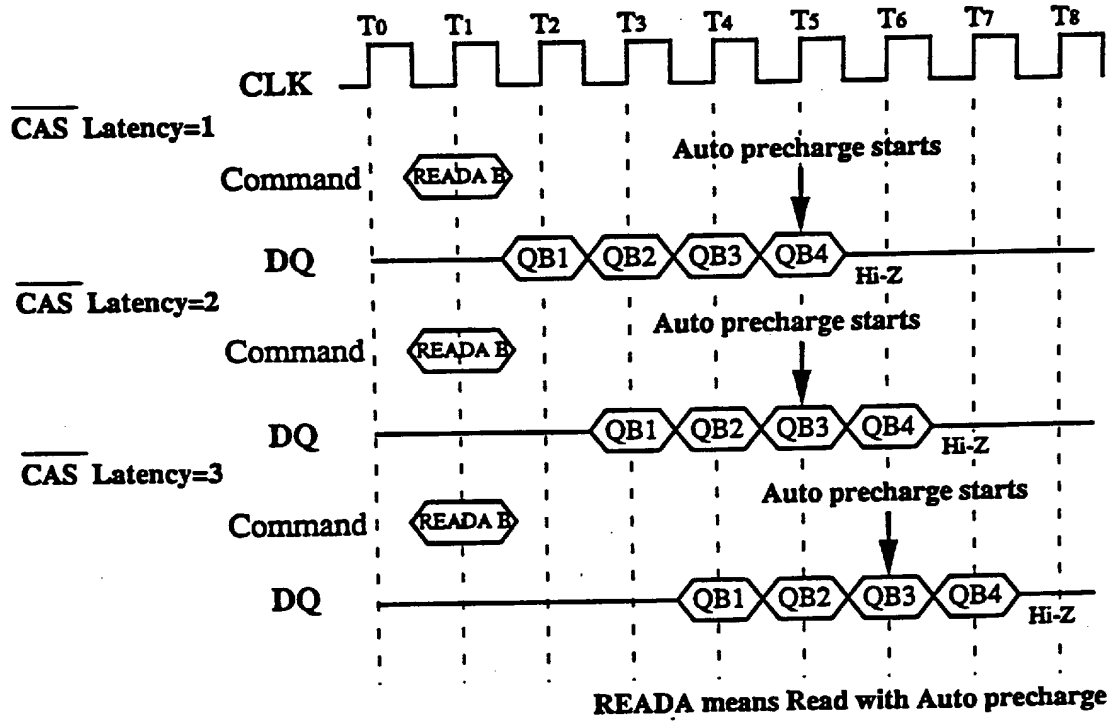
When using auto precharge in read cycle, knowing when the precharge starts is important because the next activate command to the bank being precharge can not be executed until the precharge cycle ends. Once auto precharge has started, an activate command to the bank can be asserted after t_{RP} has been satisfied.

The clock that begins the auto precharge cycle is depend on both the $\overline{CAS}$ latency programmed into the mode register and whether READ or WRITE cycle.

READ with Auto precharge

During READ cycle, the auto precharge begins on the clock that indicated the last data word output during the burst is valid ($\overline{CAS}$ latency of 1) or one clock earlier ($\overline{CAS}$ latency of 2 or 3).

Burst Length = 4



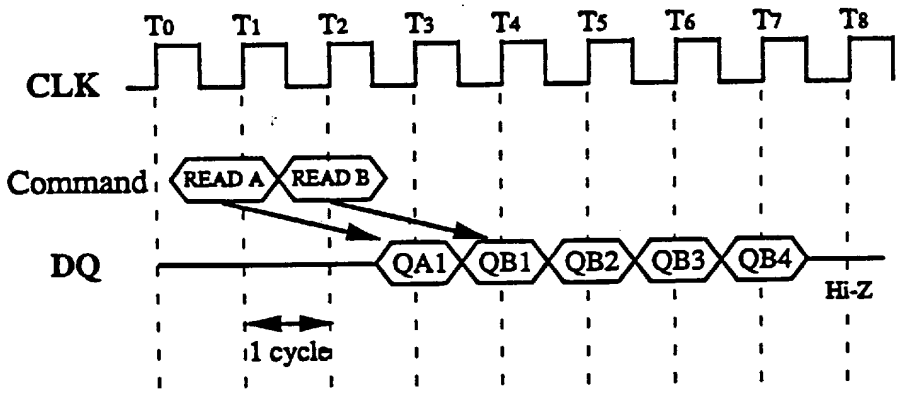
READ / WRITE Command Interval

Read to Read Command Interval

During READ cycle, when new Read command is asserted, it will be effective after $\overline{CAS}$ Latency, even if the previous READ operation does not completed. READ will be interrupted by another READ.

The interval between the commands is minimum 1 cycle. Each Read command can be asserted in every clock without any restriction.

Burst Length = 4, $\overline{CAS}$ Latency=2

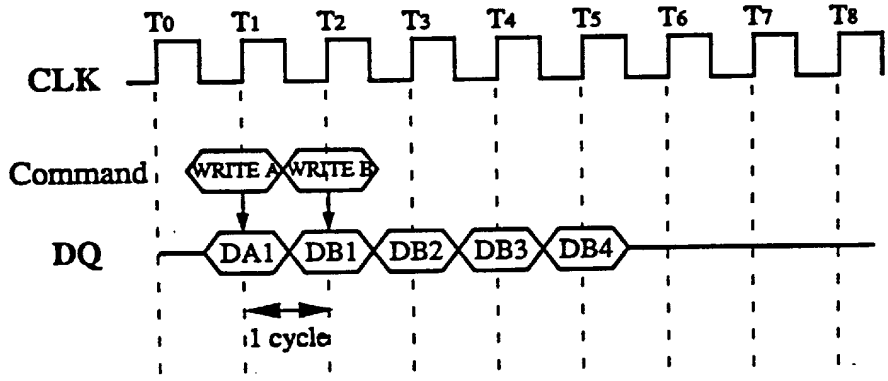


Write to Write Command Interval

During WRITE cycle, when new Write command is asserted, the previous burst will terminate and the new burst will begin with at new Write command. WRITE will be interrupted by another WRITE.

The interval between the commands is minimum 1. Each Write command can be asserted in every clock without any restriction.

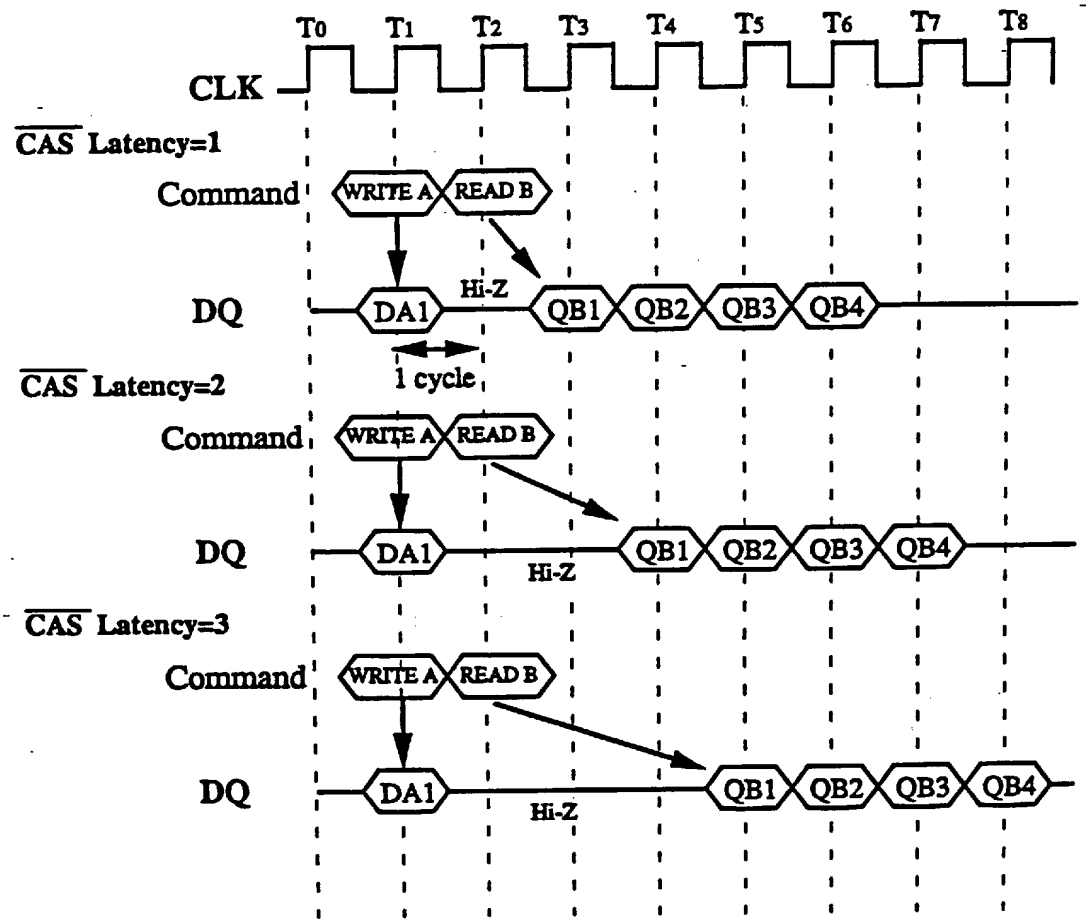
Burst Length = 4, $\overline{CAS}$ Latency=2



Write to Read Command Interval

Write command and Read command interval is also 1 cycle.
Only the write data before Read command will be written.
The data bus must be Hi-Z at least one cycle prior to the first Dout.

Burst Length = 4



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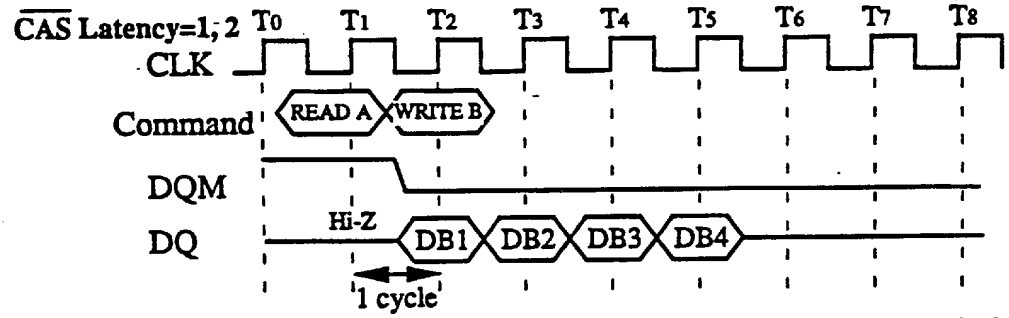
Read to Write Command Interval

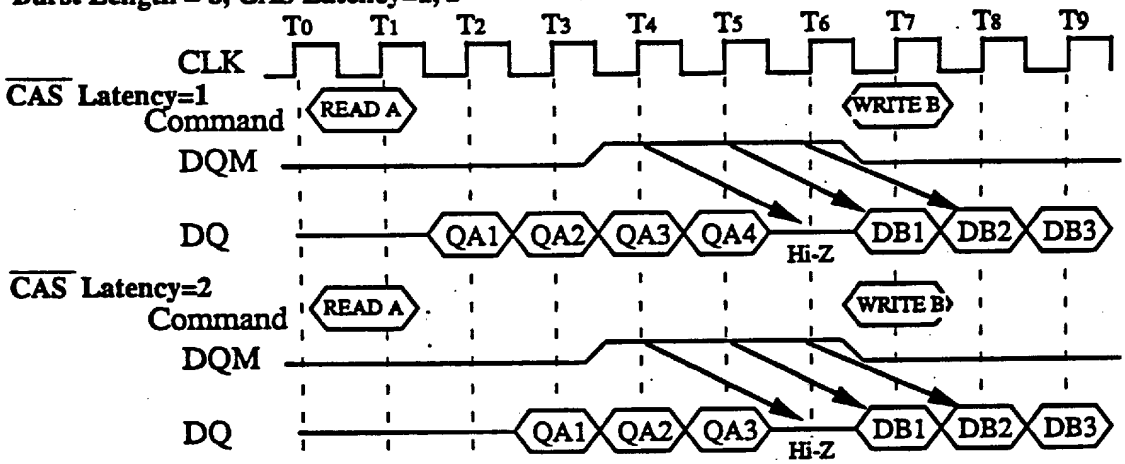
During READ cycle, Read can be interrupted by WRITE. When $\overline{\text{CAS}}$ Latency of 3 and the burst length is Full page, the burst read can not be interrupted by WRITE. Burst read can be interrupted by Burst Stop command (STOP) or Precharge command for $\overline{\text{CAS}}$ latency of 3.

For $\overline{\text{CAS}}$ latency of 1 or 2, the Read and Write command interval is minimum 1 cycle. There is a restriction to avoid data conflict. The data bus must be Hi-Z using DQM before WRITE.



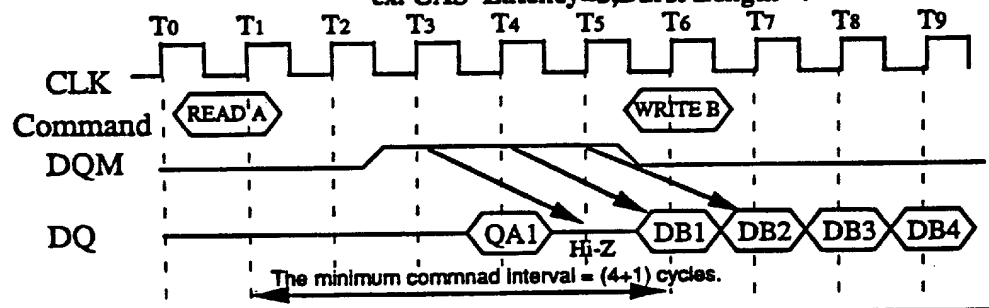
In case $\overline{\text{CAS}}$ latency is 1 or 2, READ can be interrupted by WRITE. DQM must be kept being High from at least 3 clocks to 1 clock before the Write command.

Burst Length = 8, $\overline{\text{CAS}}$ Latency=1, 2



In case CAS latency is 3 (burst length is not Full page), READ can be interrupted by WRITE. The minimum command interval is [burst length + 1] cycles. DQM must be High at least 3 clocks prior to to the Write command.

ex. $\overline{\text{CAS}}$ Latency=3,Burst Length=4



Burst Length and Sequence

Burst of Two

Starting Address (Column address A0)	Sequential Addressing Sequence (decimal)	Interleave Addressing Sequence (decimal)
0	0,1	0,1
1	1,0	1,0

Burst of Four

Starting Address (Column address A1-A0)	Sequential Addressing Sequence (decimal)	Interleave Addressing Sequence (decimal)
0 (00B)	0,1,2,3	0,1,2,3
1 (01B)	1,2,3,0	1,0,3,2
2 (10B)	2,3,0,1	2,3,0,1
3 (11B)	3,0,1,2	3,2,1,0

Burst of Eight

Starting Address (Column address A2-A0)	Sequential Addressing Sequence (decimal)	Interleave Addressing Sequence (decimal)
0 (000B)	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
1 (001B)	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
2 (010B)	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
3 (011B)	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4
4 (100B)	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
5 (101B)	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
6 (110B)	6, 7, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1
7 (111B)	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0

Full page Burst

Full page burst is an extension of the above tables of Sequential Addressing with the length being 256.

Electrical Specifications

ABSOLUTE MAXIMUM RATINGS

Voltage on Power Supply Pin Relative to GND	-1.0 to +4.6	V
Voltage on Input Pin Relative to GND	-1.0 to +4.6	V
Short Circuit Output Current	50	mA
Power Dissipation	1	W
Operating Temperature	0 to +70	°C
Storage Temperature	-55 to +125	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	Vcc	3.0	3.3	3.6	V
High Level Input Voltage	VIH	2.0		Vcc+0.3	V
Low Level Input Voltage	VIL	-0.3		0.8	V
Ambient Temperature	Ta	0		70	°C

DC CHARACTERISTICS (Recommended Operating unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION			MAX.	UNIT	NOTE
Operating Current	Icc1	Burst length=1 tRAS≥tRAS(MIN) tRP≥tRP(MIN) Io=0mA		-10 -12 -13	TBD	mA	3
Precharge Standby Current in Power Down mode	Icc2P	CKE≤VIL(MAX) tCK=15ns			TBD	mA	
	Icc2PS	CKE≤VIL(MAX) tCK=∞			TBD	mA	
Precharge Standby Current in Non Power Down mode	Icc2N	CKE≥VIH(MIN) tCK=15ns Input signals are changed one time during 30ns.			TBD	mA	
	Icc2NS	CKE≥VIH(MIN) tCK=∞ Input signals are stable.			TBD	mA	
Active Standby Current in Power Down mode	Icc3P	CKE≤VIL(MAX) tCK=15ns			TBD	mA	
	Icc3PS	CKE≤VIL(MAX) tCK=∞			TBD	mA	
Active Standby Current in Non Power Down mode	Icc3N	CKE≥VIH(MIN) tCK=15ns Input signals are changed one time during 30ns.			TBD	mA	
	Icc3NS	CKE≥VIH(MIN) tCK=∞ Input signals are stable.			TBD	mA	
Operating Current (Burst Mode)	Icc4	tCK≥tCK(MIN) Io=0mA	CAS Latency=3	-10 -12 -13	TBD TBD TBD	mA	3
			CAS Latency=2	-10 -12 -13	TBD TBD TBD	mA	3
			CAS Latency=1	-10 -12 -13	TBD TBD TBD	mA	3
Refresh Current	Icc5	tRC≥tRC(MIN)		-10 -12 -13	TBD TBD TBD	mA	
Self Refresh Current	Icc6	CKE≤0.2V			TBD	mA	
Operating Current (Block Write Mode)	Icc7	tCK≥tCK(MIN) Io=0mA	CAS cycle = 20ns		TBD	mA	

SYNCHRONOUS CHARACTERISTICS (Recommended Operating unless otherwise noted)

PARAMETER		SYMBOL	-10 MIN.	-10 MAX.	-12 MIN.	-12 MAX.	-13 MIN.	-13 MAX.	UNIT	NOTE
Clock Cycle Time	CAS Latency=3	tCK3	10		12		13		ns	
	CAS Latency=2	tCK2	15		18		19.5		ns	
	CAS Latency=1	tCK1	30		36		39		ns	
Access Time from CLK	CAS Latency=3	tAC3		9		11		12	ns	30pF
	CAS Latency=2	tAC2		12		15		16.5	ns	30pF
	CAS Latency=1	tAC1		27		33		36	ns	30pF
CLK High Level Width		tCH	3.5		4		5		ns	
CLK Low Level Width		tCL	3.5		4		5		ns	
Data-out Hold Time		tOH	4		4		4		ns	
Data-out Low Impedance Time		tLZ	0		0		0		ns	
Data-out High Impedance Time		tHZ		10		10		10	ns	
Data-in Set-up Time		tDS	3		3.5		3.5		ns	
Data-in Hold Time		tDH	1		1.5		1.5		ns	
Address Set-up Time		tAS	3		3.5		3.5		ns	
Address Hold Time		tAH	1		1.5		1.5		ns	
CKE Set-up Time		tCKS	3		3.5		3.5		ns	
CKE Hold Time		tCKH	1		1.5		1.5		ns	
Command ($\overline{CS}$,$\overline{RAS}$,$\overline{CAS}$,$\overline{WE}$,DSF,DQM) Set-up Time		tCMS	3		3.5		3.5		ns	
Command ($\overline{CS}$,$\overline{RAS}$,$\overline{CAS}$,$\overline{WE}$,DSF,DQM) Hold Time		tCMH	1		1.5		1.5		ns	

ASYNCHRONOUS CHARACTERISTICS (Recommend Operating unless otherwise noted)

PARAMETER		SYMBOL	-10 MIN.	-10 MAX.	-12 MIN.	-12 MAX.	-13 MIN.	-13 MAX.	UNIT	NOTE
REF to REF/ACTIVE Command Period		tRC	100		120		130		ns	
ACTIVE to PRE Command Period		tRAS	70	120,000	84	120,000	91	120,000	ns	
PRE to ACTIVE Command Period		tRP	30		36		39		ns	
Delay Time ACTIVE to READ/WRITE Command		tRCD	30		36		39		ns	
ACTIVE(0) to ACTIVE(1) Command Period		tRRD	30		36		39		ns	
Data-in to PRE Command Period	CAS Latency=3	tDPL3	1CLK+10		1CLK+12		1CLK+13		ns	
	CAS Latency=2	tDPL2	15		18		19.5		ns	
	CAS Latency=1	tDPL1	15		18		19.5		ns	
Data-in to ACTIVE(REF) Command Period (Auto Precharge)	CAS Latency=3	tDAL3	2CLK+30		2CLK+36		2CLK+39		ns	
	CAS Latency=2	tDAL2	1CLK+30		1CLK+36		1CLK+39		ns	
	CAS Latency=1	tDAL1	1CLK+30		1CLK+36		1CLK+39		ns	
Block Write Cycle Time		tBWC	20		24		26		ns	
Block Write Data-in to PRE Command Period	CAS Latency=3	tBPL3	1CLK+20		1CLK+24		1CLK+26		ns	
	CAS Latency=2	tBPL2	30		36		39		ns	
	CAS Latency=1	tBPL1	30		36		39		ns	
Block Write Data-in to ACTIVE(REF) Command Period (Auto Precharge)	CAS Latency=3	tBAL3	2CLK+40		2CLK+48		2CLK+52		ns	
	CAS Latency=2	tBAL2	1CLK+40		1CLK+48		1CLK+52		ns	
	CAS Latency=1	tBAL1	1CLK+40		1CLK+48		1CLK+52		ns	
Self-Refresh Exit Time		tSREX	20		24		26		ns	
Transition Time		tT	1	30	1	30	1	30	ns	
Refresh Period		tREF		16		16		16	ms	1024 rows

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DC CHARACTERISTICS (Recommended Operating Conditions unless otherwise noted)

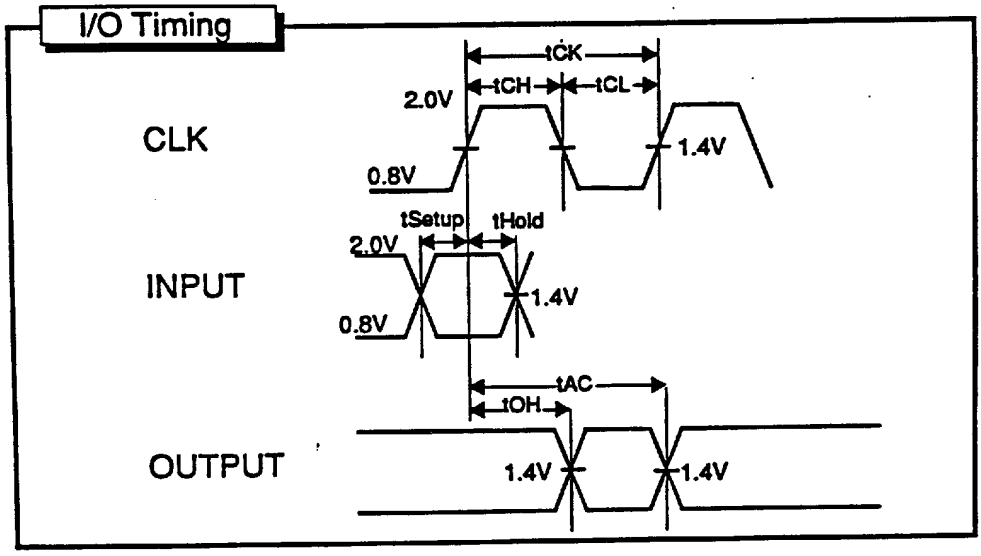
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	NOTE
Input Leakage Current	Ii (L)	VI=0 to 3.6V, all other pins no under test=0V	-1.0		1.0	μA	
Output Leakage Current	Io (L)	Dout is disabled, Vo=0 to 3.6V	-1.0		1.0	μA	
Output High Voltage	VOH	Io= -2mA	2.4			V	
Output Low Voltage	VOL	Io= +2mA			0.4	V	

CAPACITANCE (Ta=25°C,f=1MHz)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	TEST CONDITION
Input Capacitance	CI1	2	4	pF	A0 to A9
	CI2	2	4	pF	CLK,CKE,$\overline{CS}$,$\overline{RAS}$,$\overline{CAS}$,$\overline{WE}$,DSF,DQM
Data Input/Output Capacitance	CI0	2	5	pF	DQ0 to DQ31

NOTES

(1) All Voltages referenced Vss(GND).
(2) an initial pause of 100μs is required after power-on followed by ***Power On Sequence & Auto Refresh*** before proper device operation is achieved.
(3) Icc1 depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, Icc1 is measured on condition that addresses are changed only one time during tCK(MIN).
(4) AC measurements assume tT=1ns.
(5) Reference level for measuring timing of input signals is 1.40V.
(6) An access time is measured at 1.40V.



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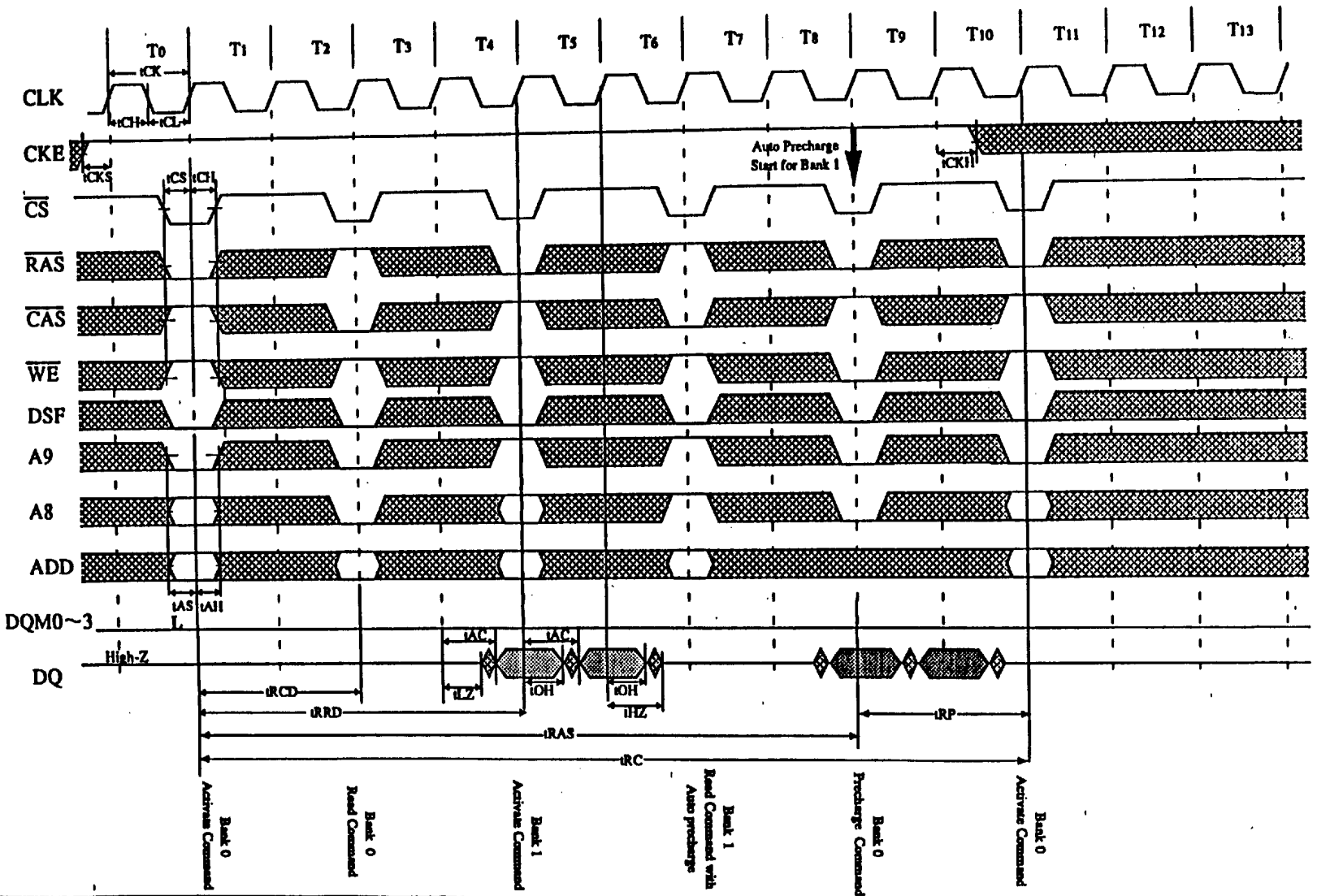
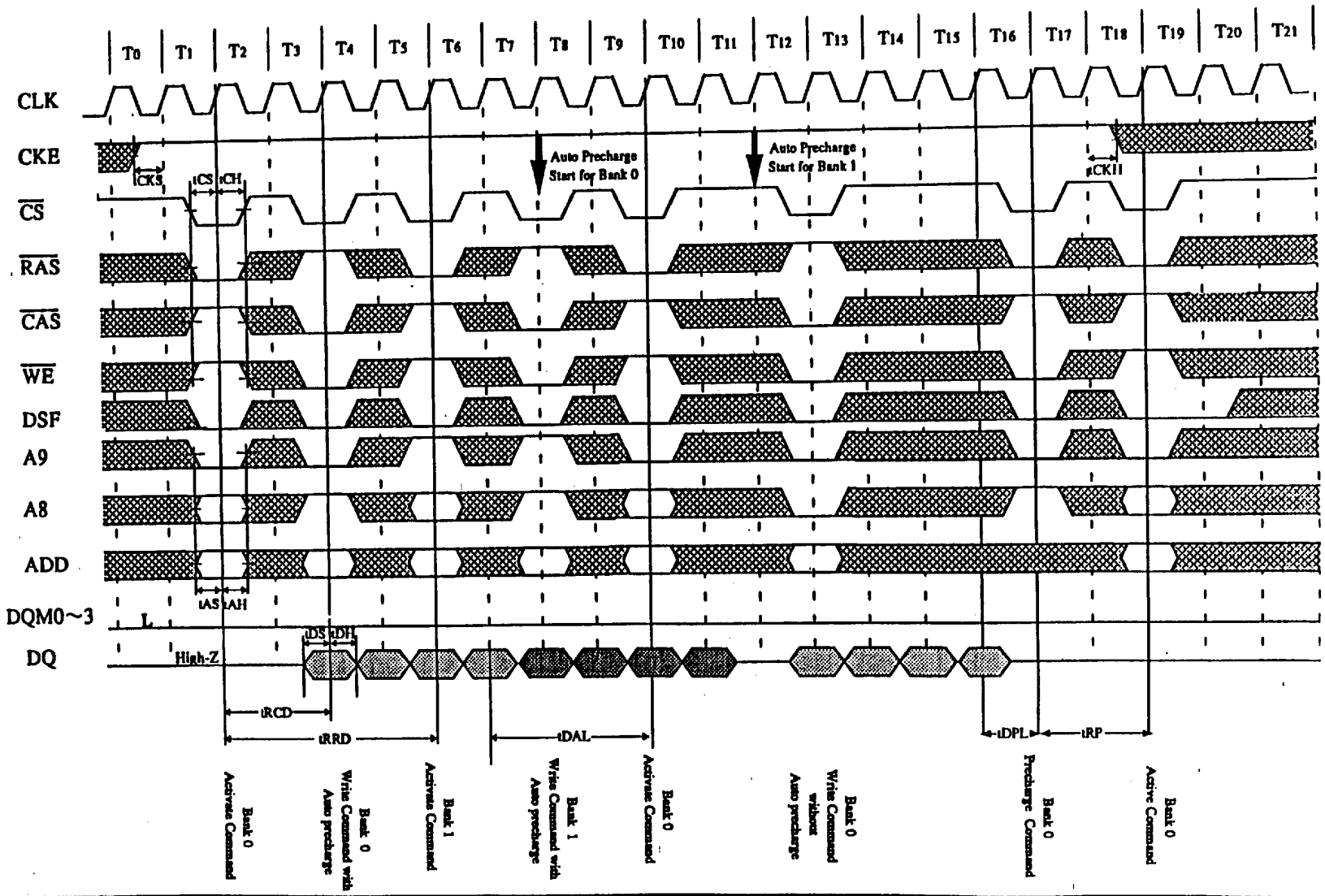
AC Parameters for Read Timing

Burst Length = 2 CAS Latency = 2



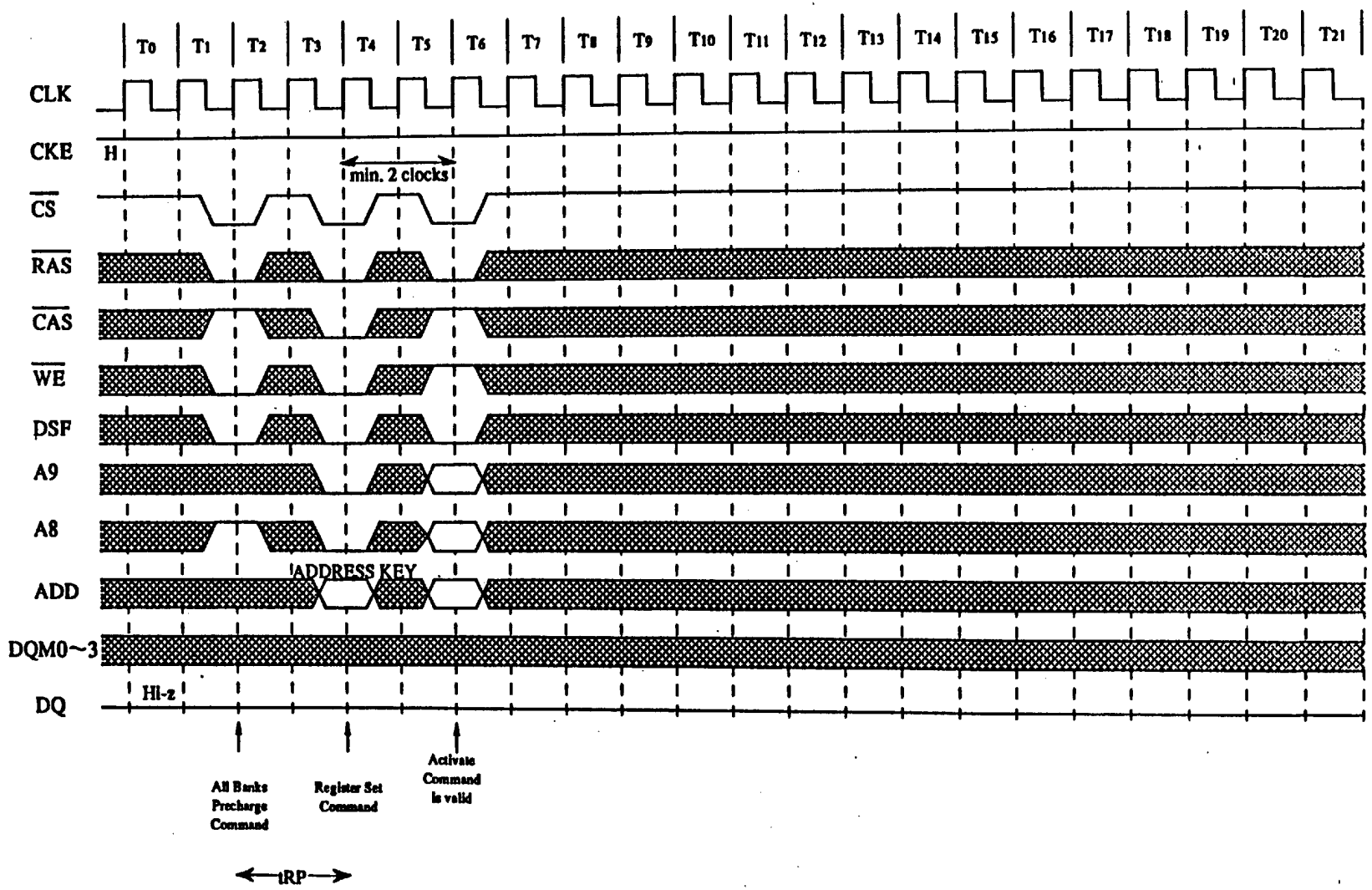
AC Parameters for Write Timing

Burst Length = 4 CAS Latency = 2

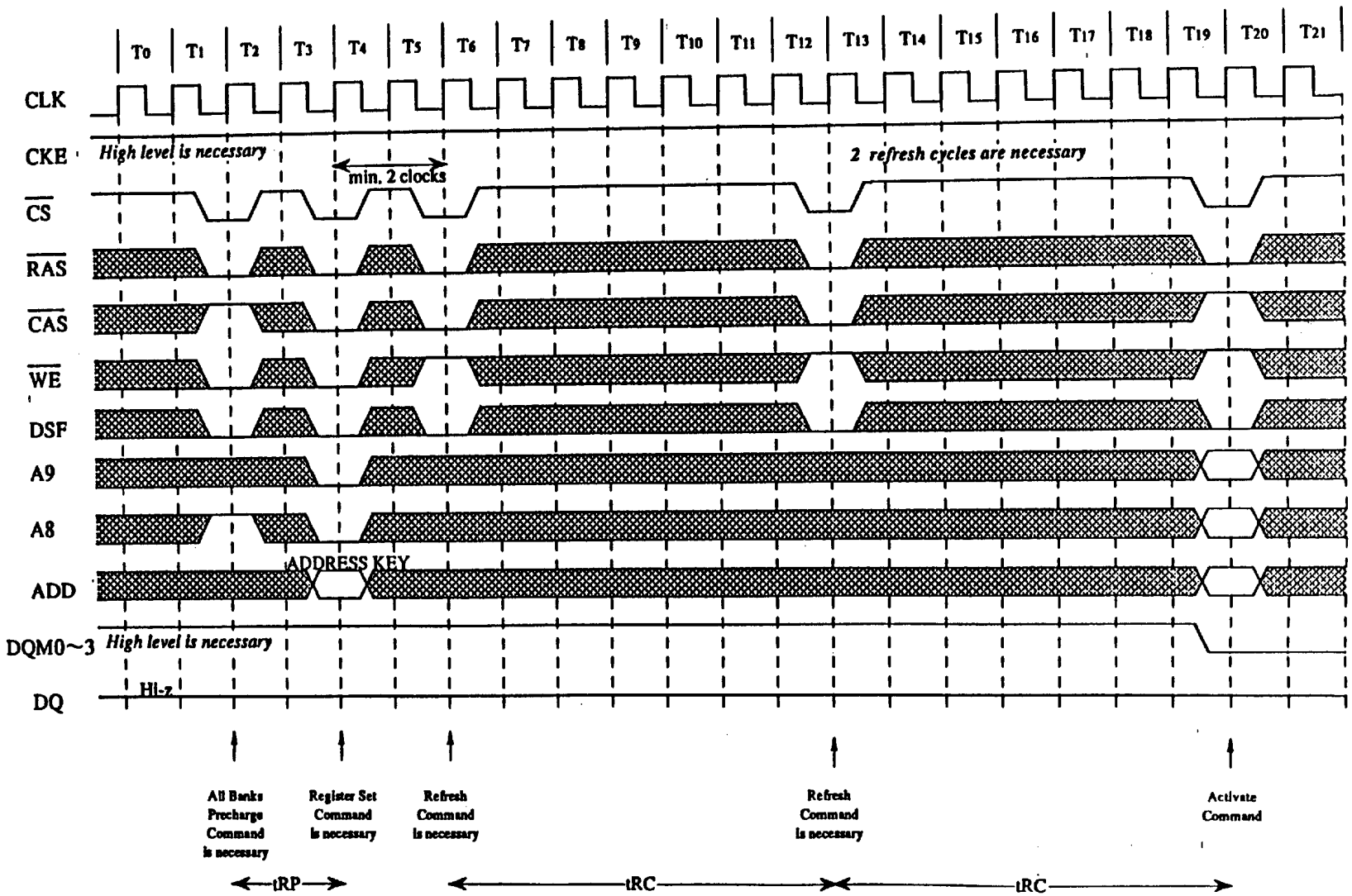


Mode Register Set

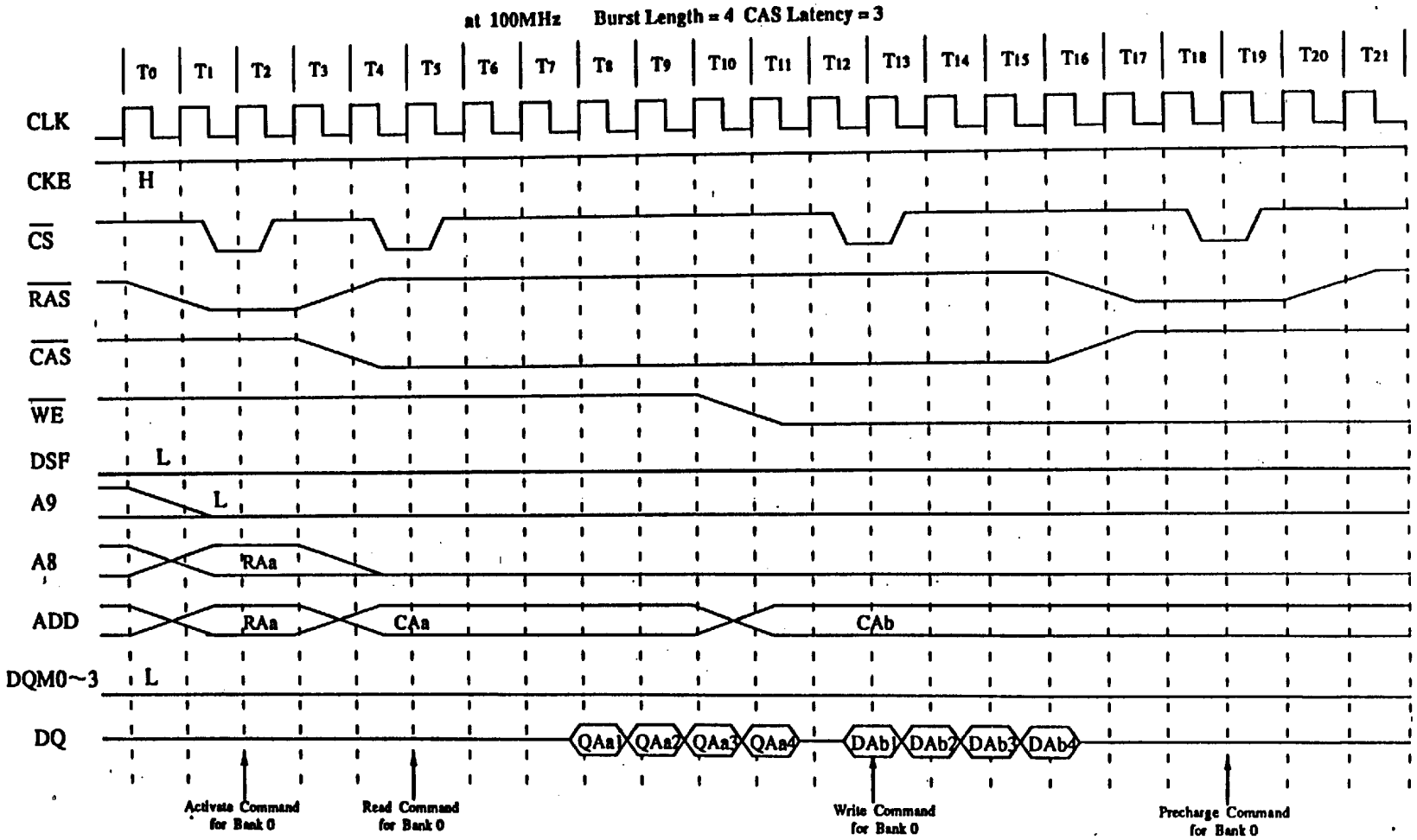
Burst Length = 4 CAS Latency = 2



Power On Sequence & Auto Refresh

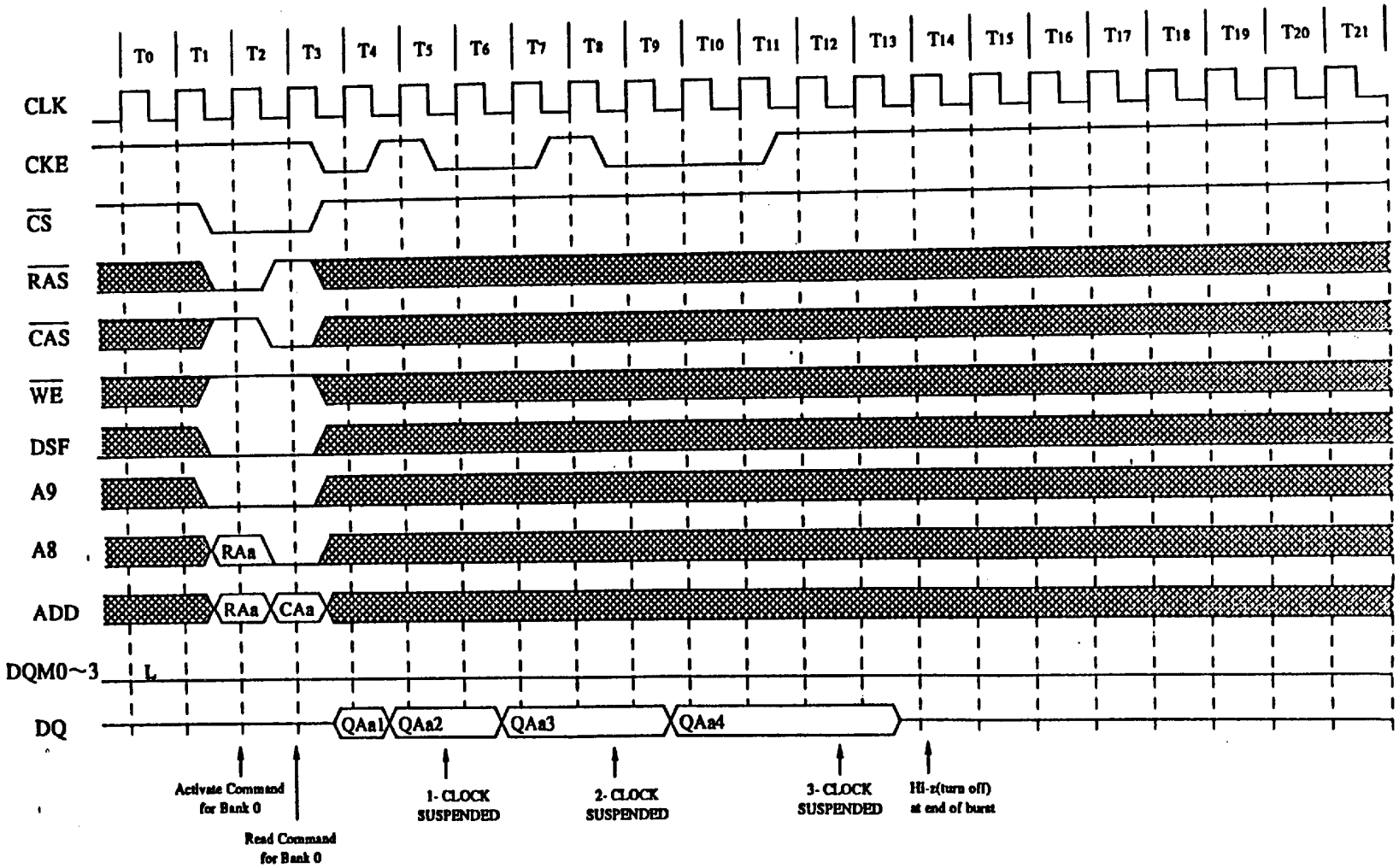


$\overline{CS}$ Function — Only $\overline{CS}$ signal needs to be asserted at minimum rate.



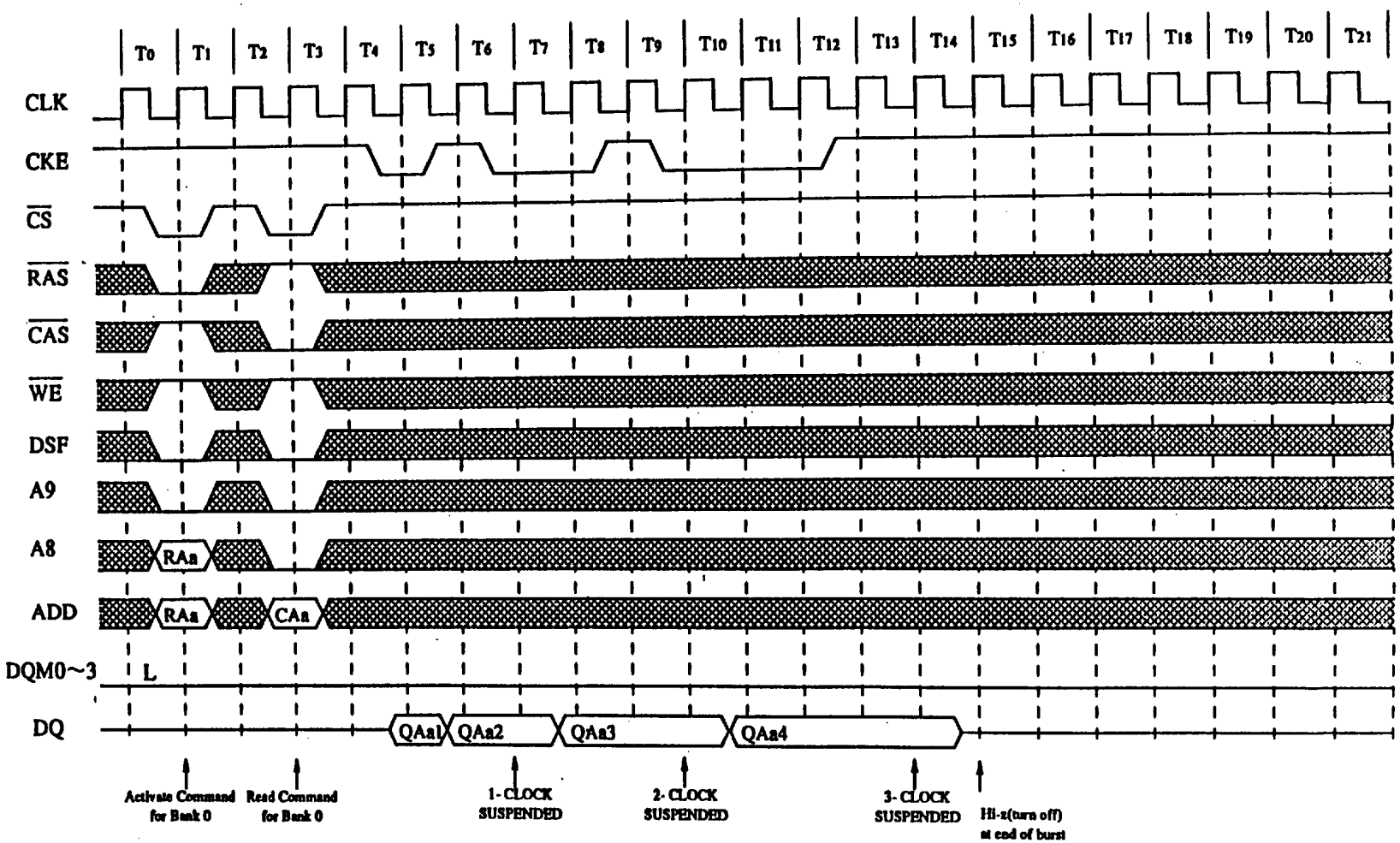
CLOCK SUSPENSION during BURST READ (using CKE Function)

Burst Length = 4 CAS Latency = 1



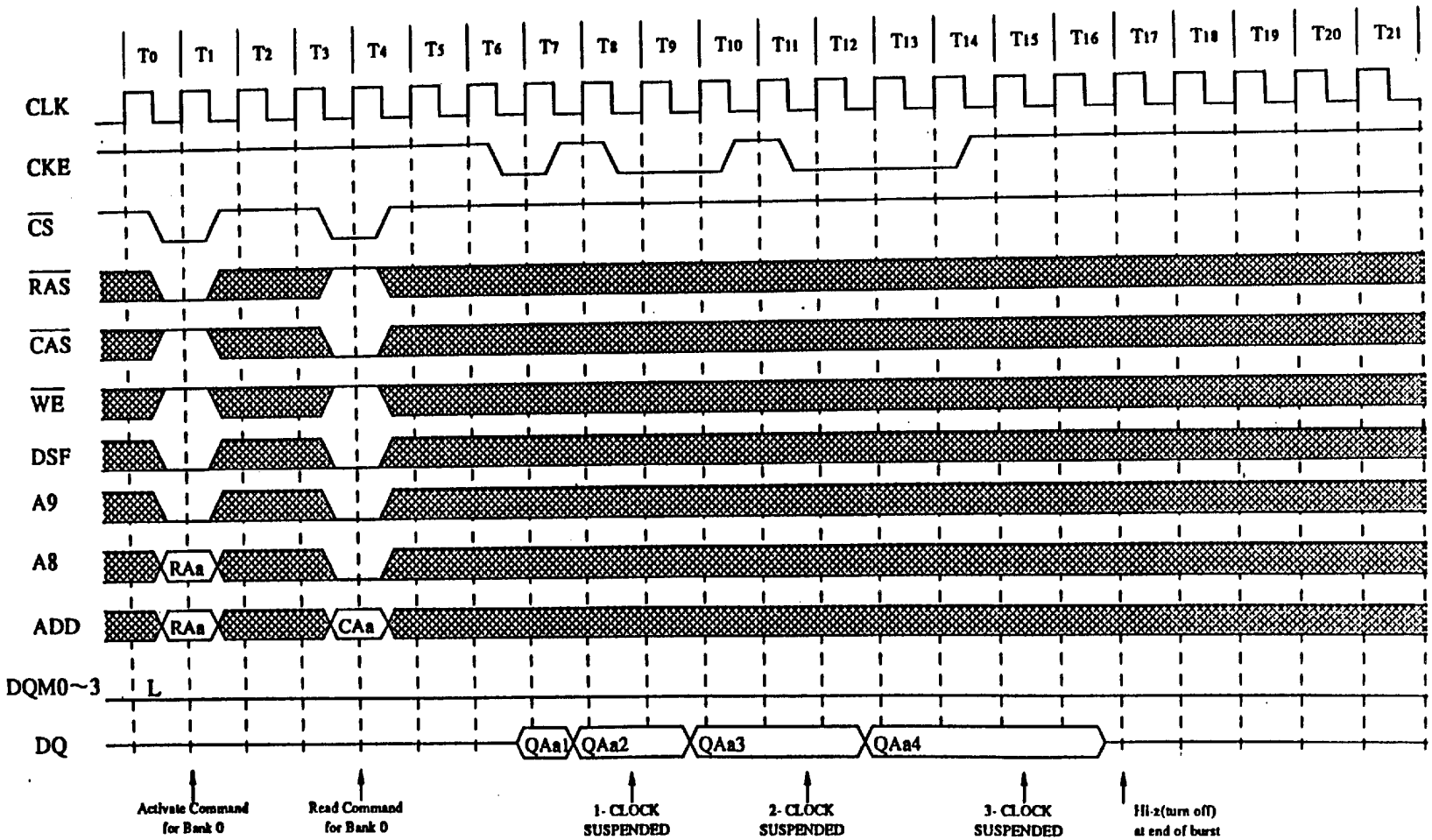
CLOCK SUSPENSION during BURST READ (using CKE Function)

Burst Length = 4 CAS Latency = 2



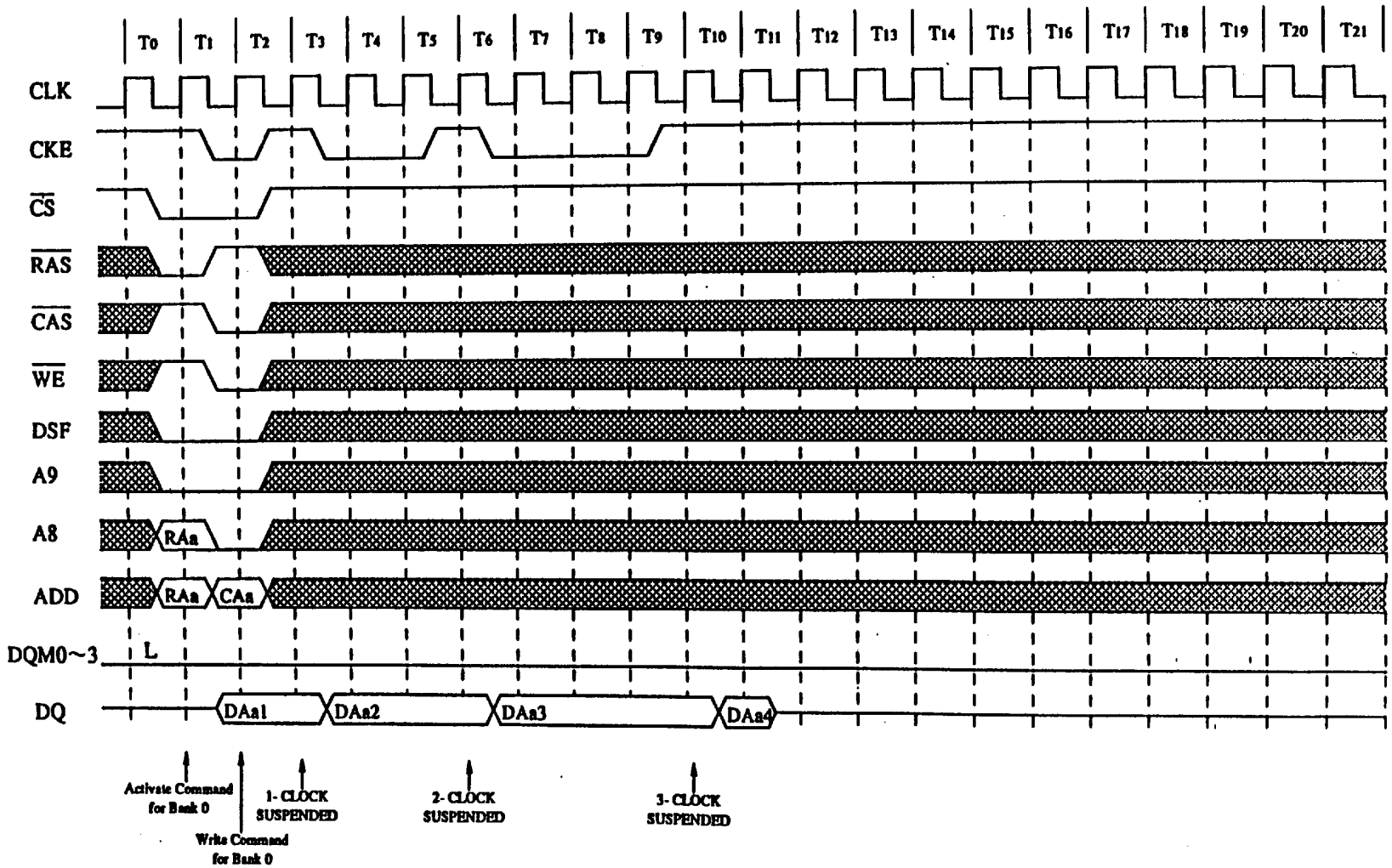
CLOCK SUSPENSION during BURST READ (using CKE Function)

Burst Length = 4 CAS Latency = 3



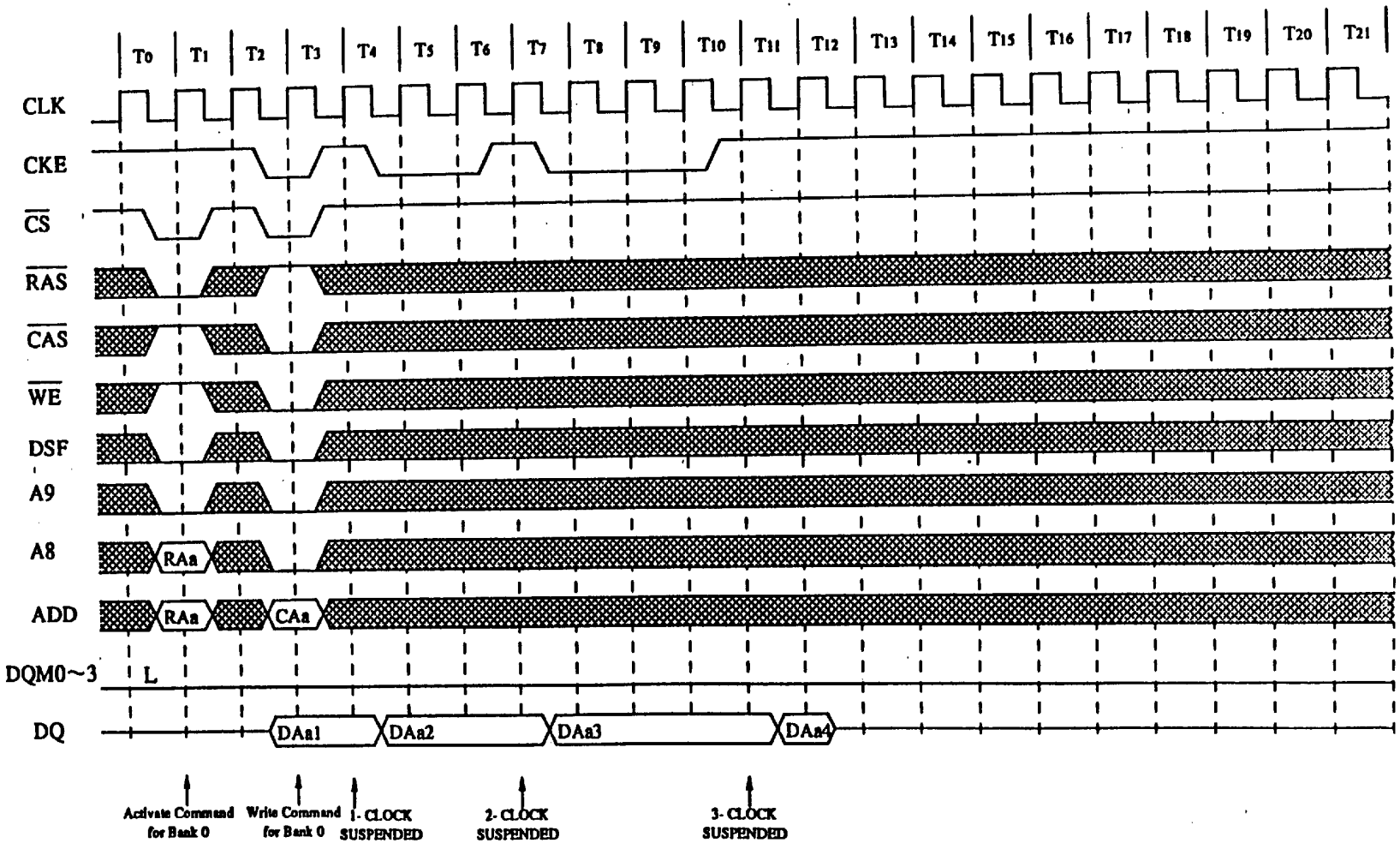
CLOCK SUSPENSION during BURST WRITE (using CKE Function)

Burst Length = 4 CAS Latency = 1

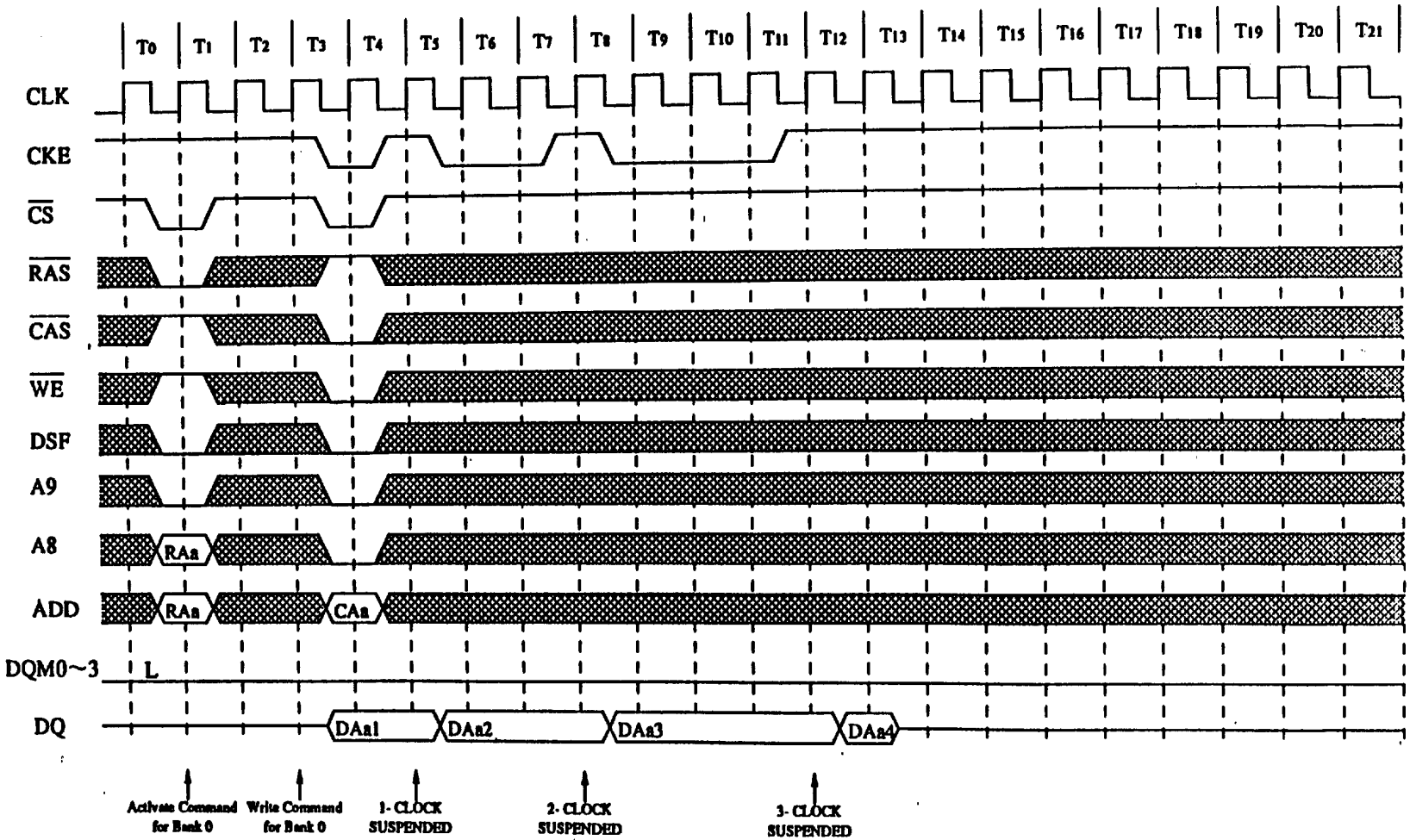


CLOCK SUSPENSION during BURST WRITE (using CKE Function)

Burst Length = 4 CAS Latency = 2

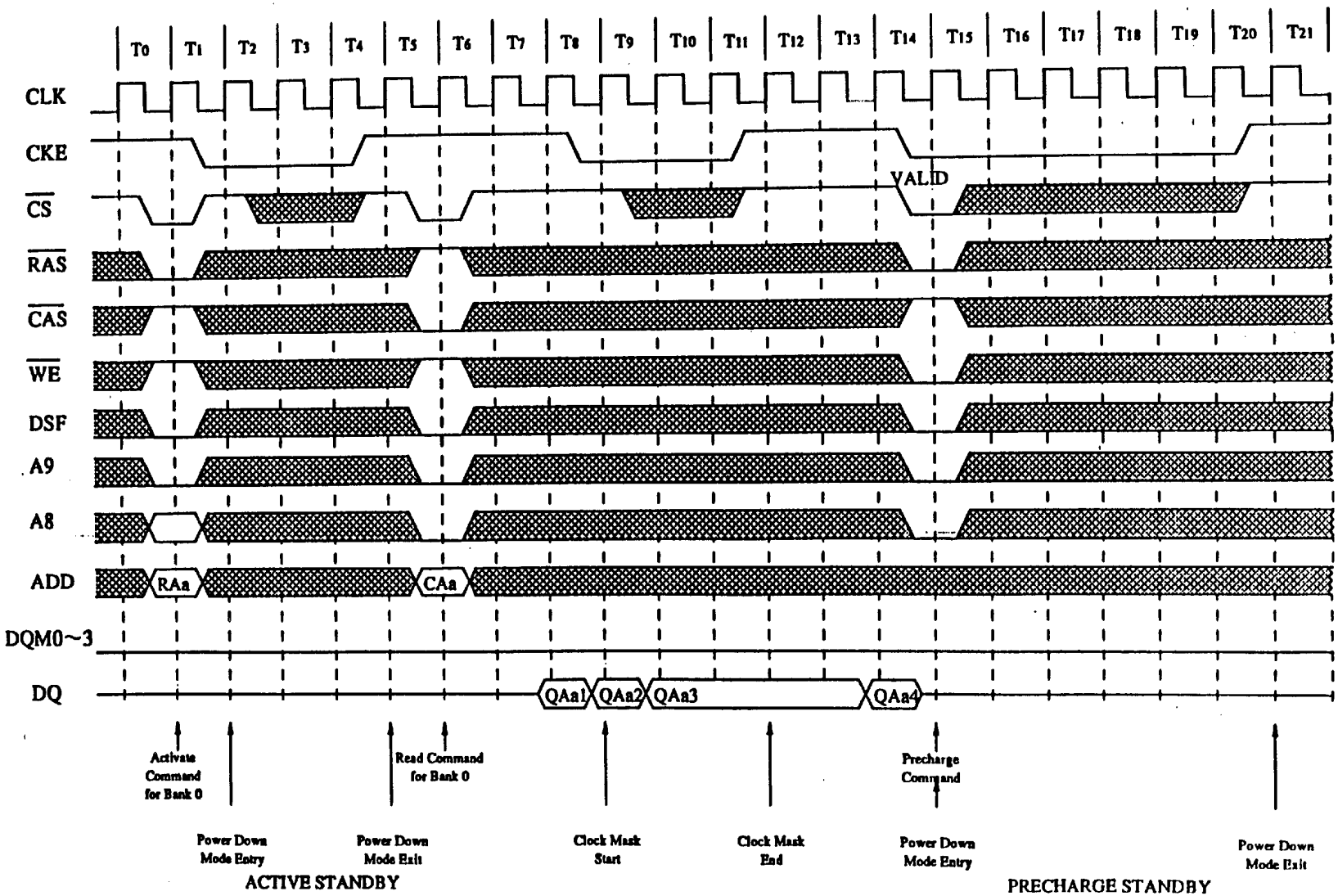


CLOCK SUSPENSION during BURST WRITE (using CKE Function) Burst Length = 4 CAS Latency = 3



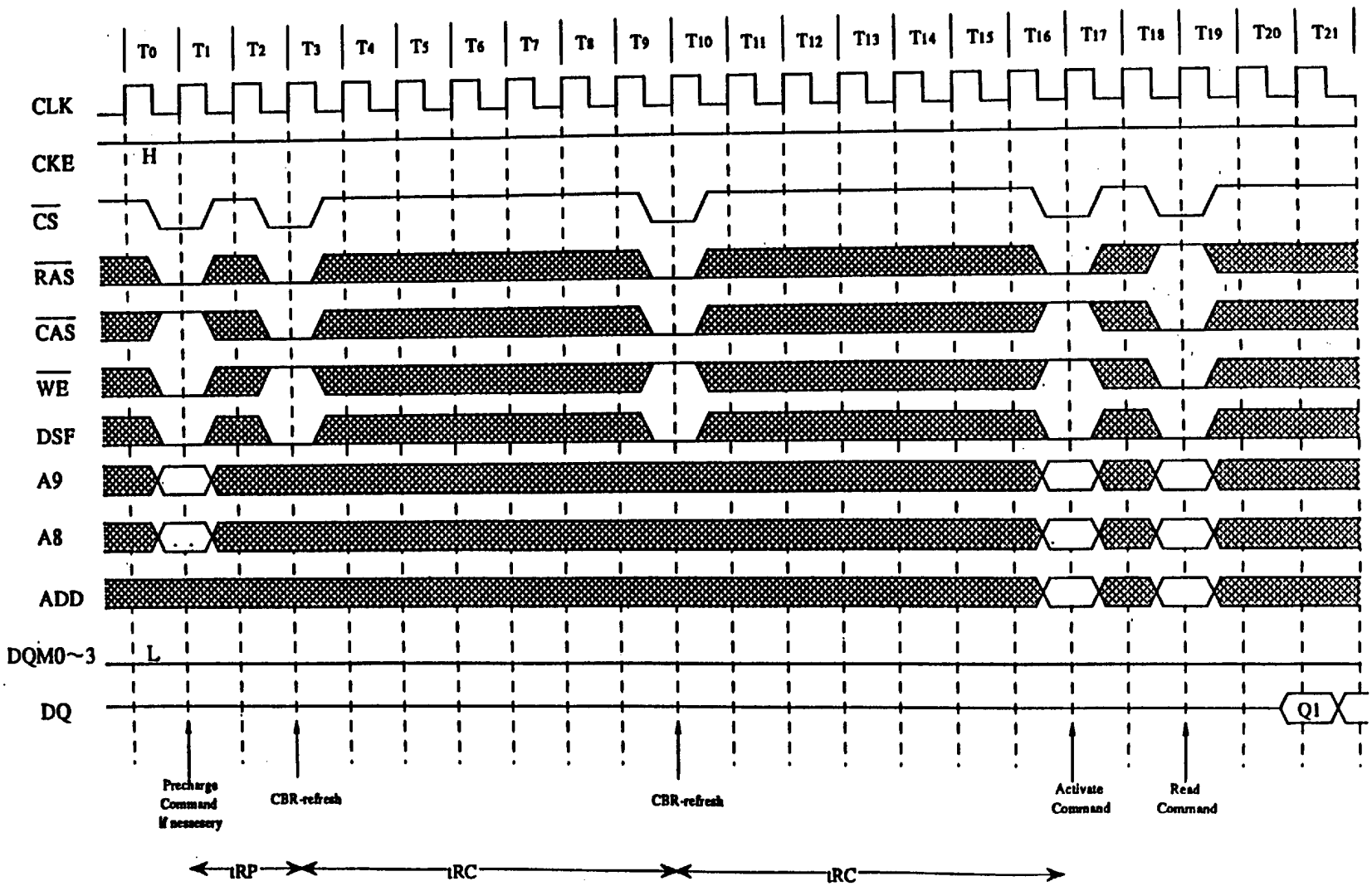
Power Down Mode and Clock Suspension

Burst Length = 4 CAS Latency = 2

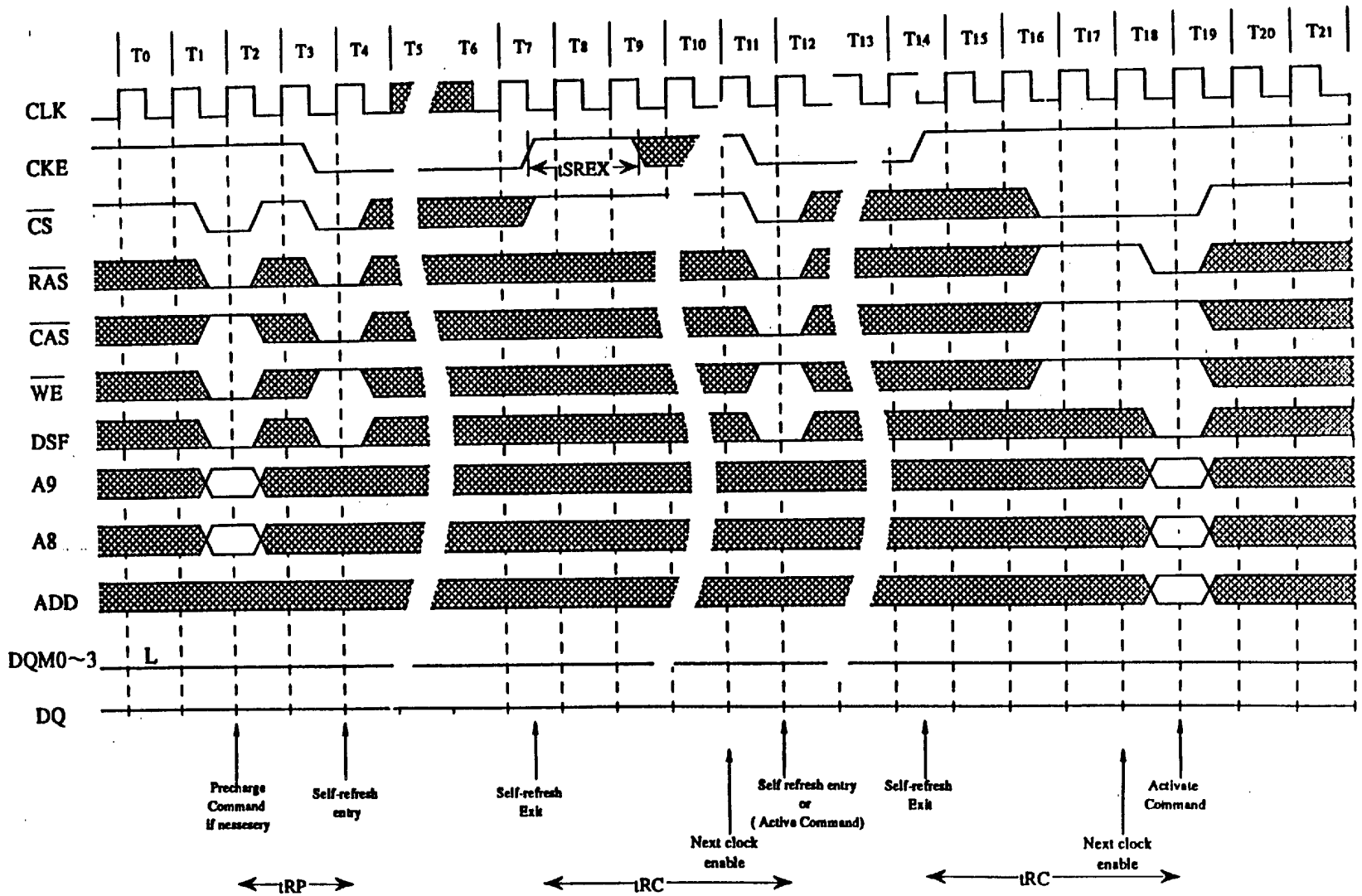


CBR Refresh

Burst Length = 4 CAS Latency =2

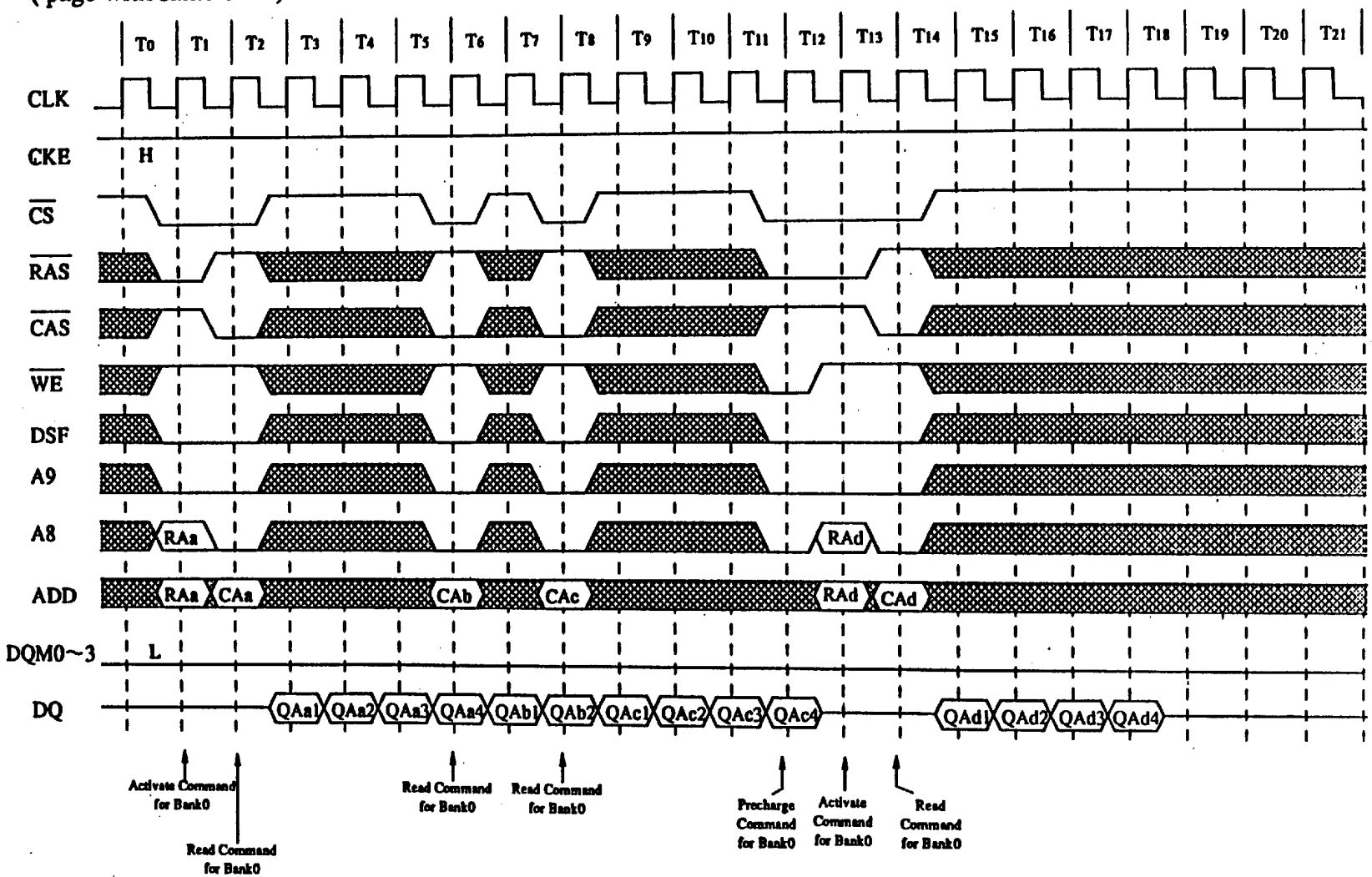


Self Refresh (entry&exit)



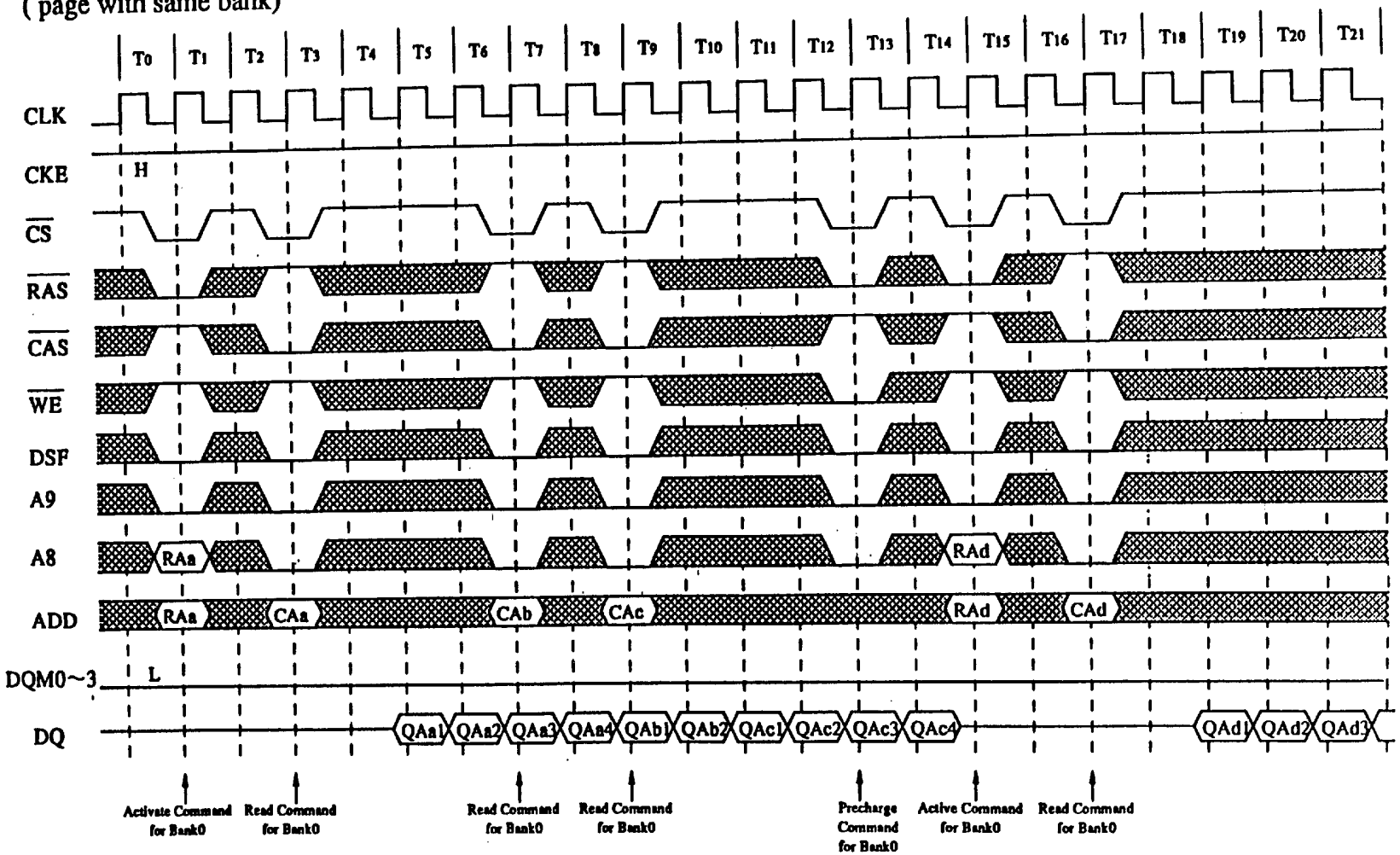
Random Column Read
(page with same bank)

Burst Length= 4 CAS Latency = 1



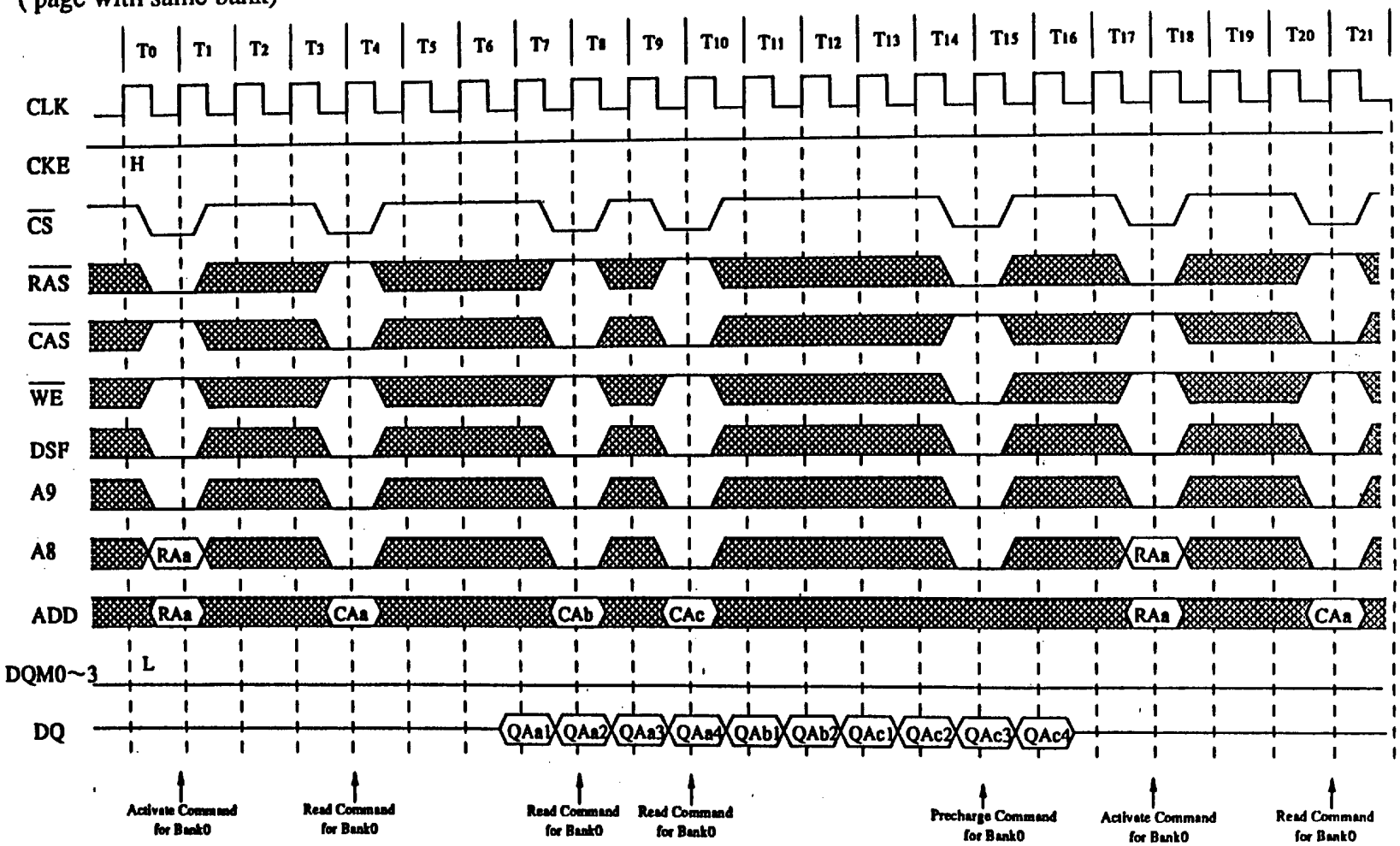
Random Column Read
(page with same bank)

Burst Length = 4 CAS Latency = 2



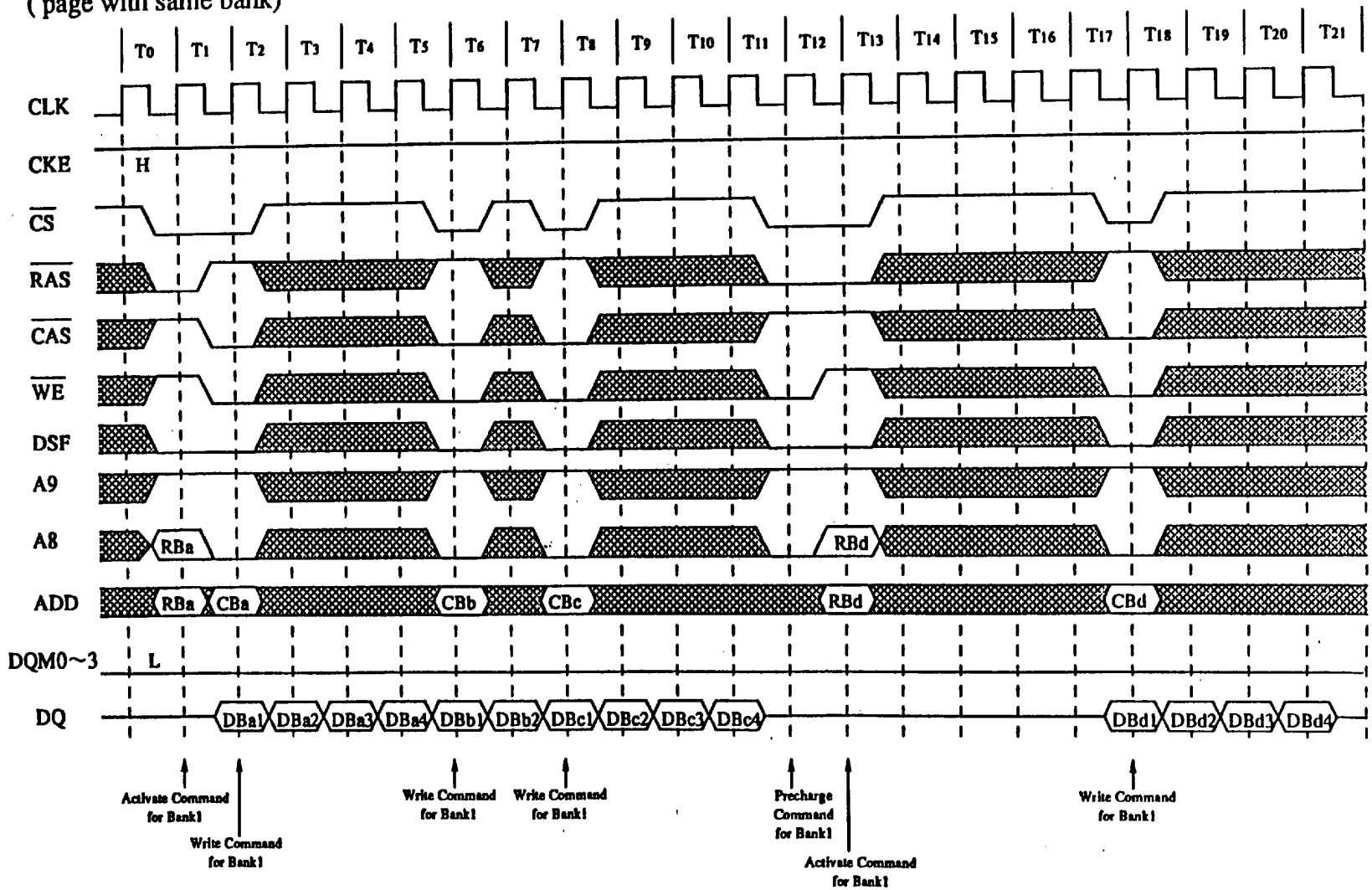
Random Column Read
(page with same bank)

Burst Length= 4 CAS Latency = 3



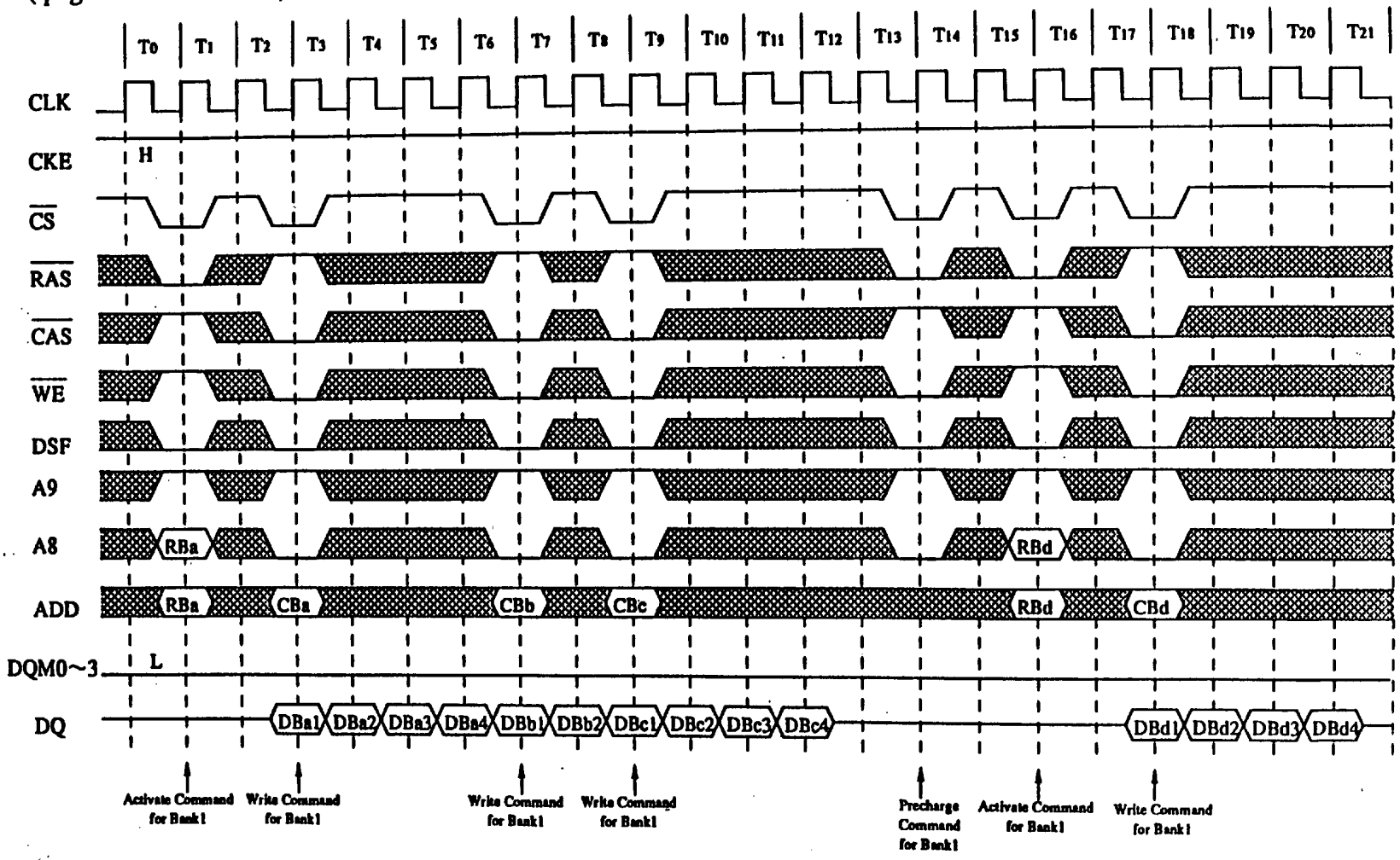
Random Column Write
(page with same bank)

Burst Length= 4 CAS Latency = 1



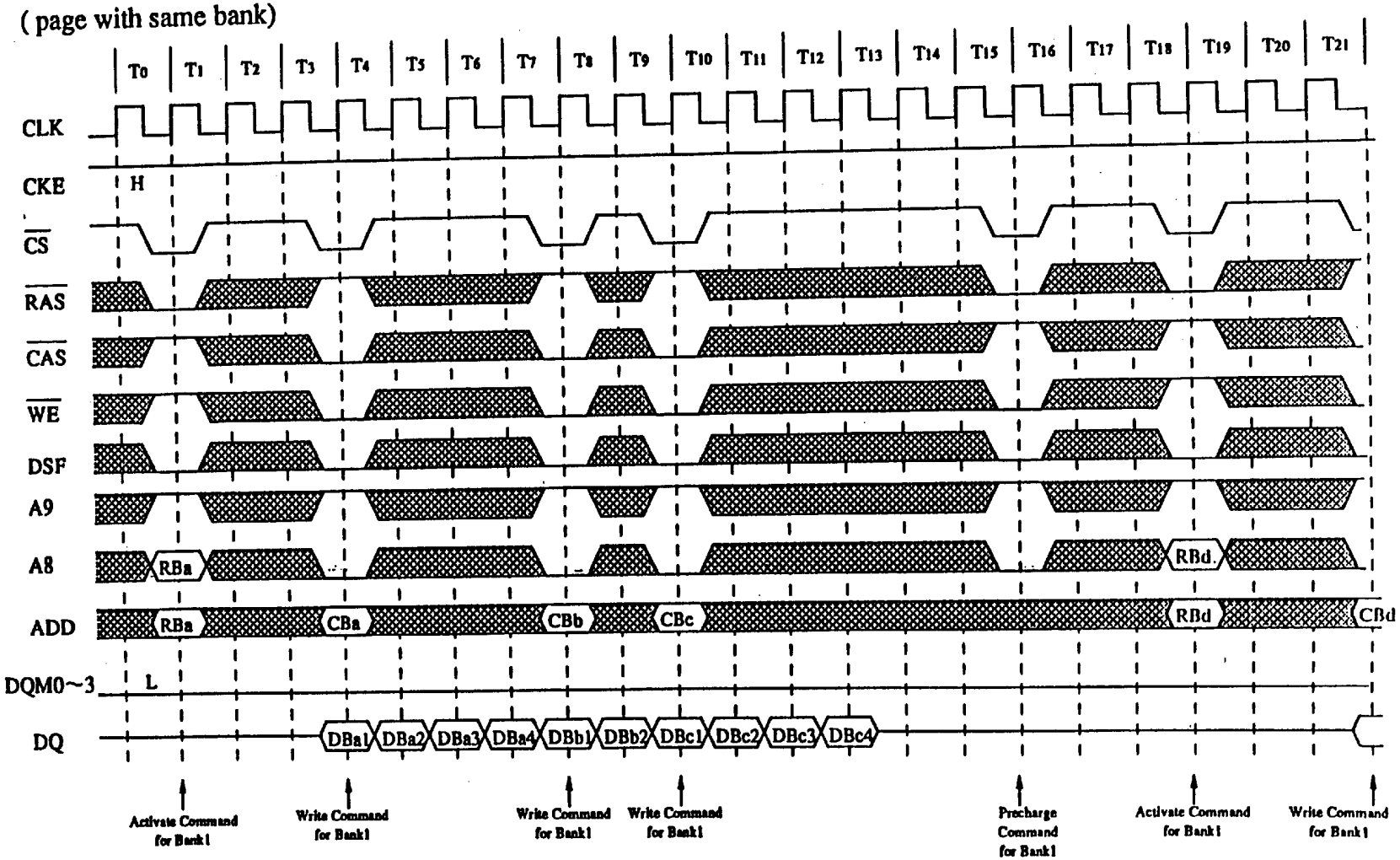
Random Column Write
(page with same bank)

Burst Length = 4 CAS Latency = 2



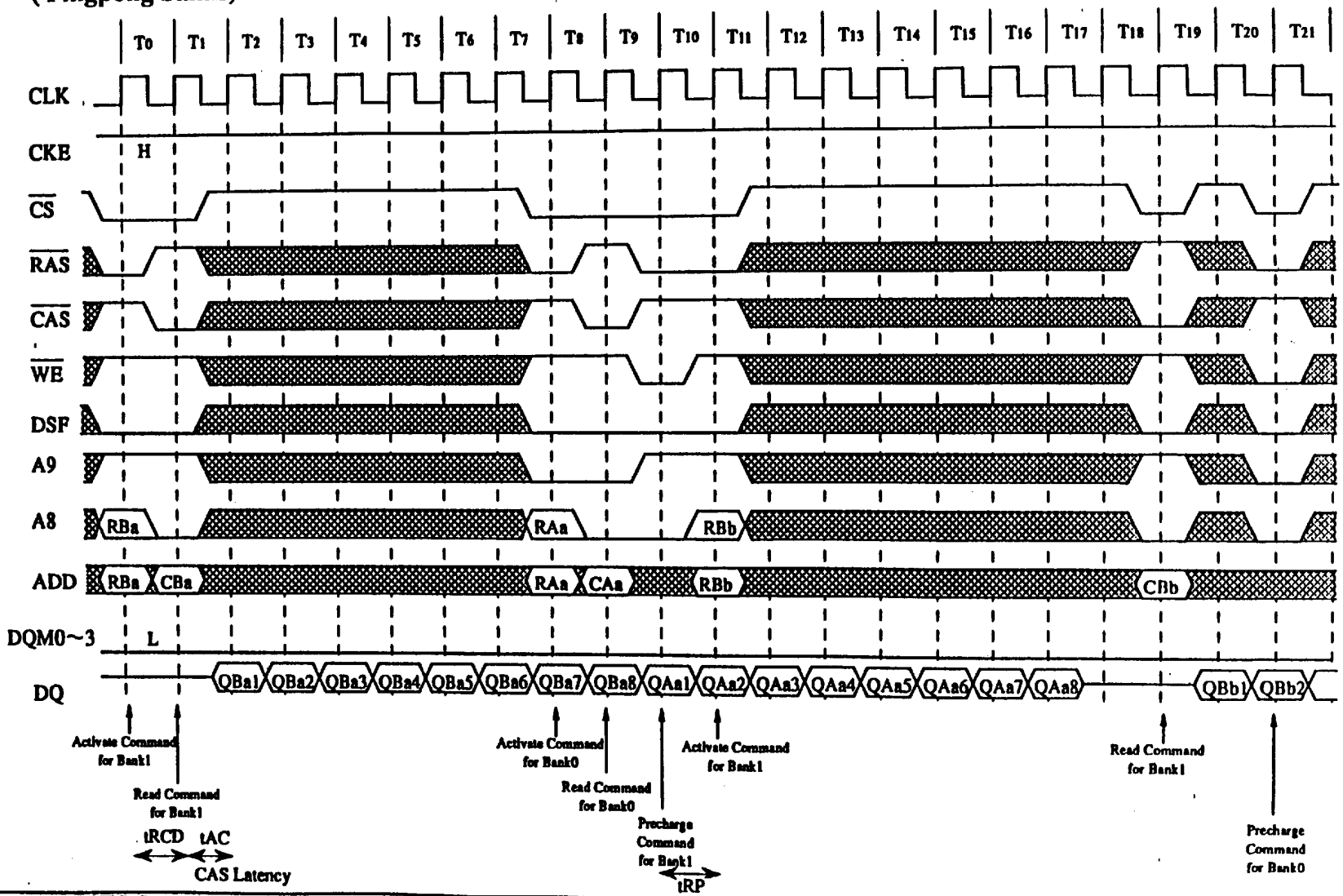
Random Column Write
(page with same bank)

Burst Length= 4 CAS Latency = 3



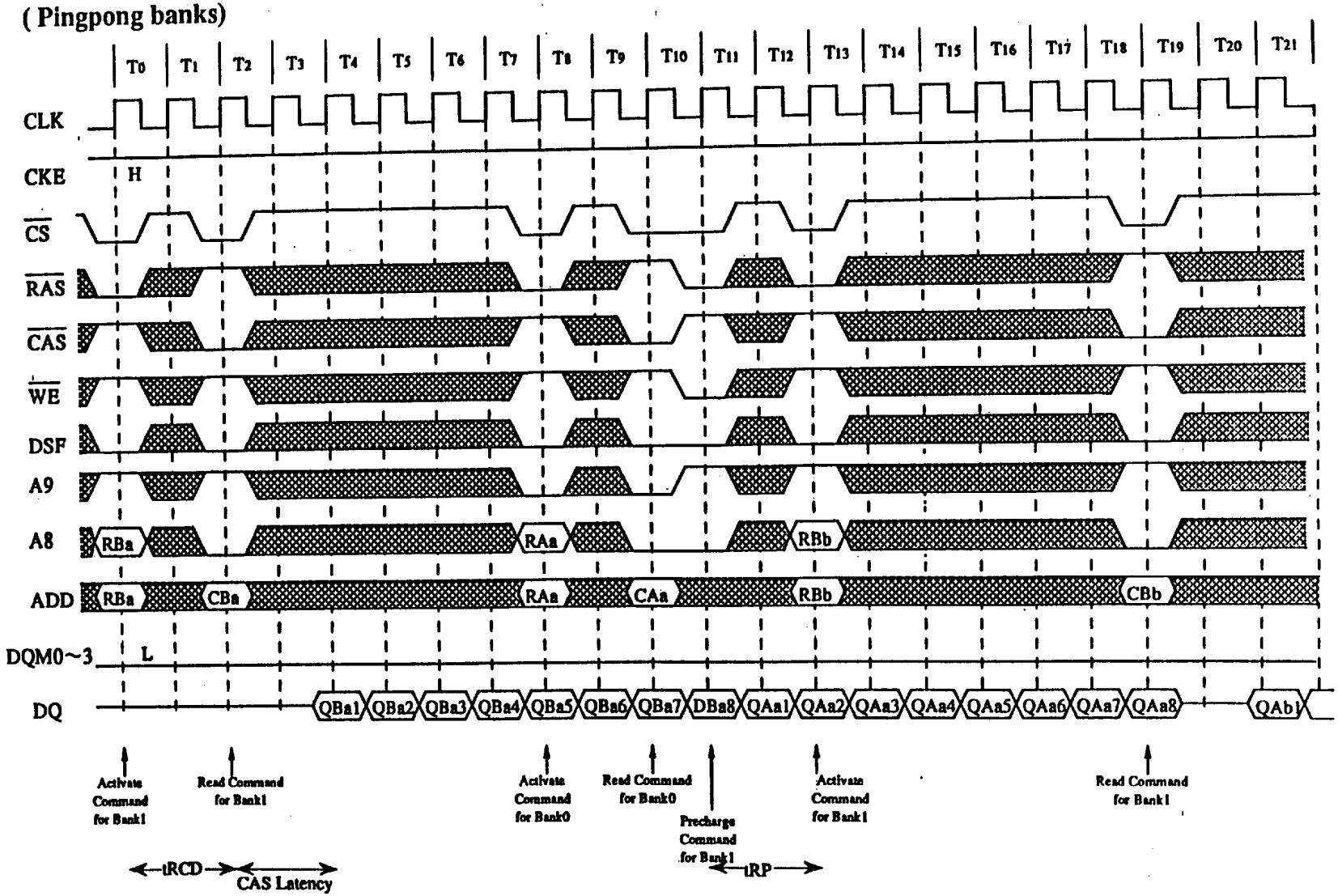
Random Row READ
(Pingpong banks)

Burst Length = 8 CAS Latency = 1



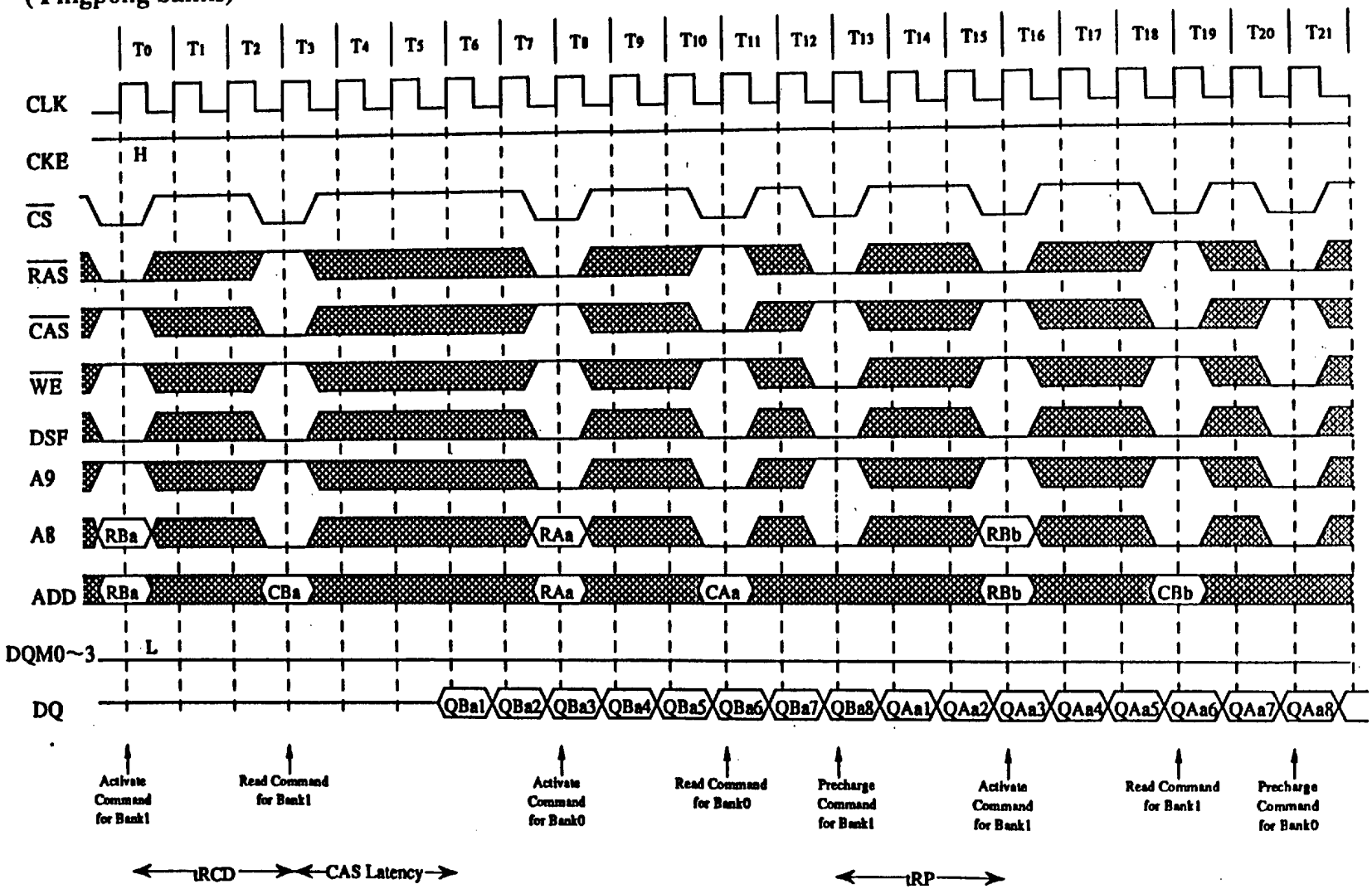
Random Row READ
(Pingpong banks)

Burst Length = 8 CAS Latency = 2



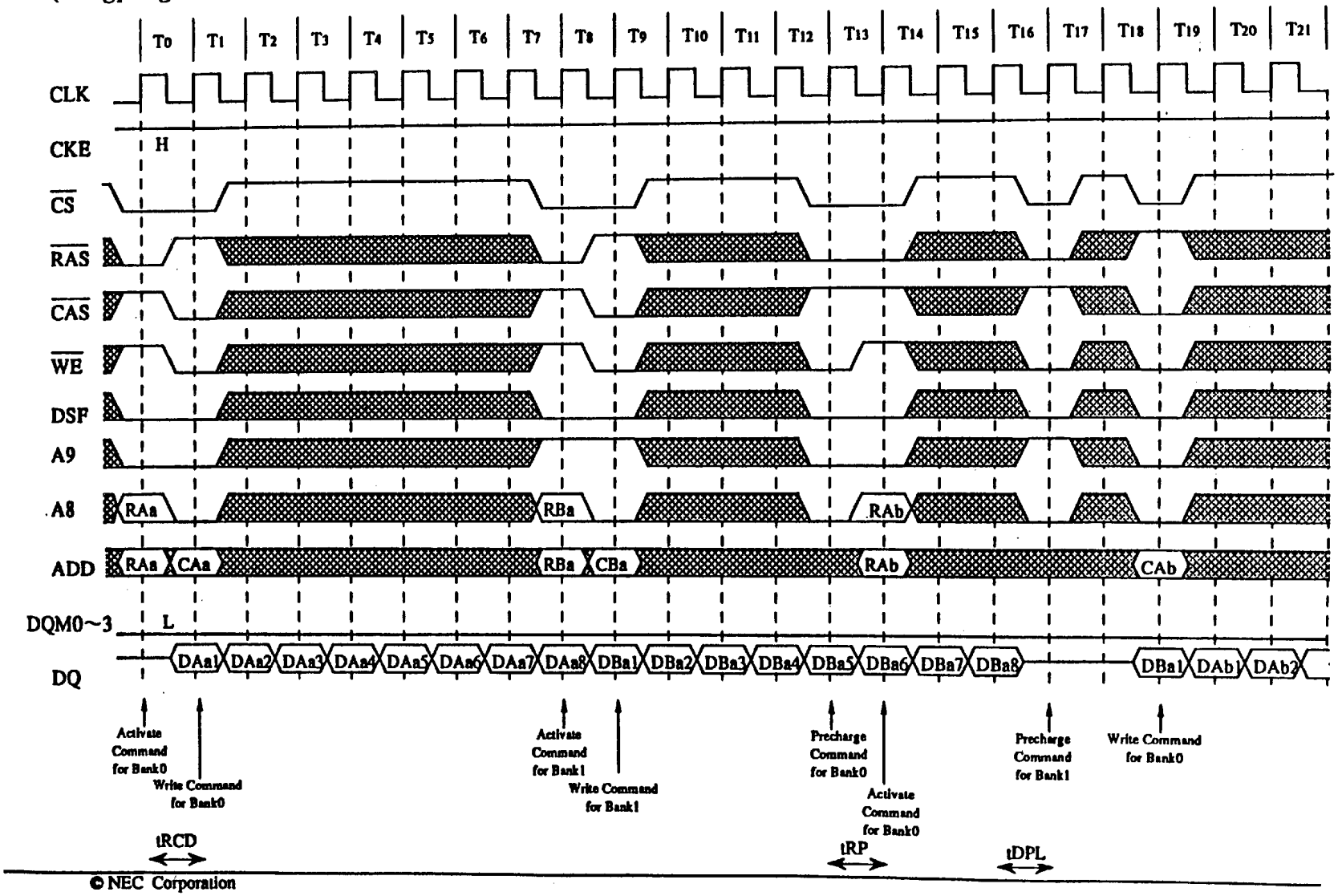
Random Row READ
(Pingpong banks)

Burst Length = 8 CAS Latency = 3



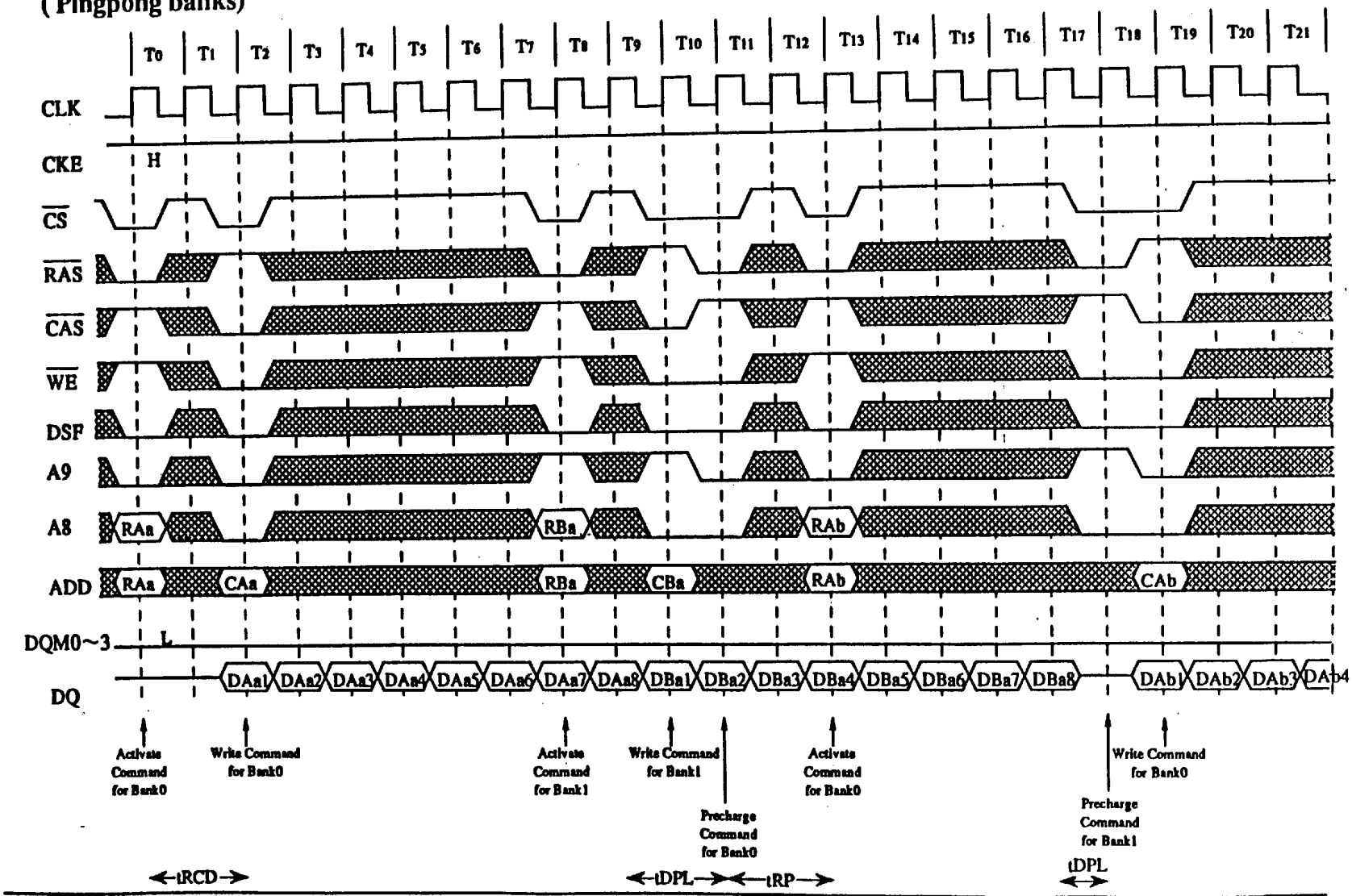
Random Row Write
(Pingpong banks)

Burst Length = 8 CAS Latency = 1



Random Row Write (Pingpong banks)

Burst Length = 8 CAS Latency = 2



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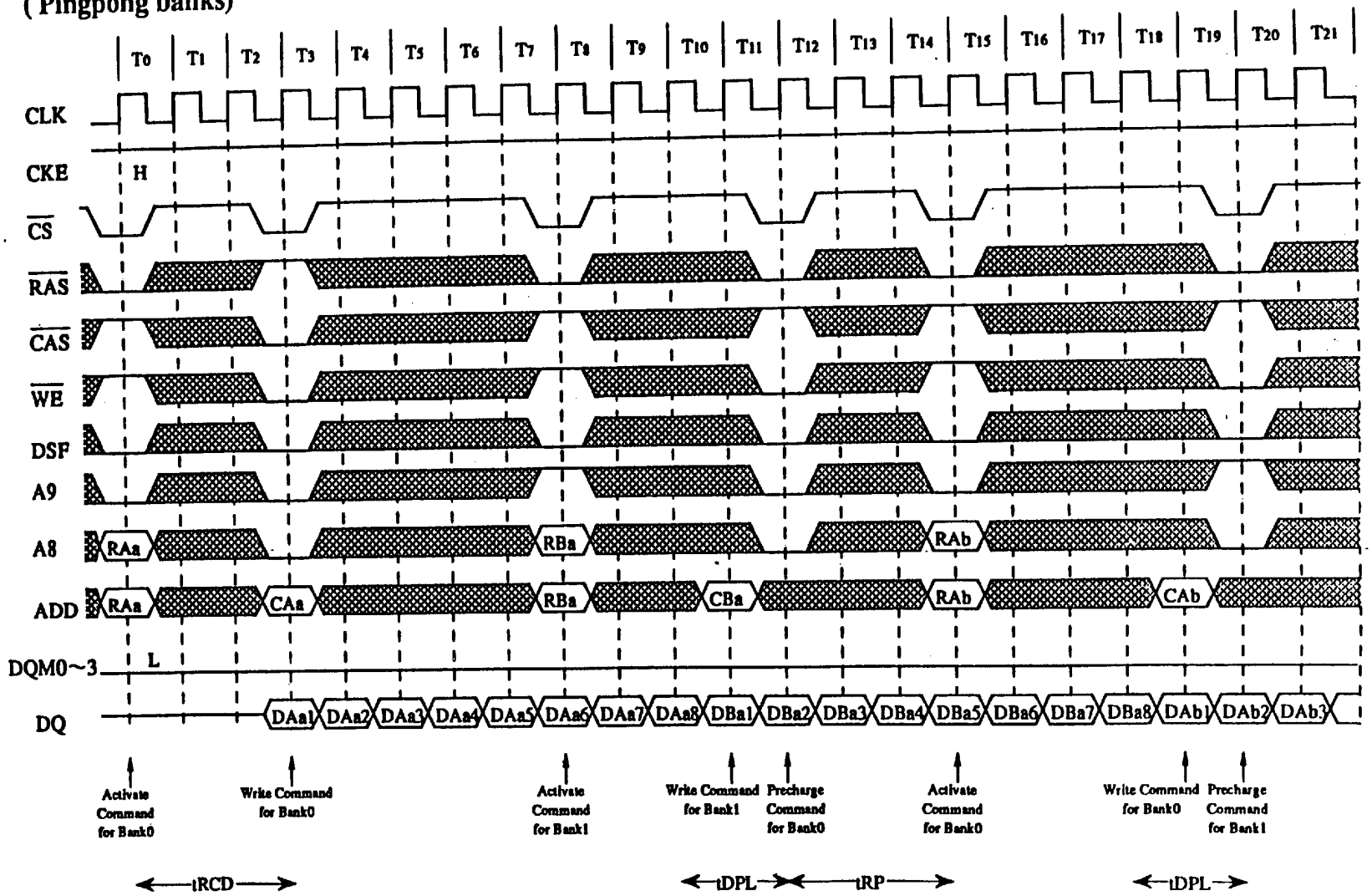
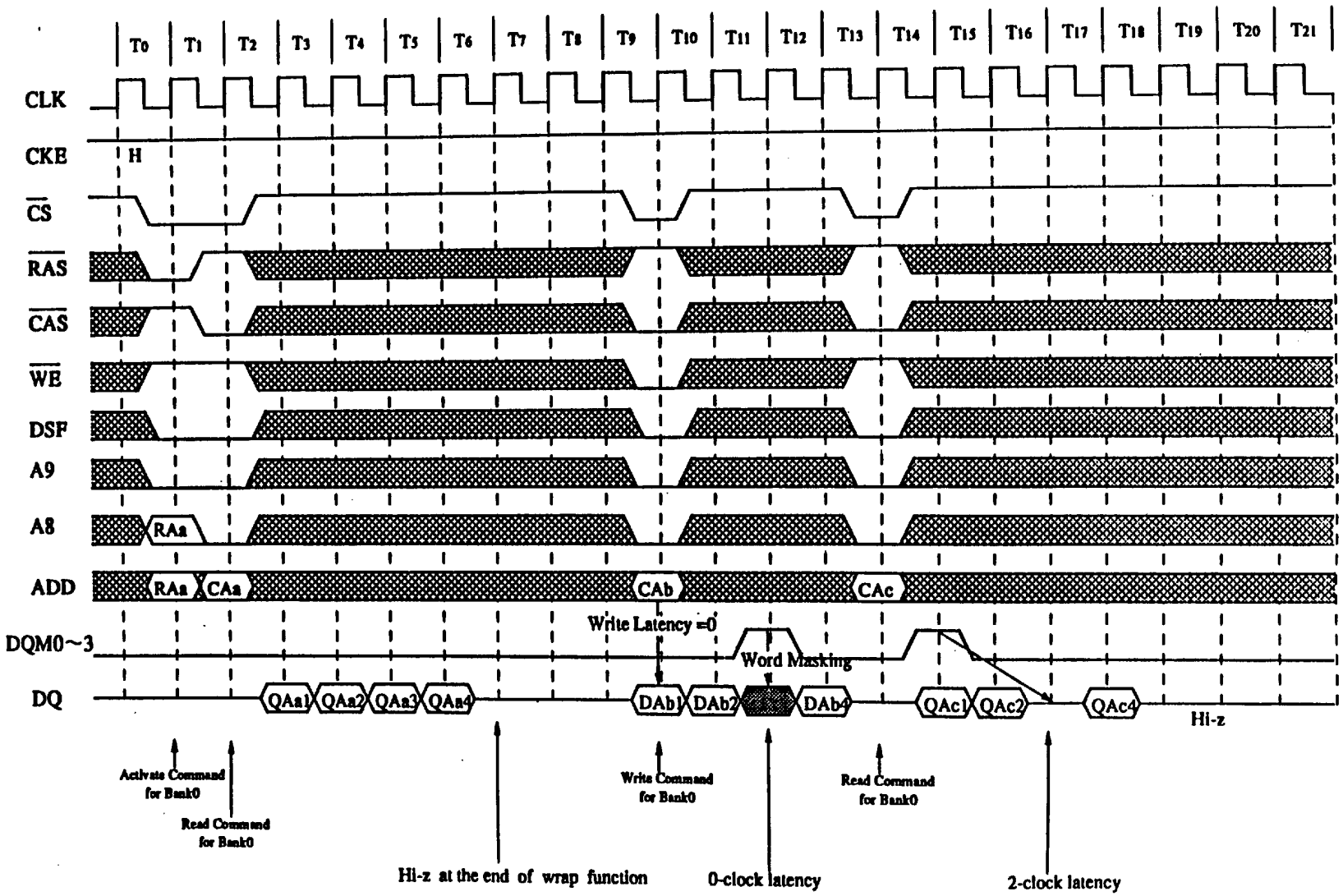
Random Row Write
(Pingpong banks)

Burst Length = 8 CAS Latency = 3



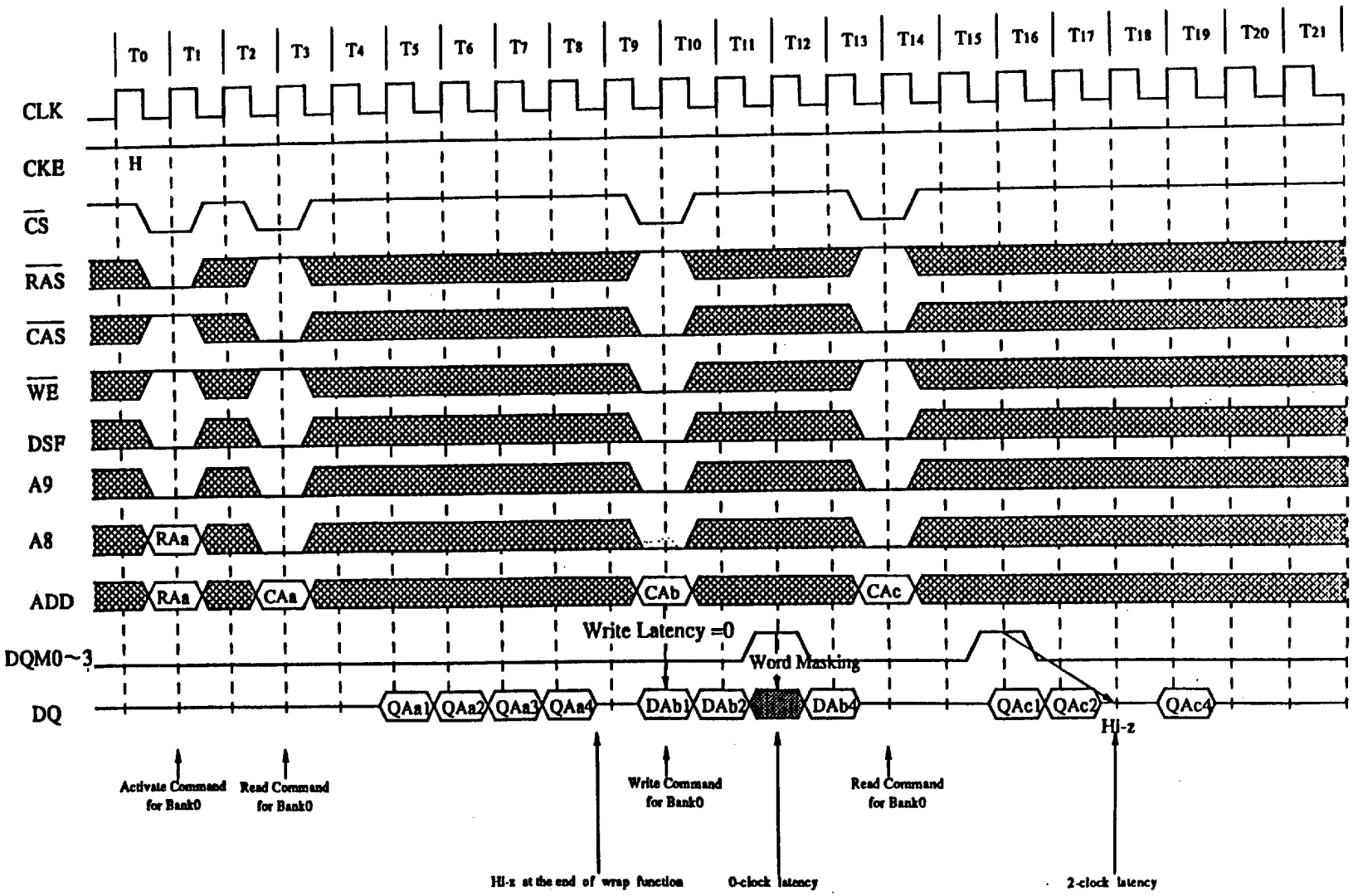
READ and WRITE

Burst Length = 4 CAS Latency = 1



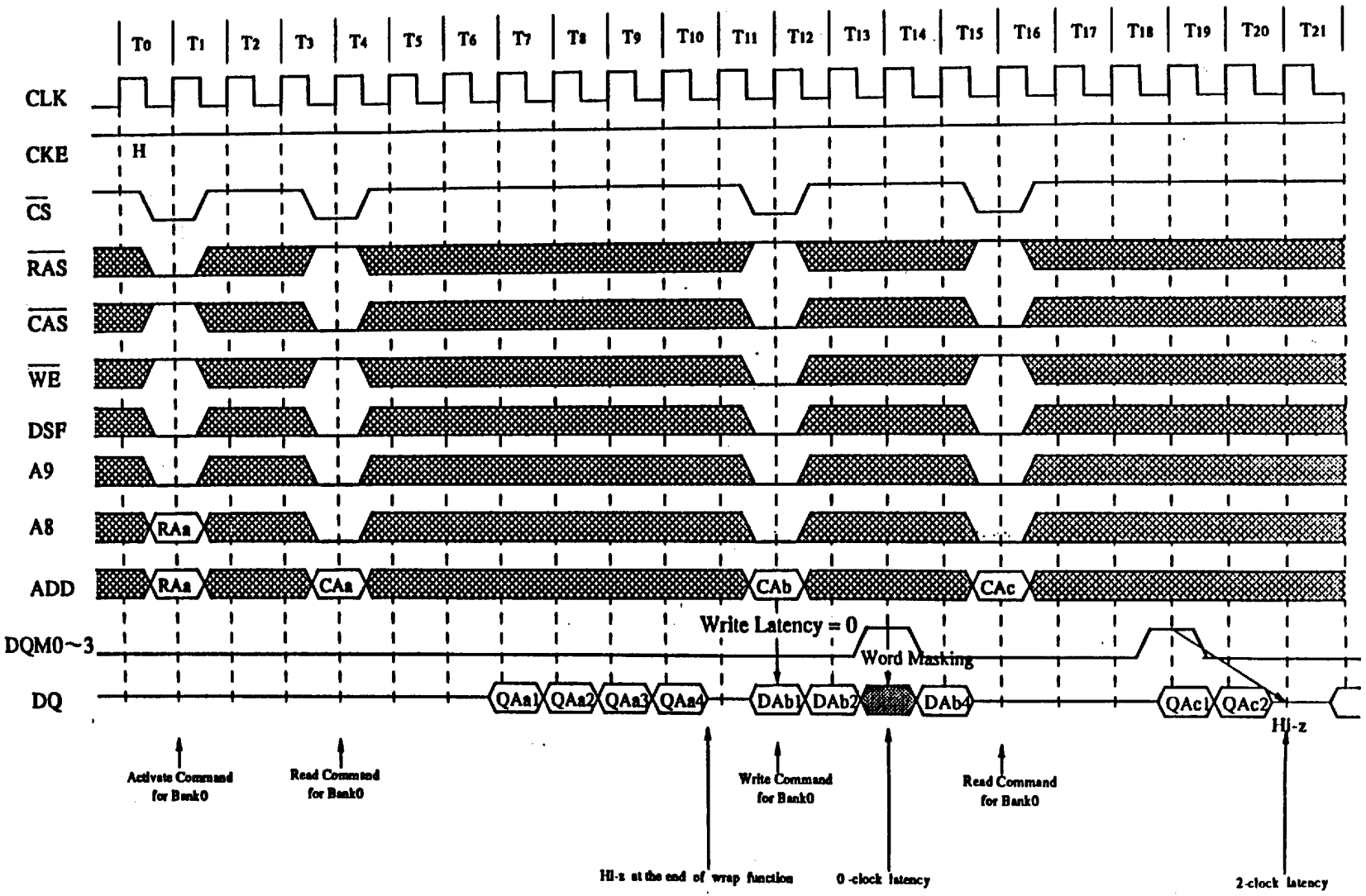
READ and WRITE

Burst Length = 4 CAS Latency = 2



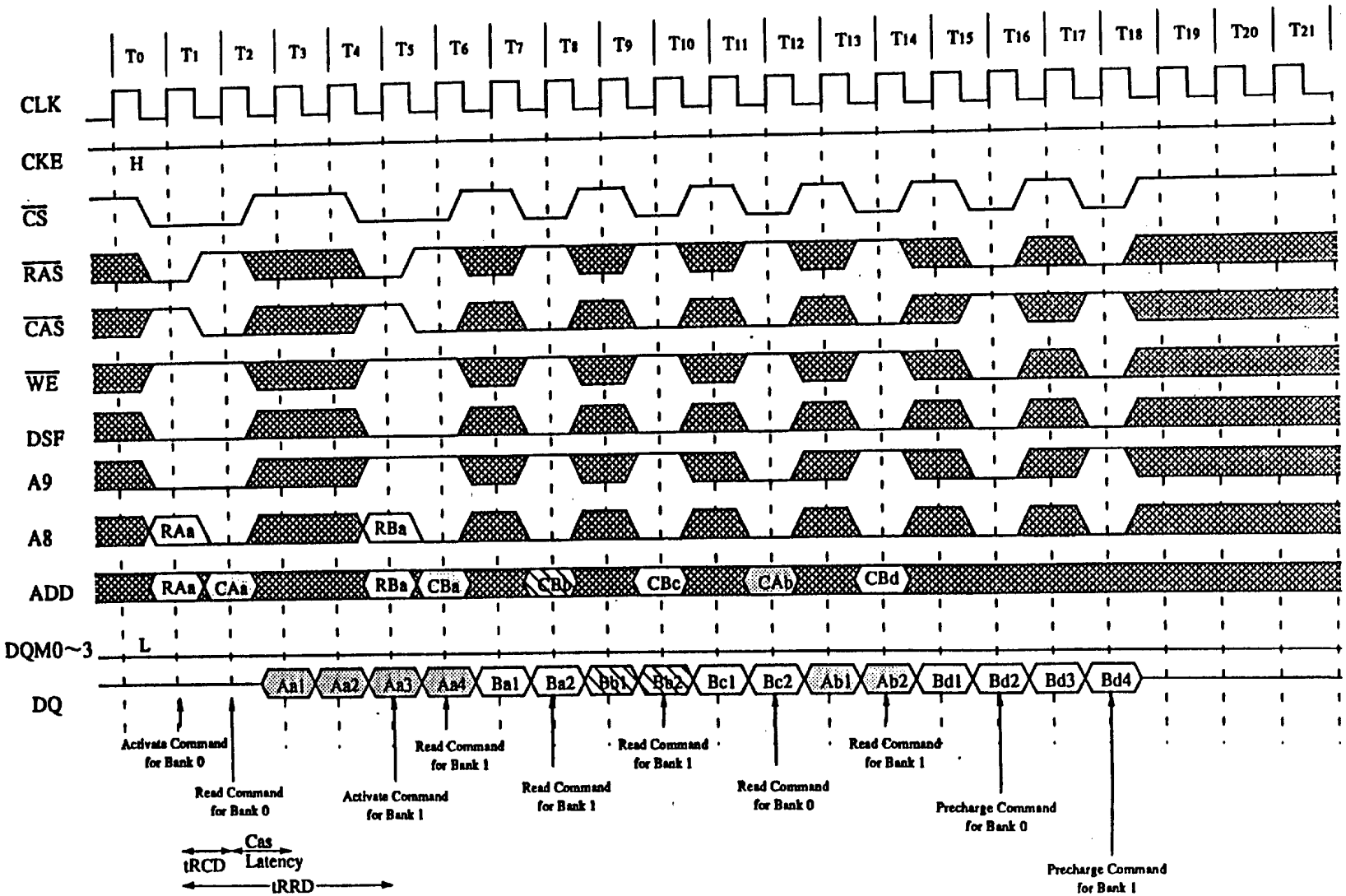
READ and WRITE

Burst Length = 4 CAS Latency = 3



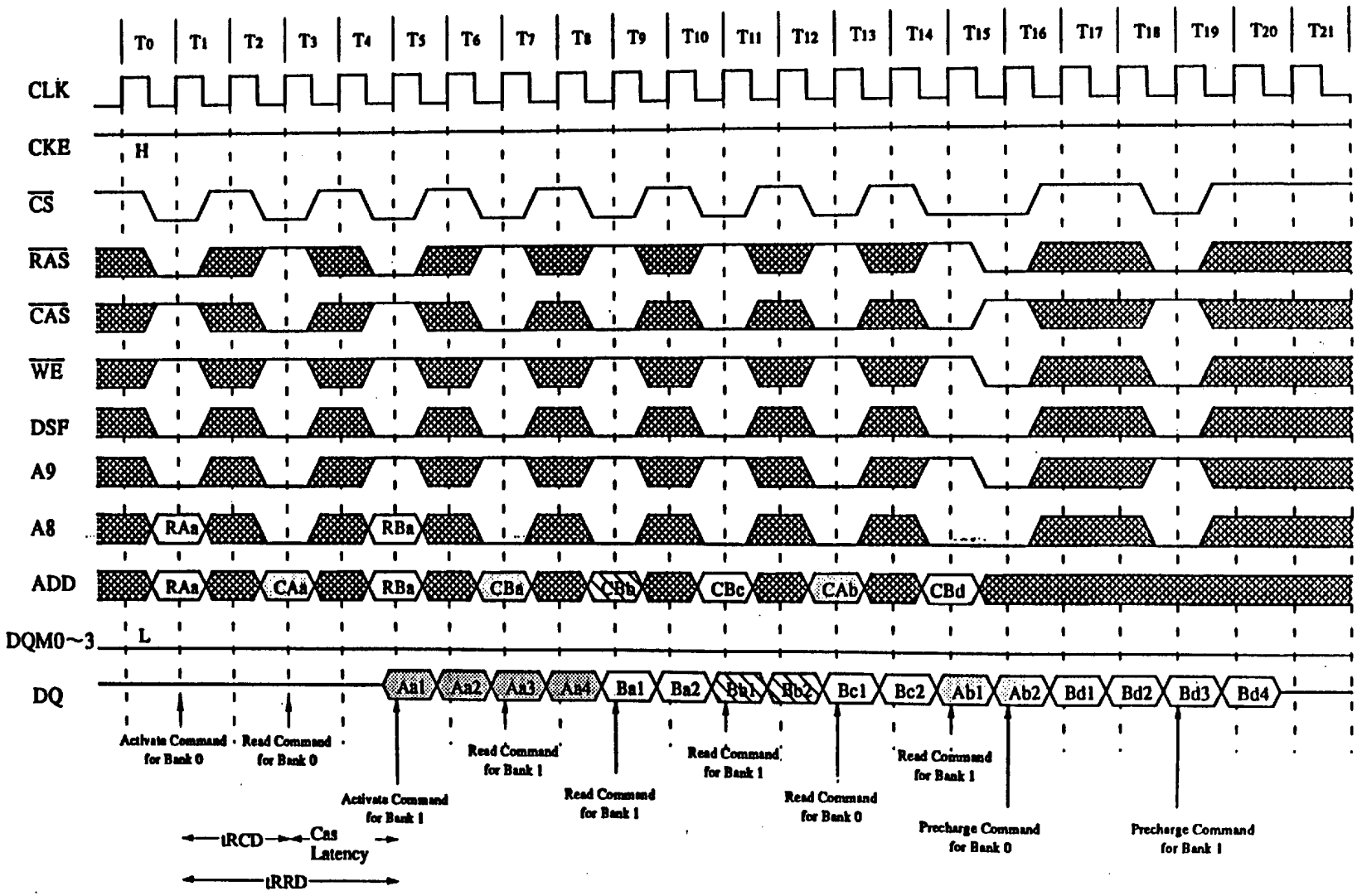
Interleaved Column READ CYCLE

Burst Length = 4 CAS Latency = 1



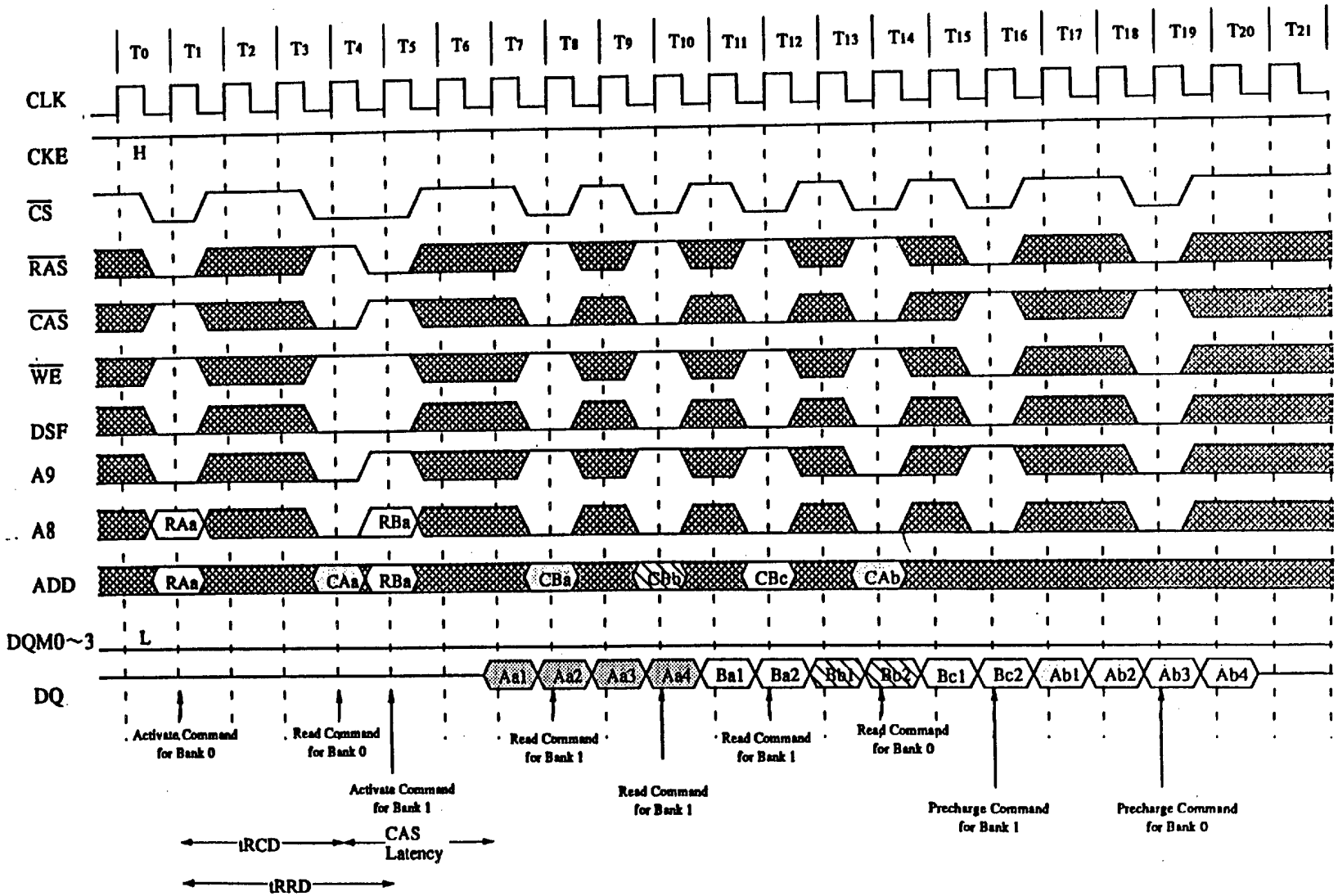
Interleaved Column READ CYCLE

Burst Length = 4 CAS Latency = 2



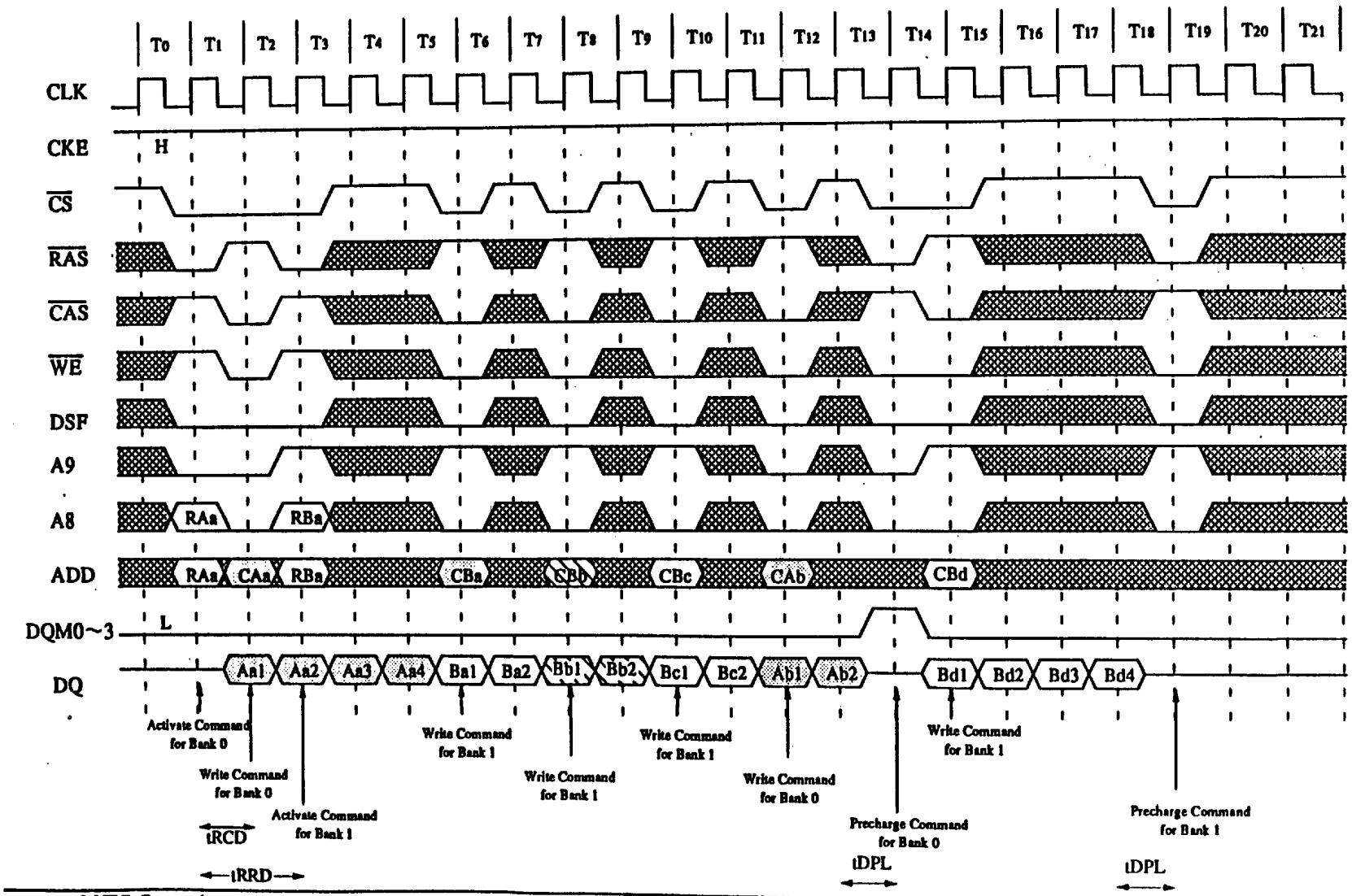
Interleaved Column READ CYCLE

Burst Length = 4 CAS Latency = 3



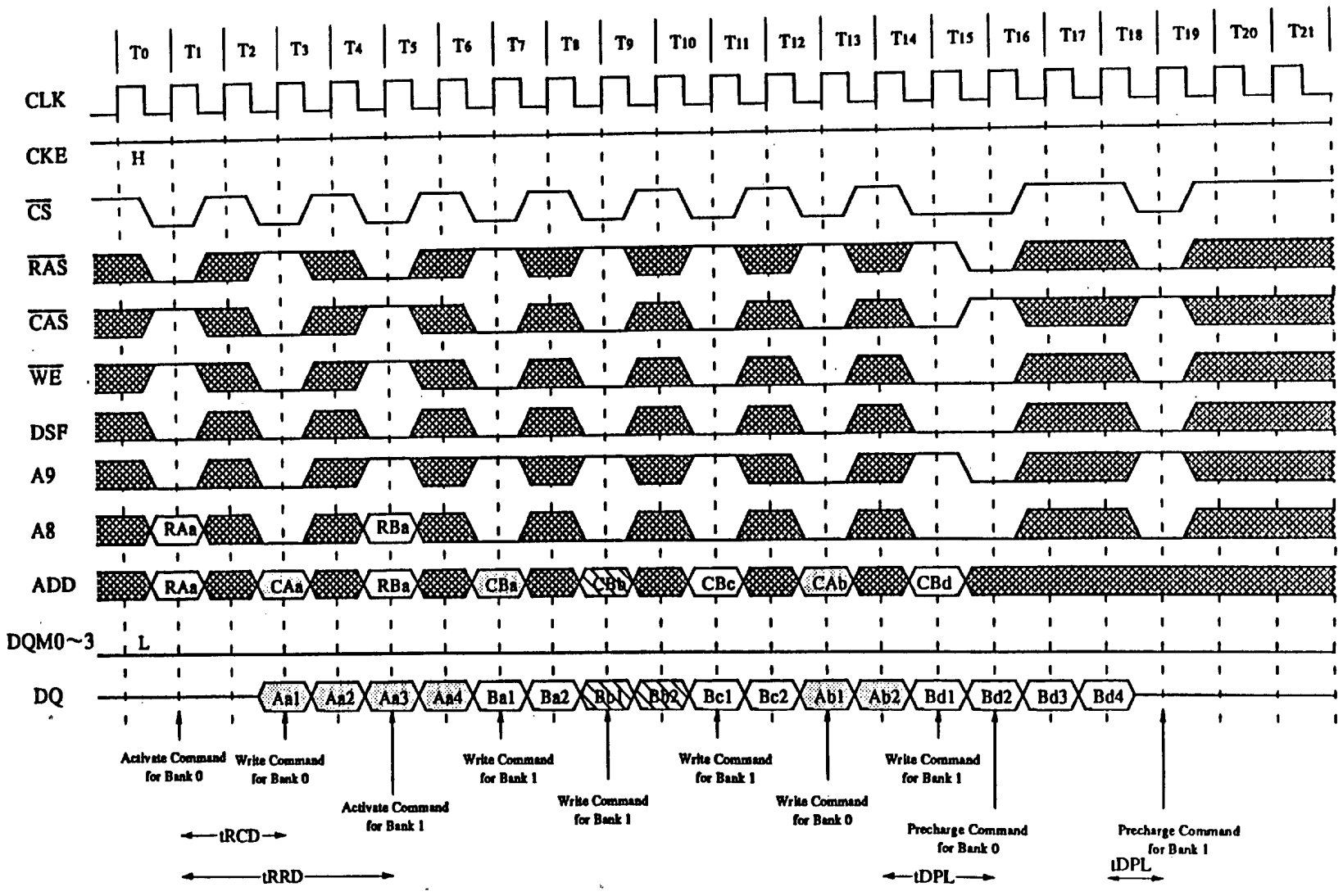
Interleaved Column WRITE CYCLE

Burst Length = 4 CAS Latency = 1



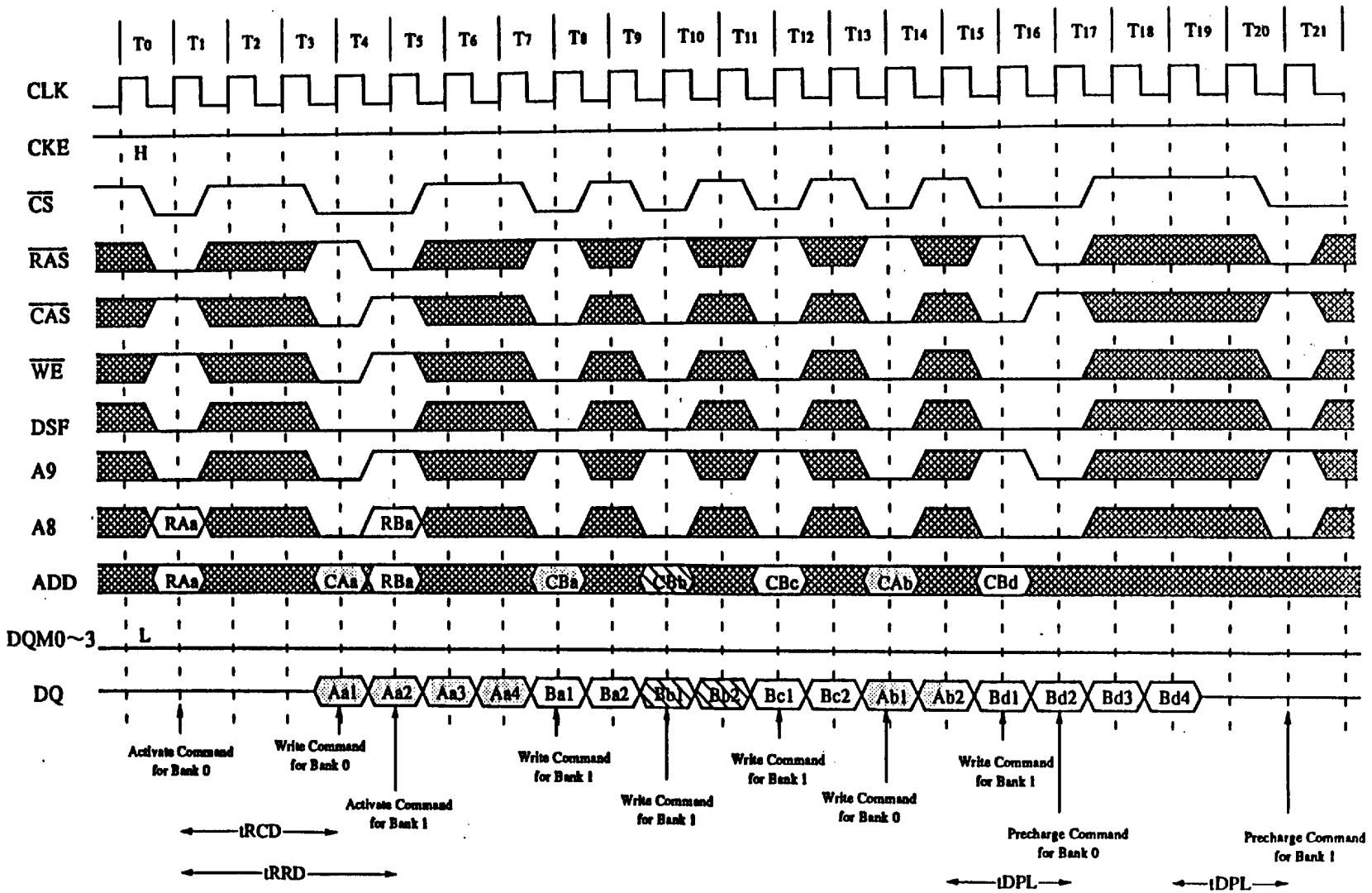
Interleaved Column WRITE CYCLE

Burst Length = 4 CAS Latency = 2



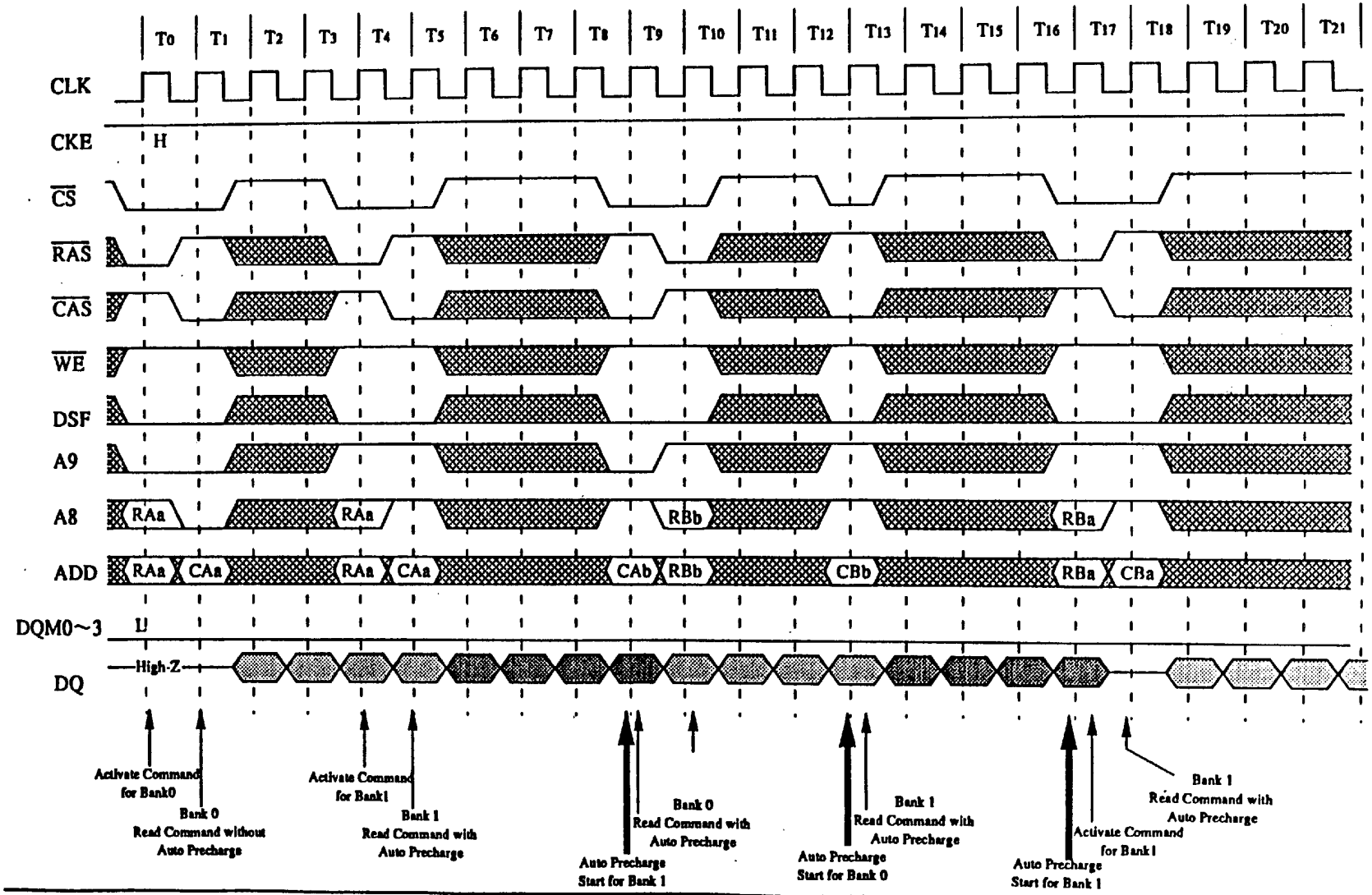
Interleaved Column WRITE CYCLE

Burst Length = 4 CAS Latency = 3



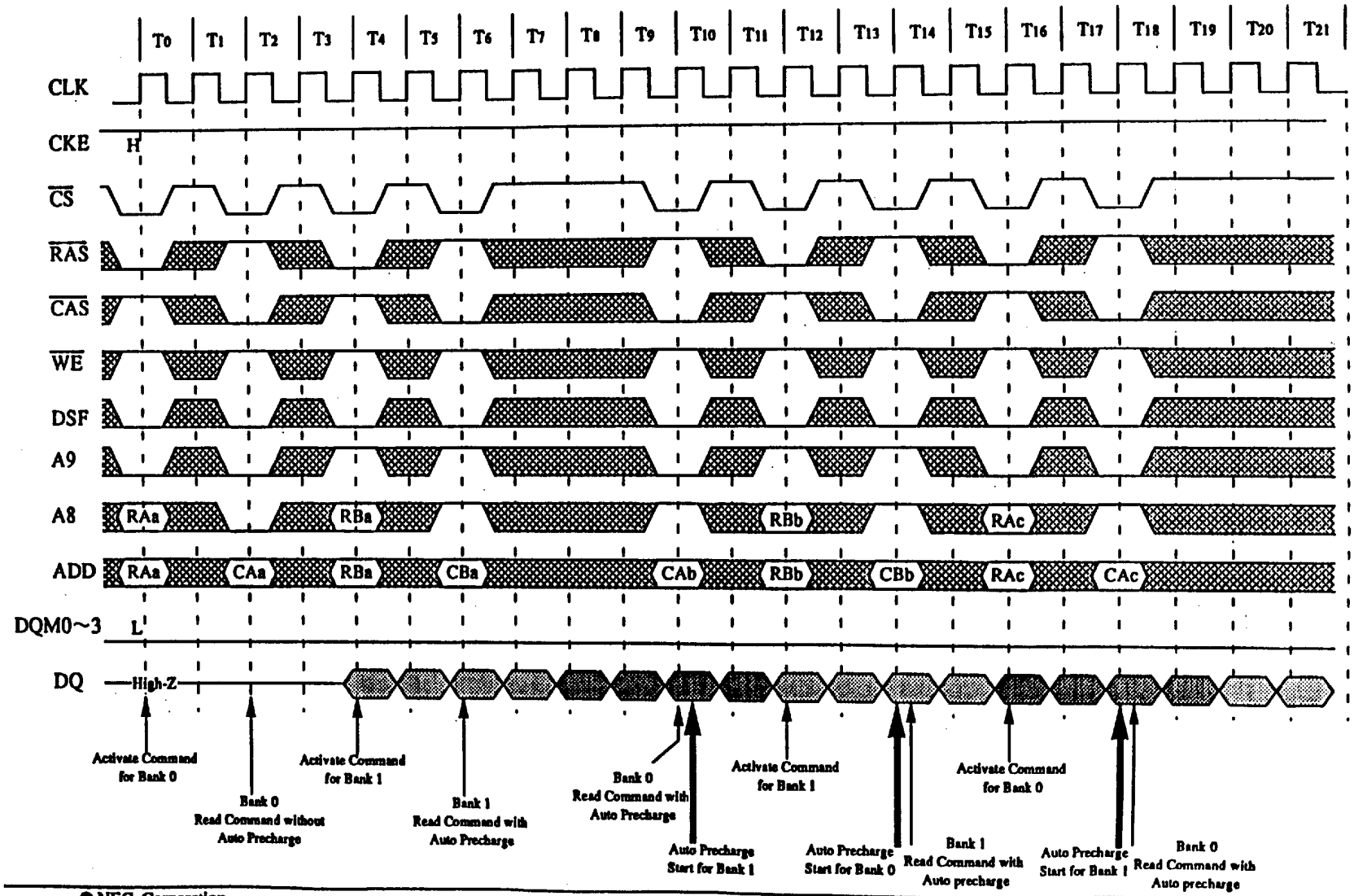
Auto Precharge after Read Burst

Burst Length = 4 CAS Latency = 1



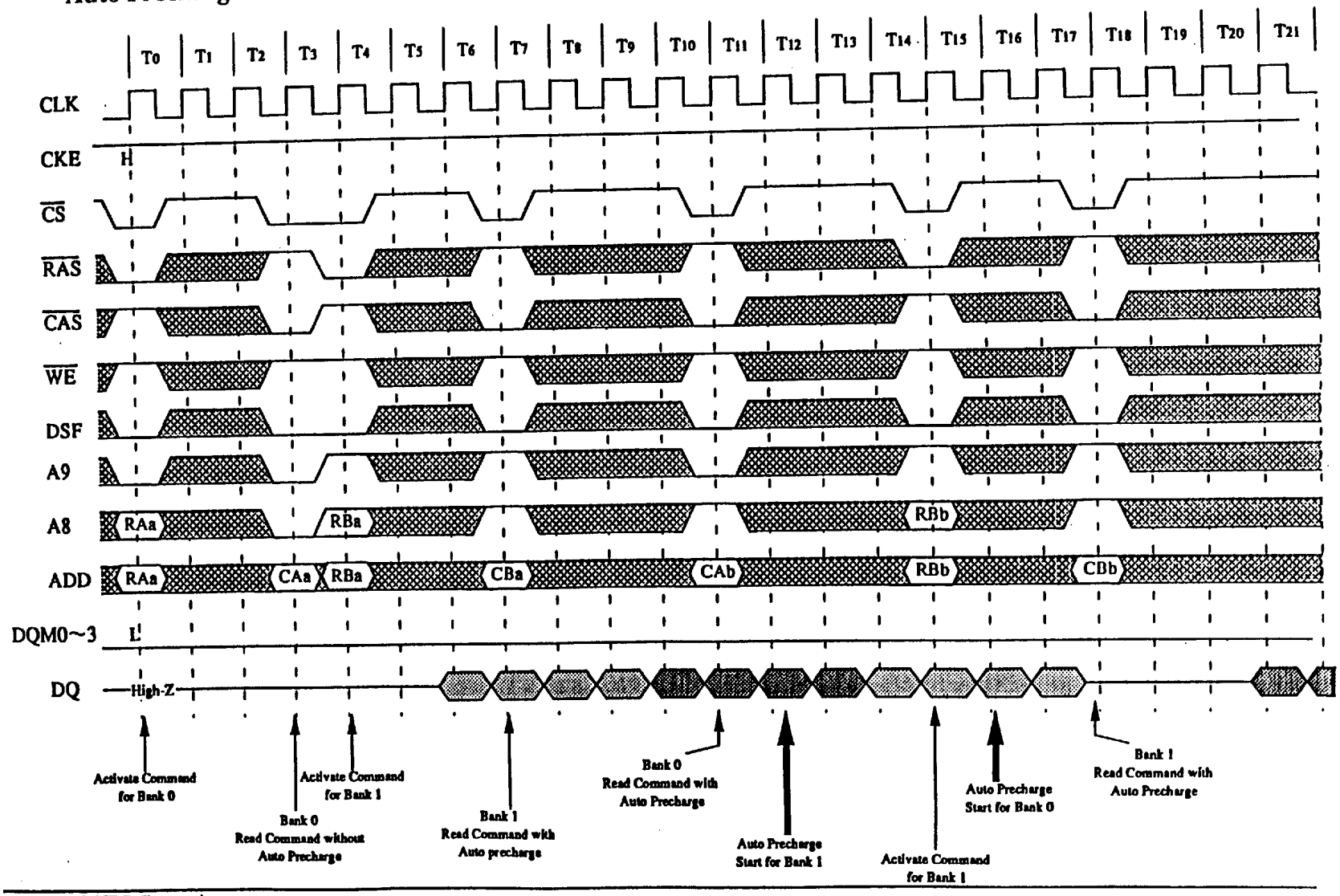
Auto Precharge after Read Burst

Burst Length = 4 CAS Latency = 2



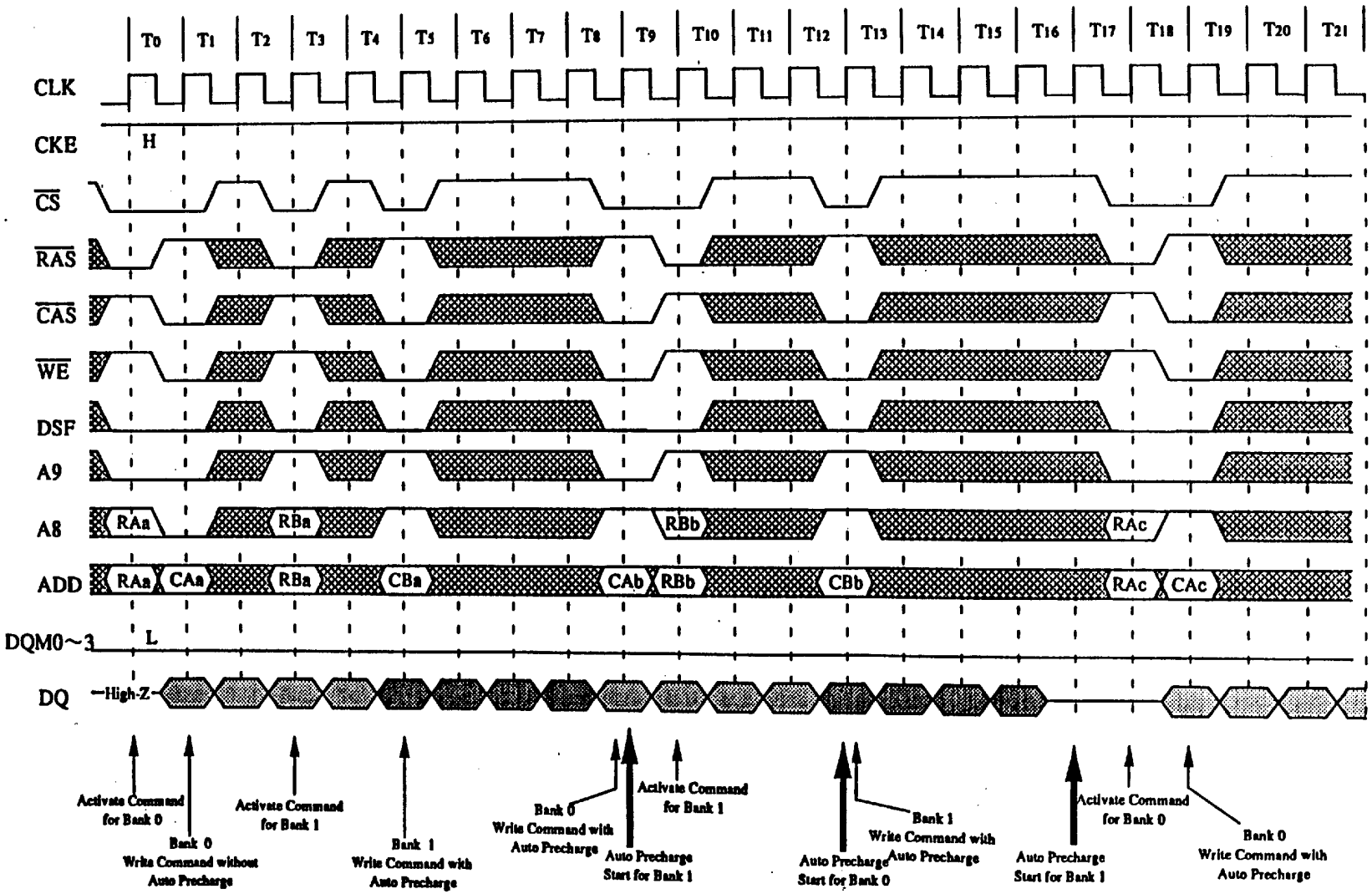
Auto Precharge after Read Burst

Burst Length = 4 CAS Latency = 3



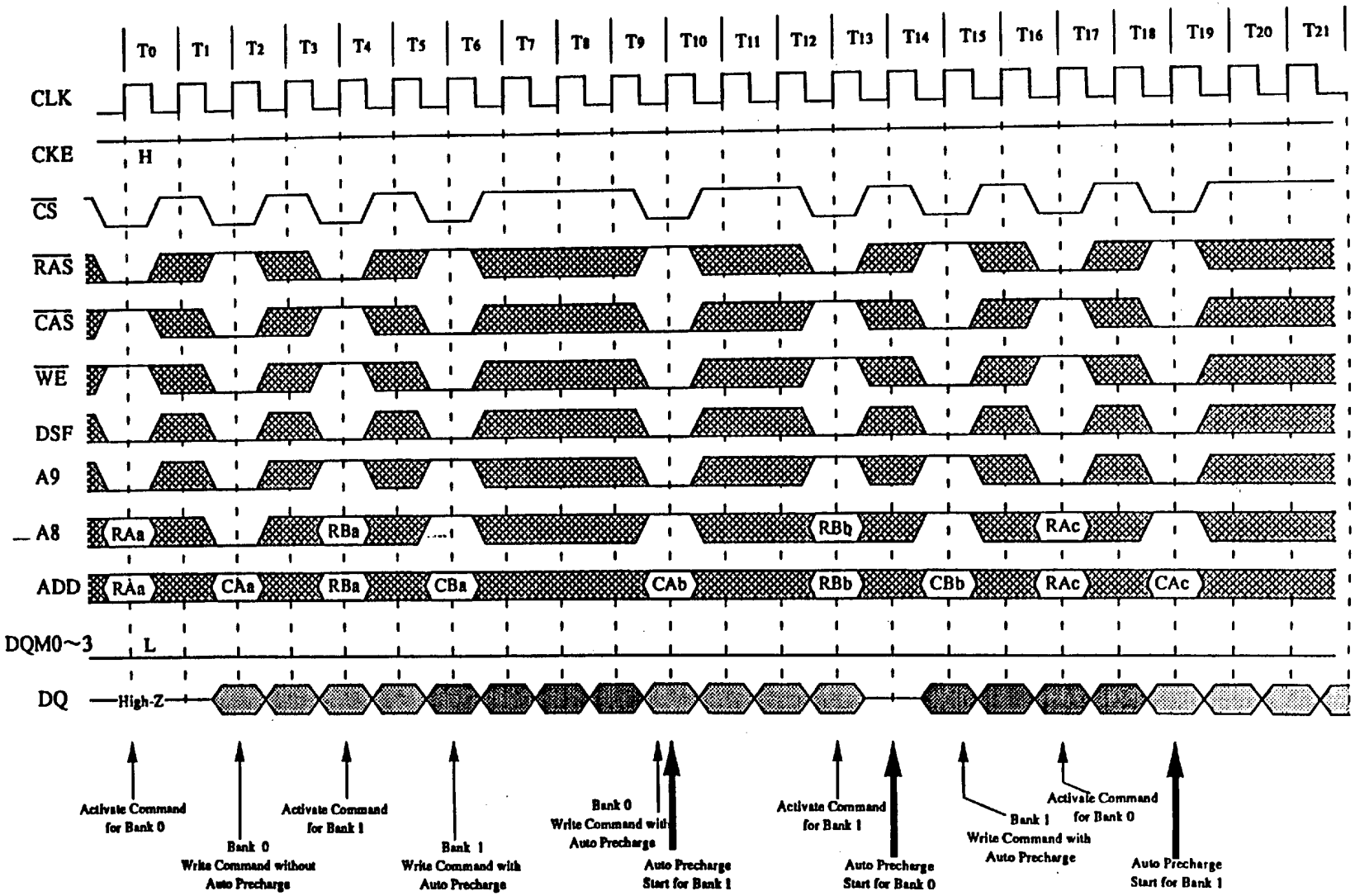
Auto Precharge after Write Burst

Burst Length = 4 CAS Latency = 1



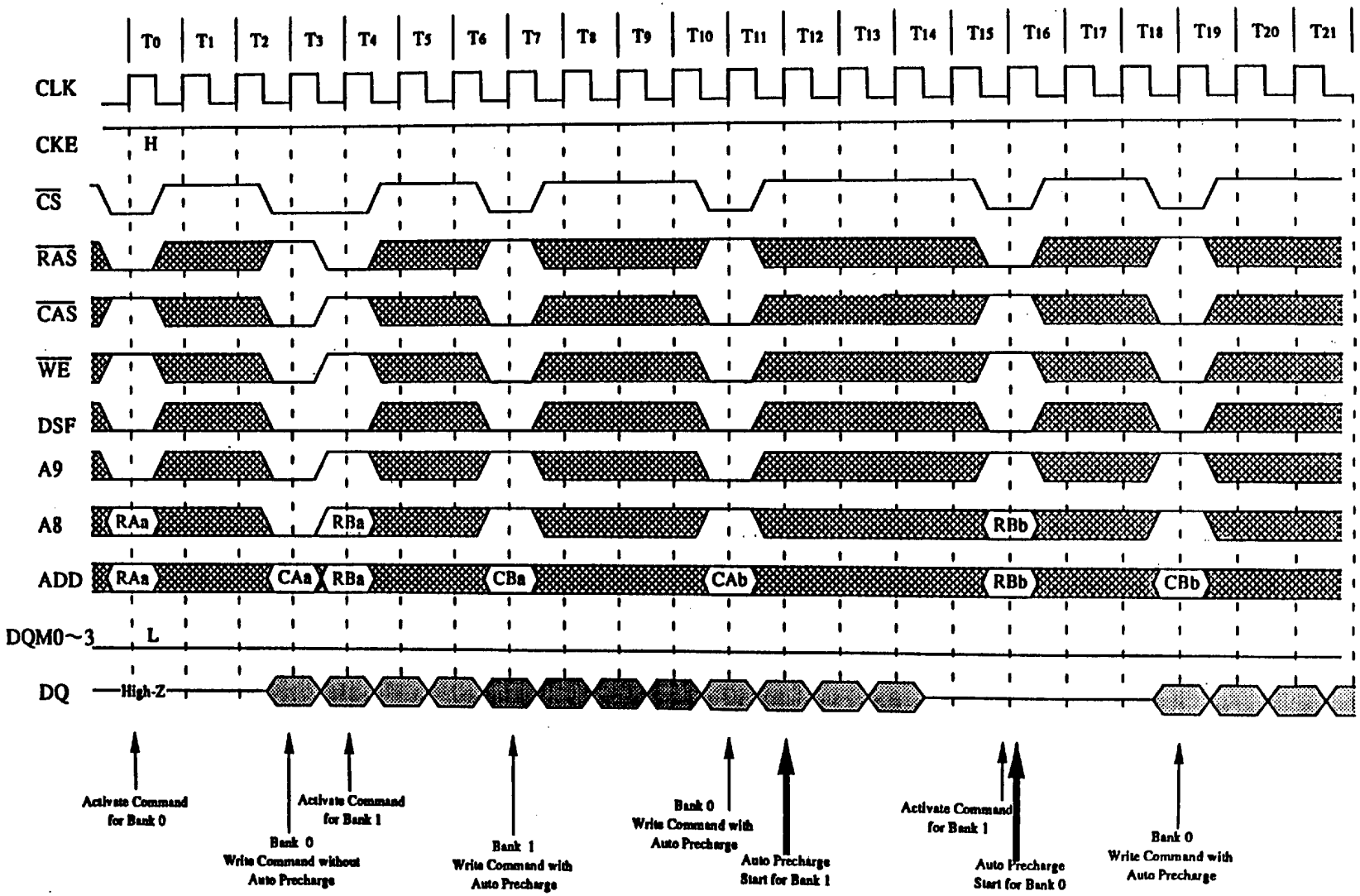
Auto Precharge after Write Burst

Burst Length = 4 CAS Latency = 2



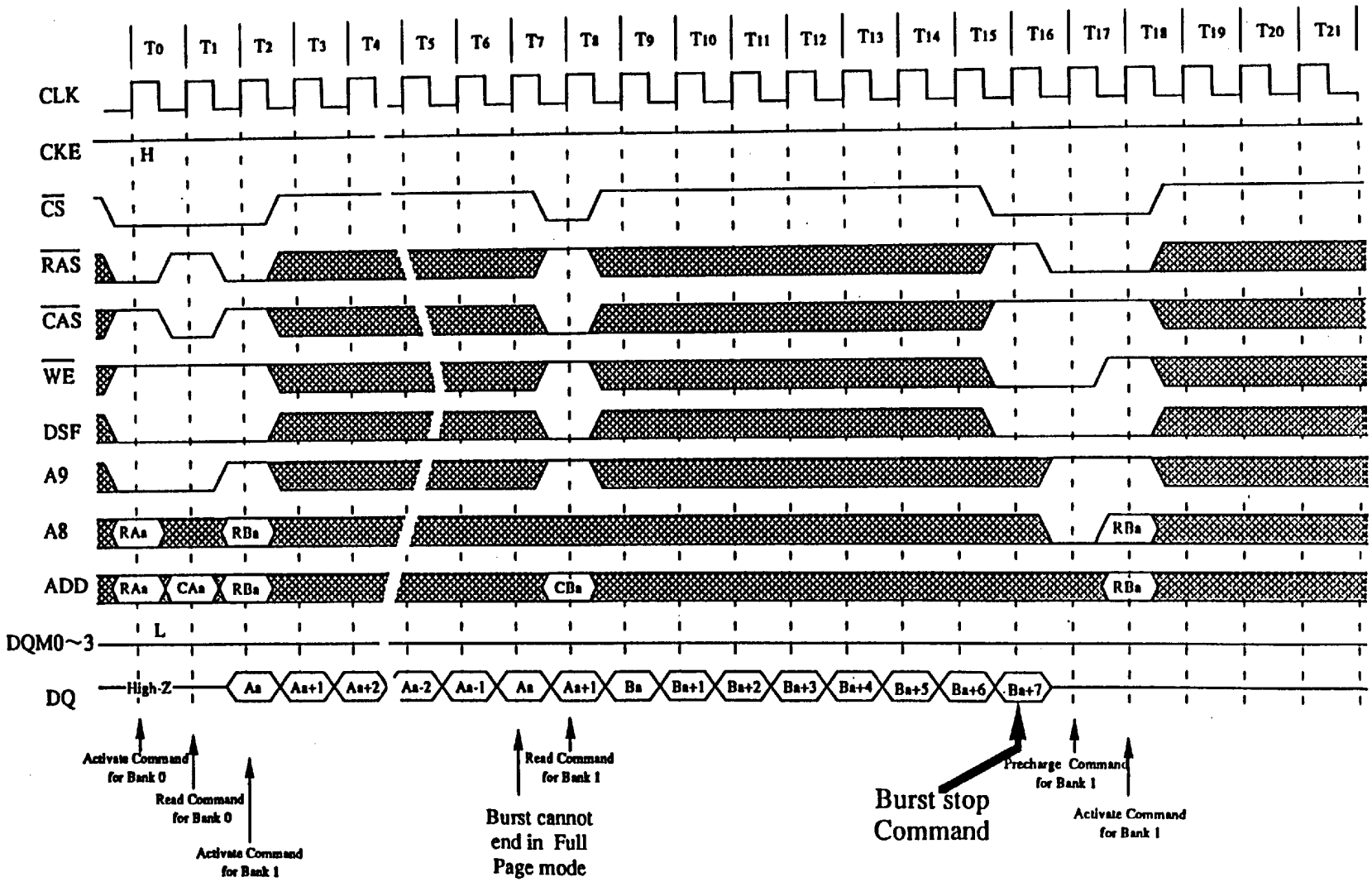
Auto Precharge after Write Burst

Burst Length = 4 CAS Latency = 3



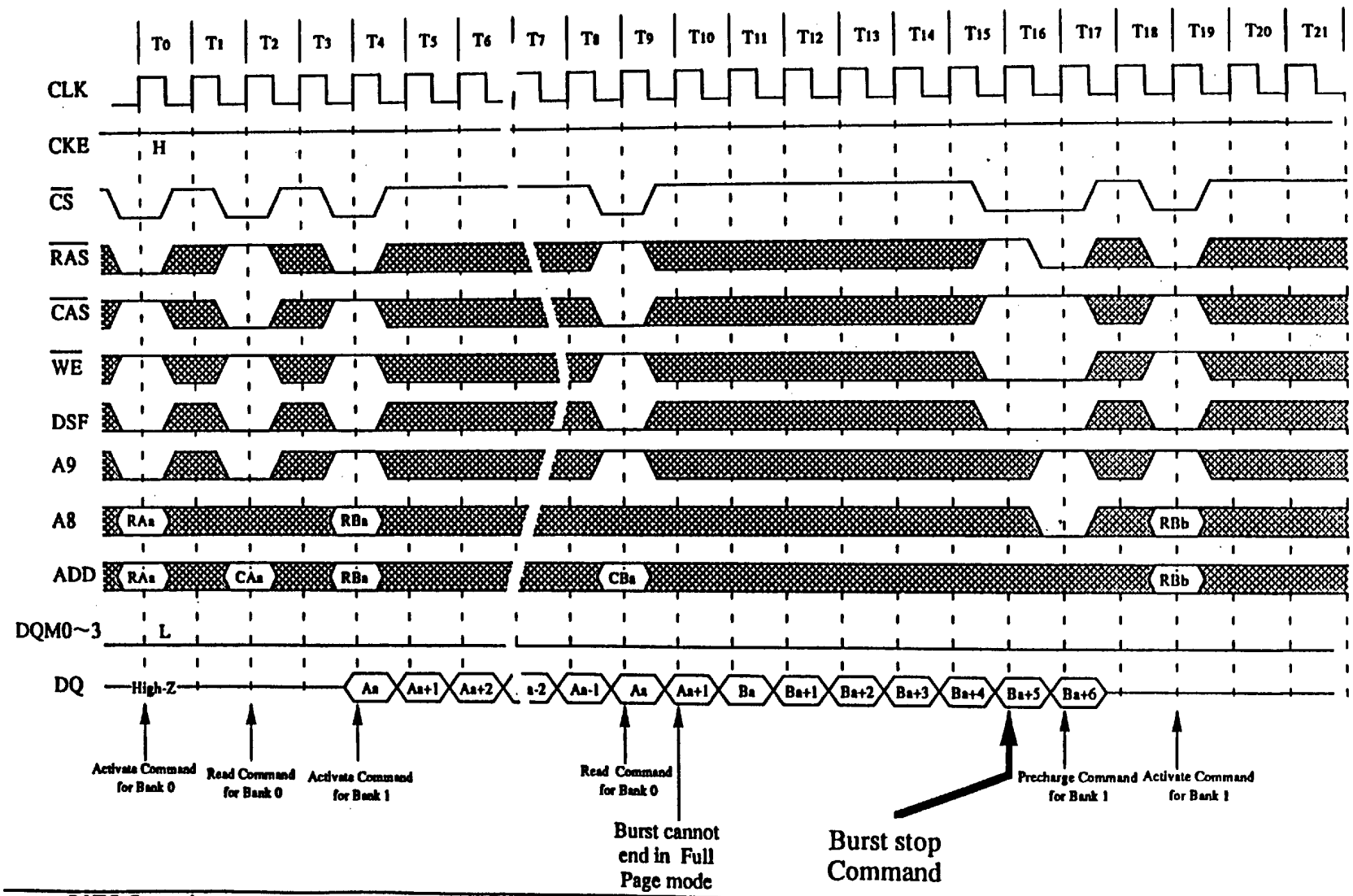
Full Page READ CYCLE

CAS Latency = 1



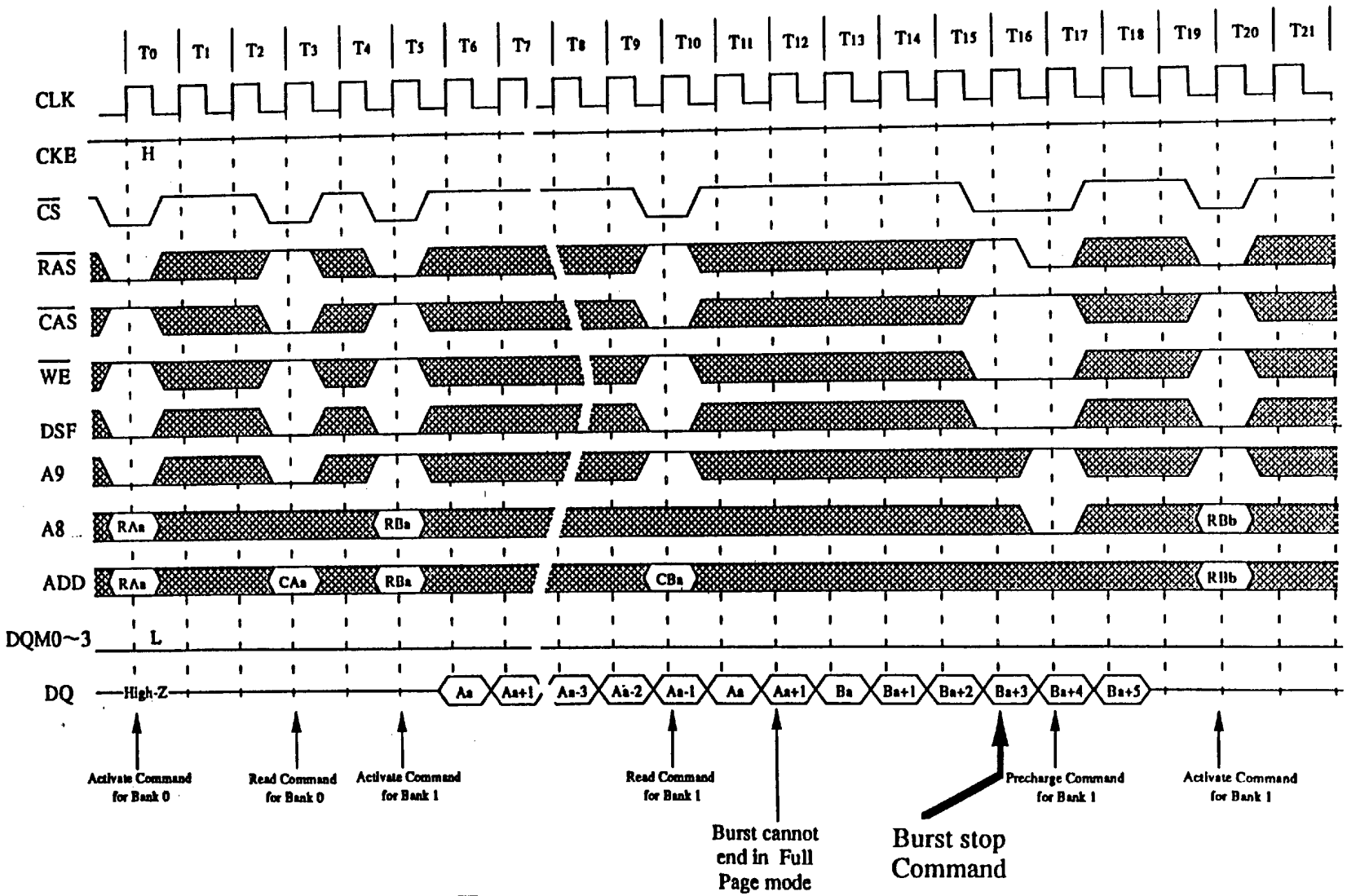
Full Page READ CYCLE

CAS Latency = 2



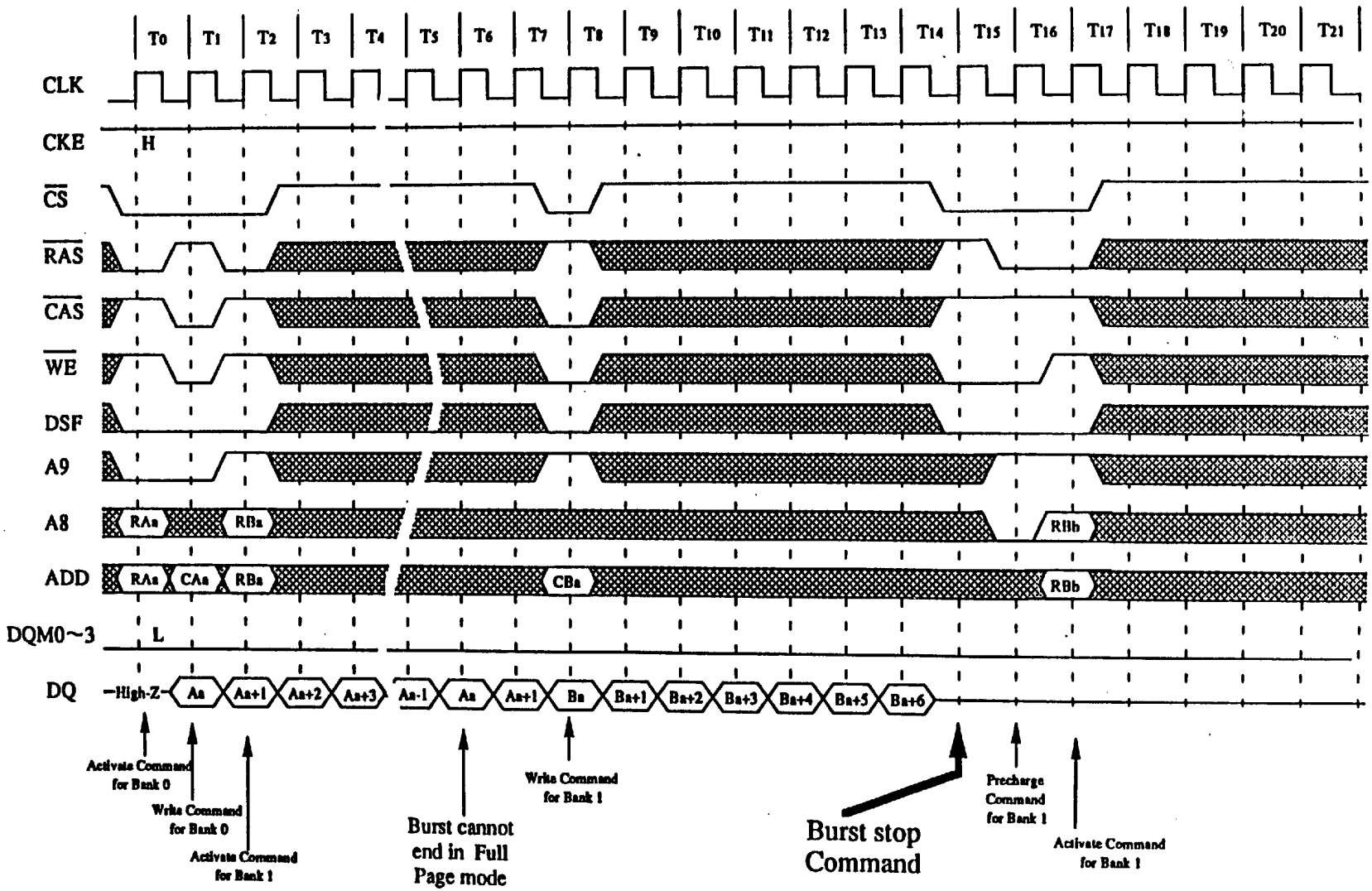
Full Page READ CYCLE

CAS Latency = 3



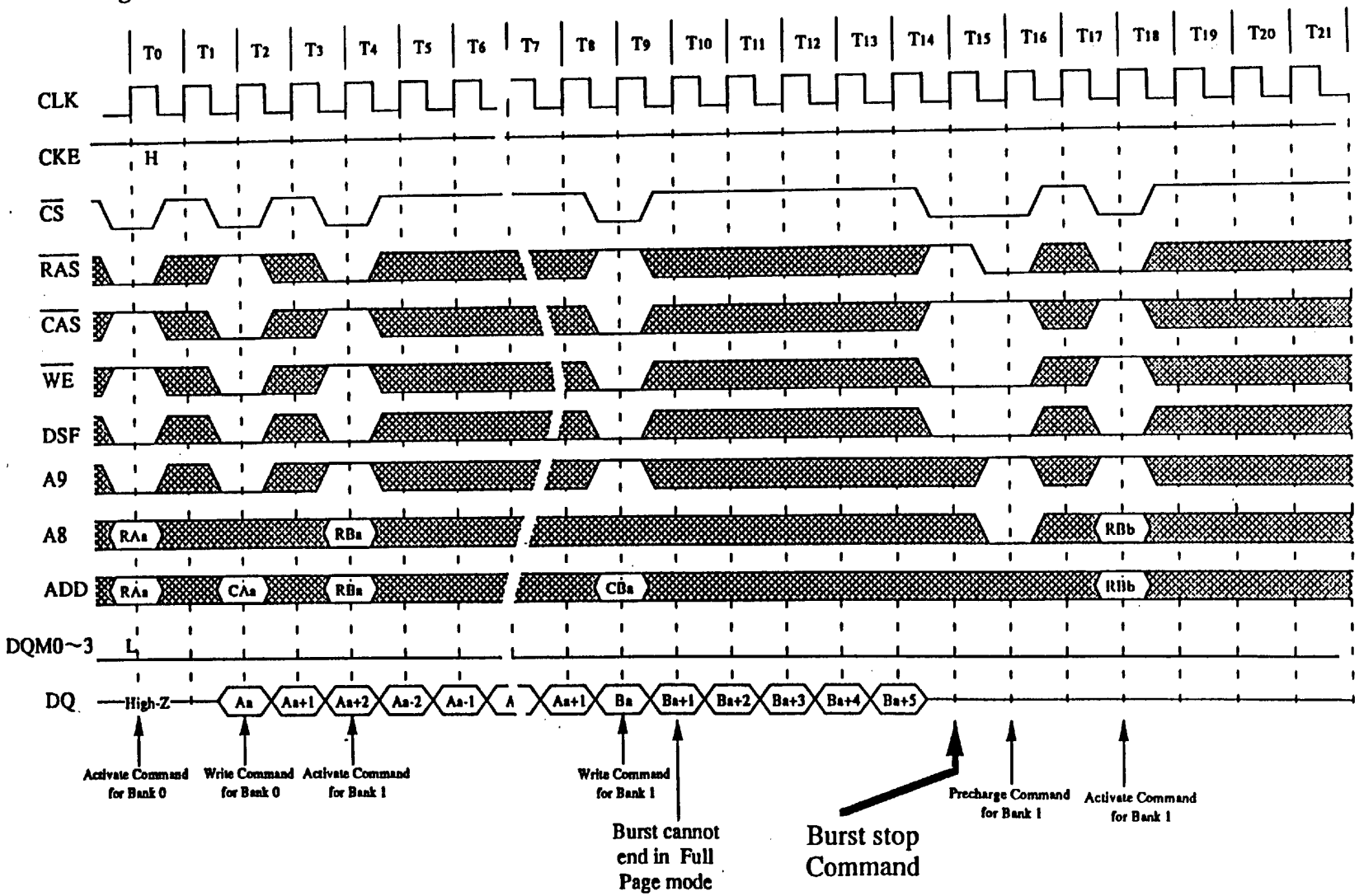
Full Page WRITE CYCLE

CAS Latency = 1



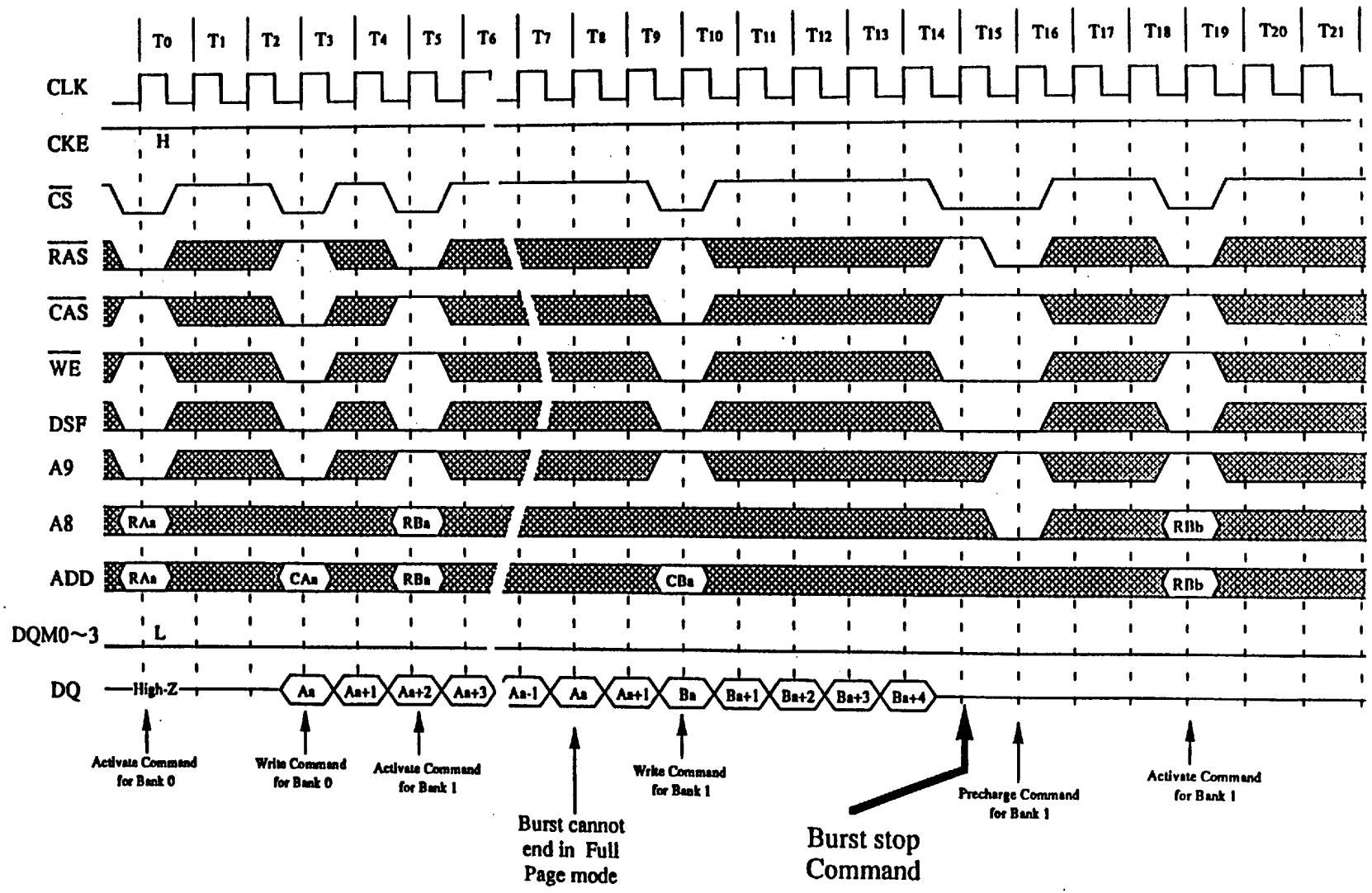
Full Page WRITE CYCLE

CAS Latency = 2



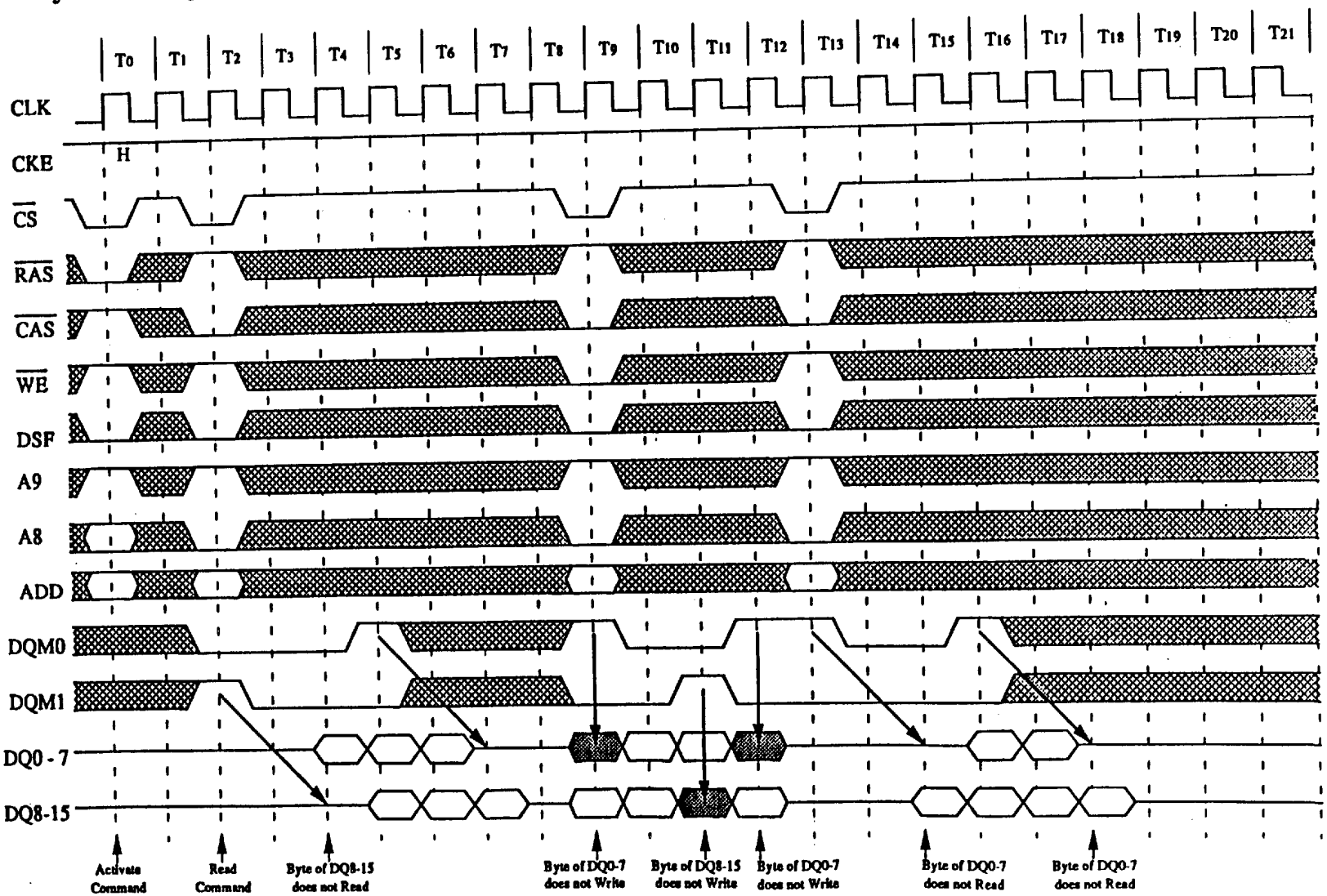
Full Page WRITE CYCLE

CAS Latency = 3



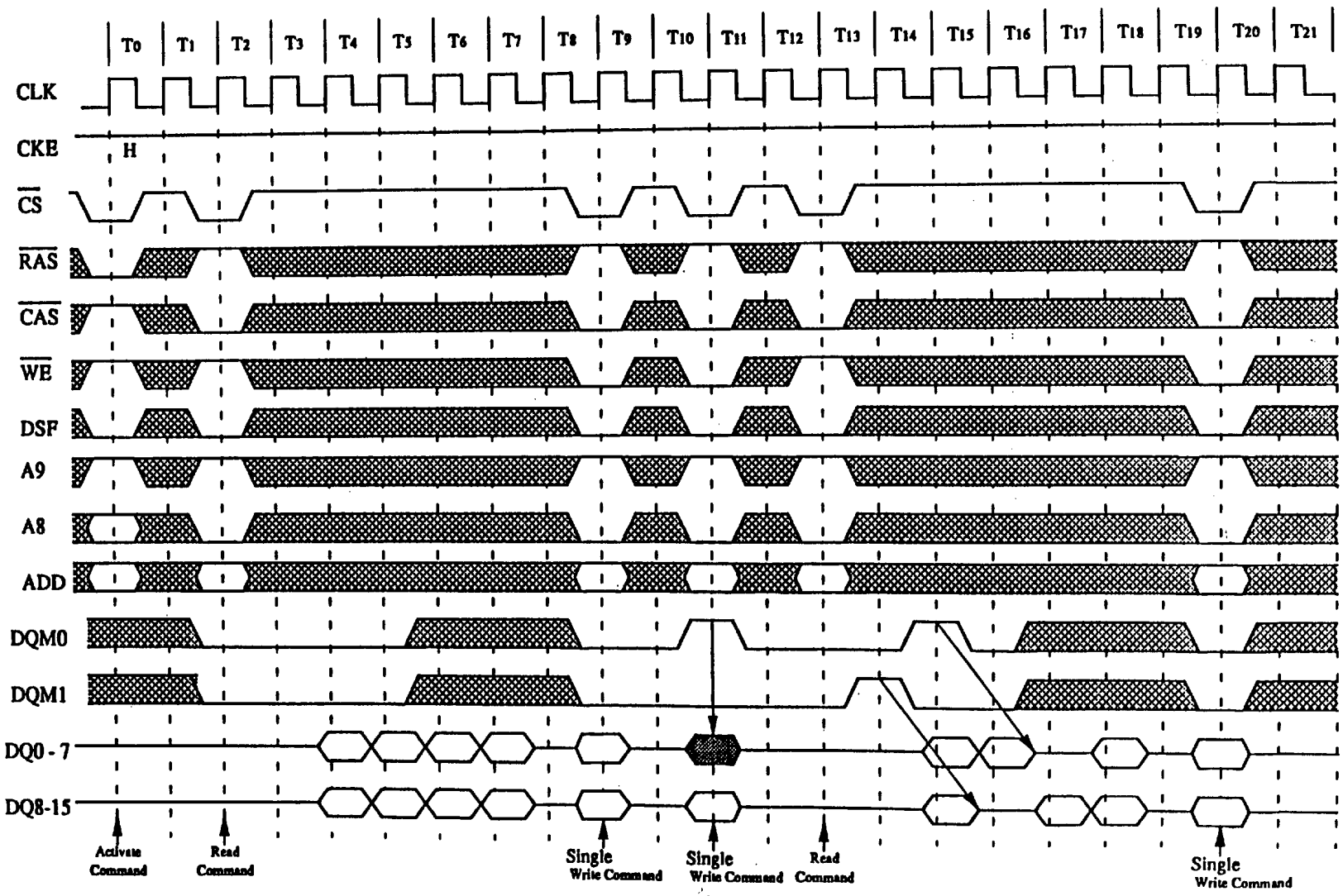
Byte Write Operation

Burst Length = 4 CAS Latency = 2



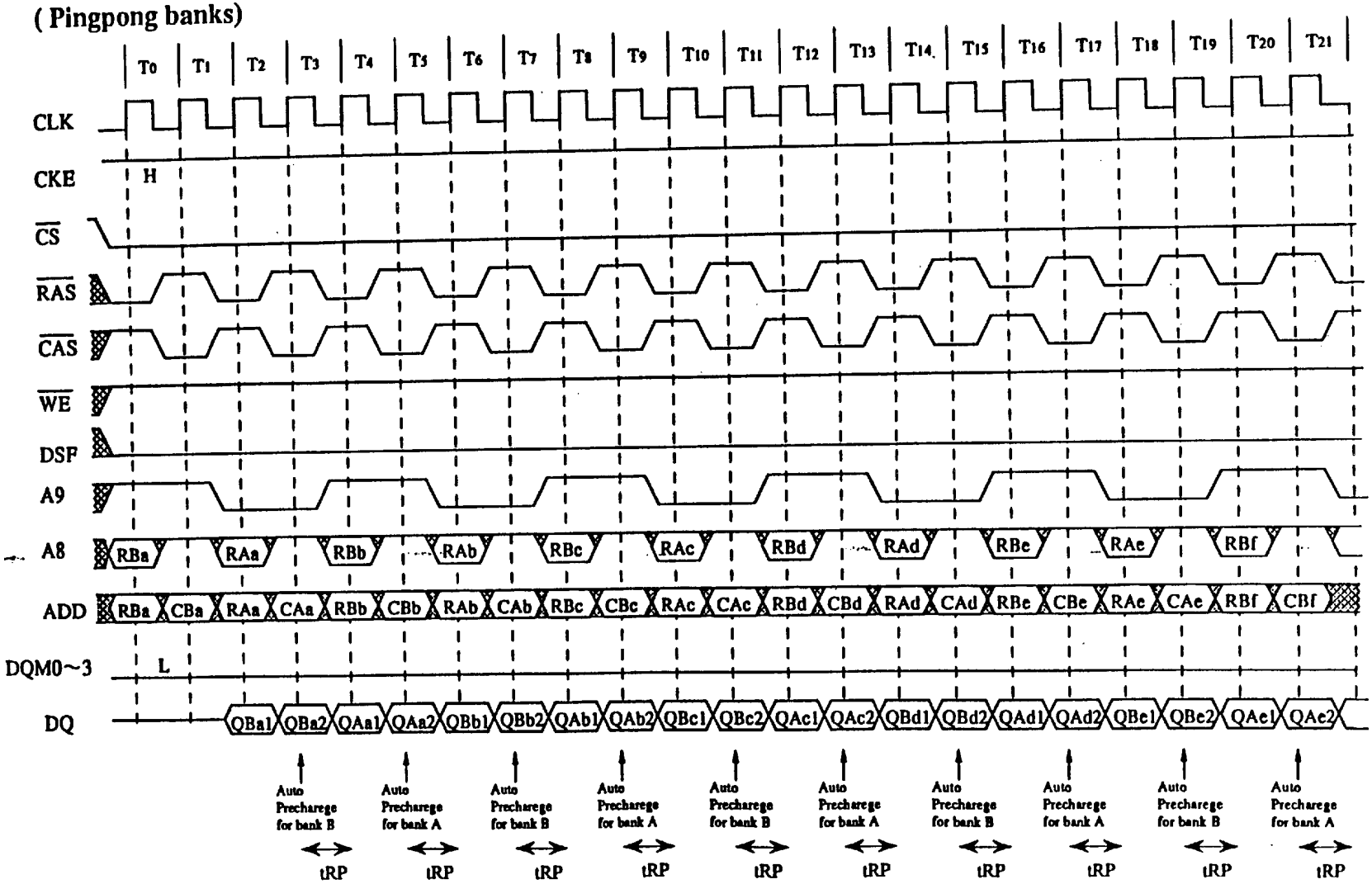
Burst Read and Single Write

Burst Length = 4 CAS Latency = 2



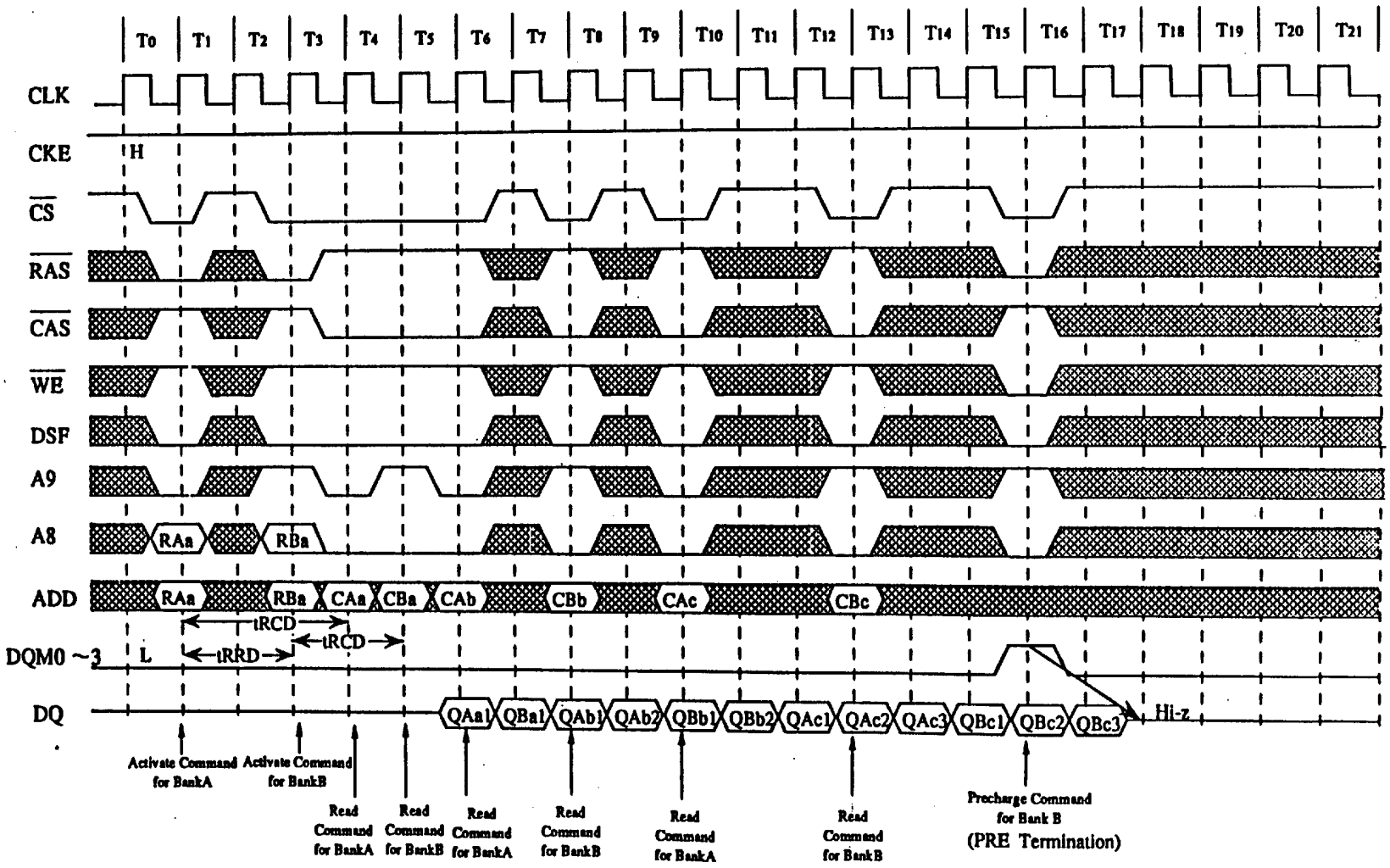
Random Row READ
(Pingpong banks)

Burst Length = 2 CAS Latency = 1



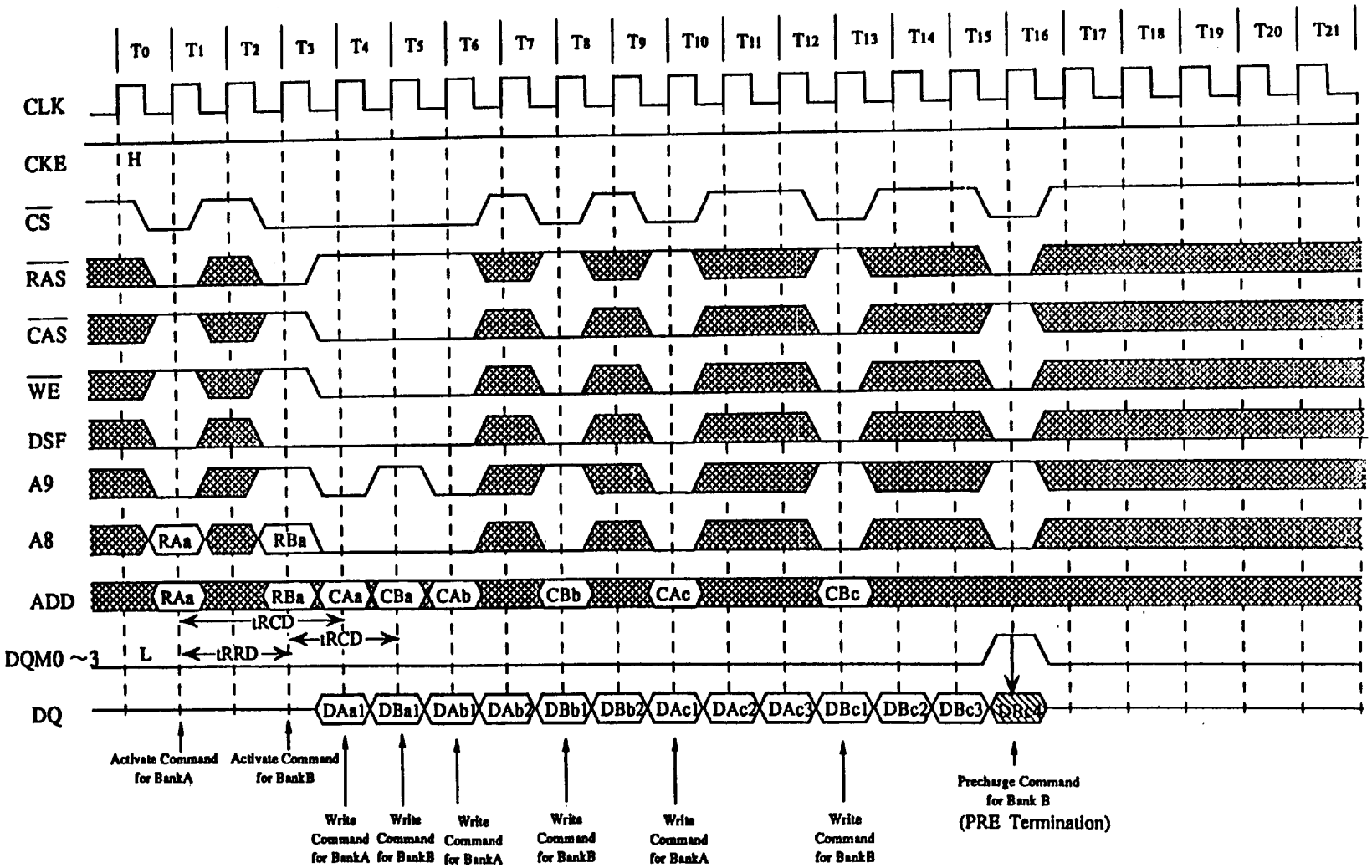
Full Page Random Column Read

Burst Length= Full Page CAS Latency = 2



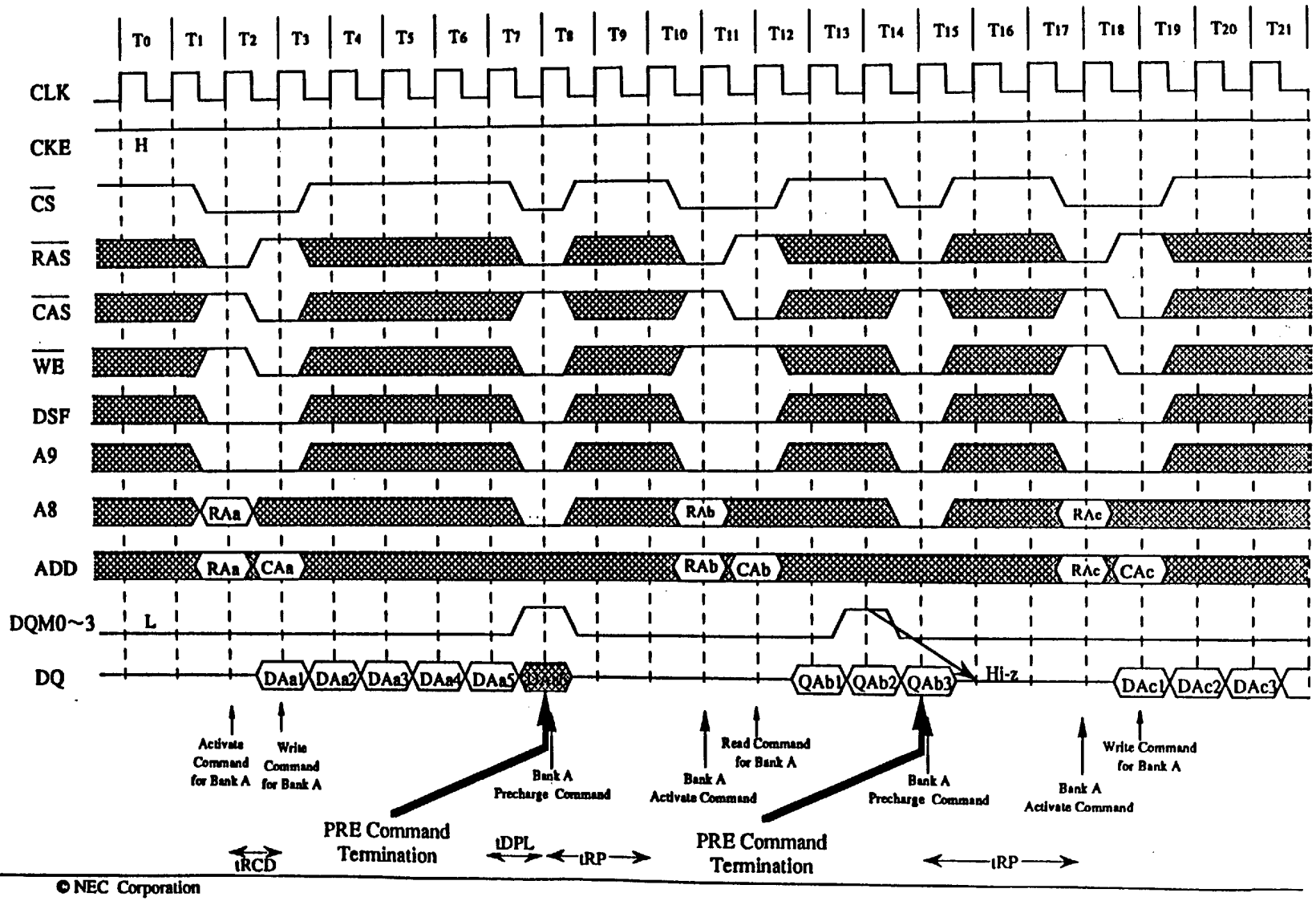
Full Page Random Column Write

Burst Length= Full Page CAS Latency = 2



PRE(Precharge)Termination of Burst

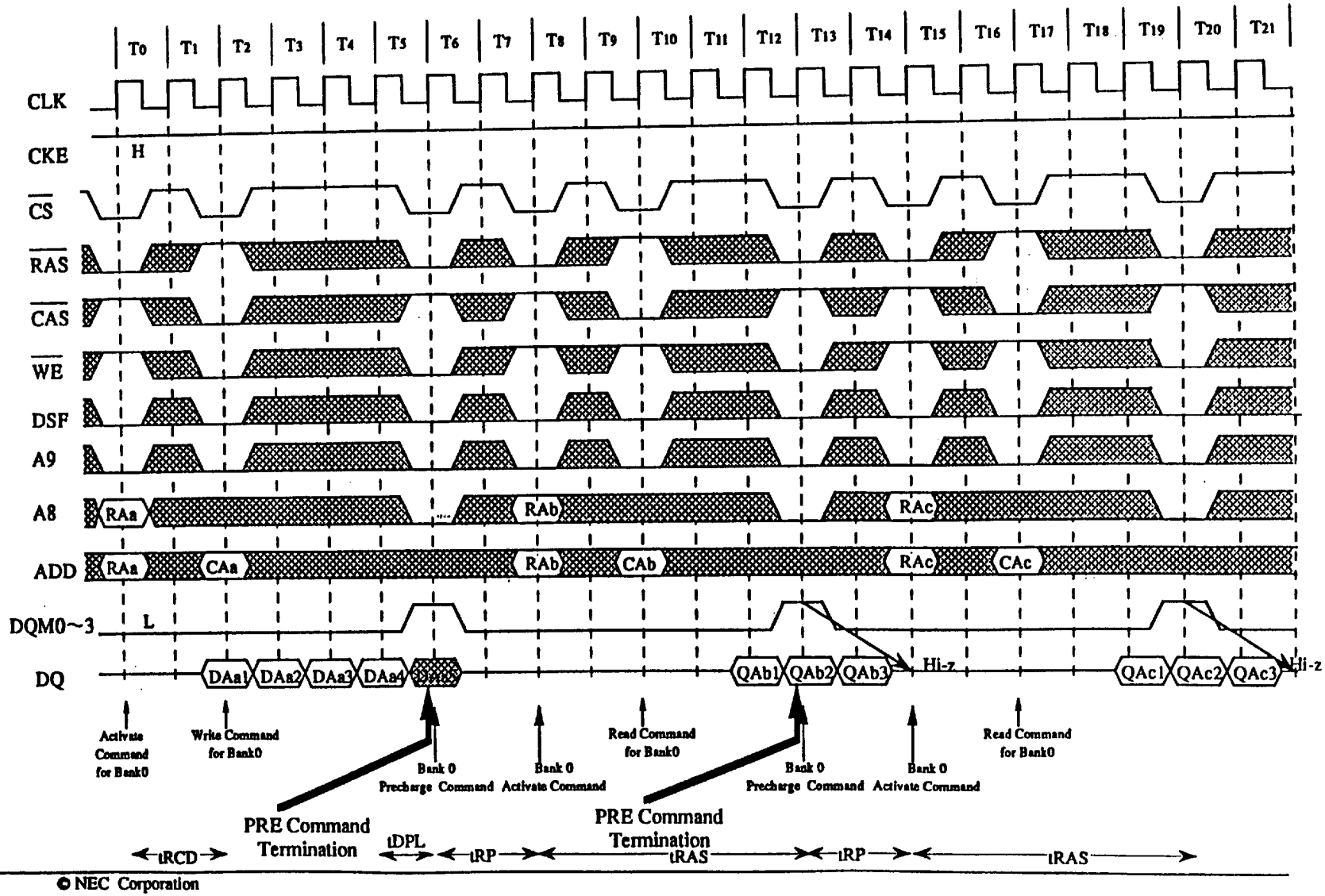
Burst Length = 2,4,8,FULL CAS Latency = 1



NON JEDEC STANDARD

PRE(Precharge)Termination of Burst

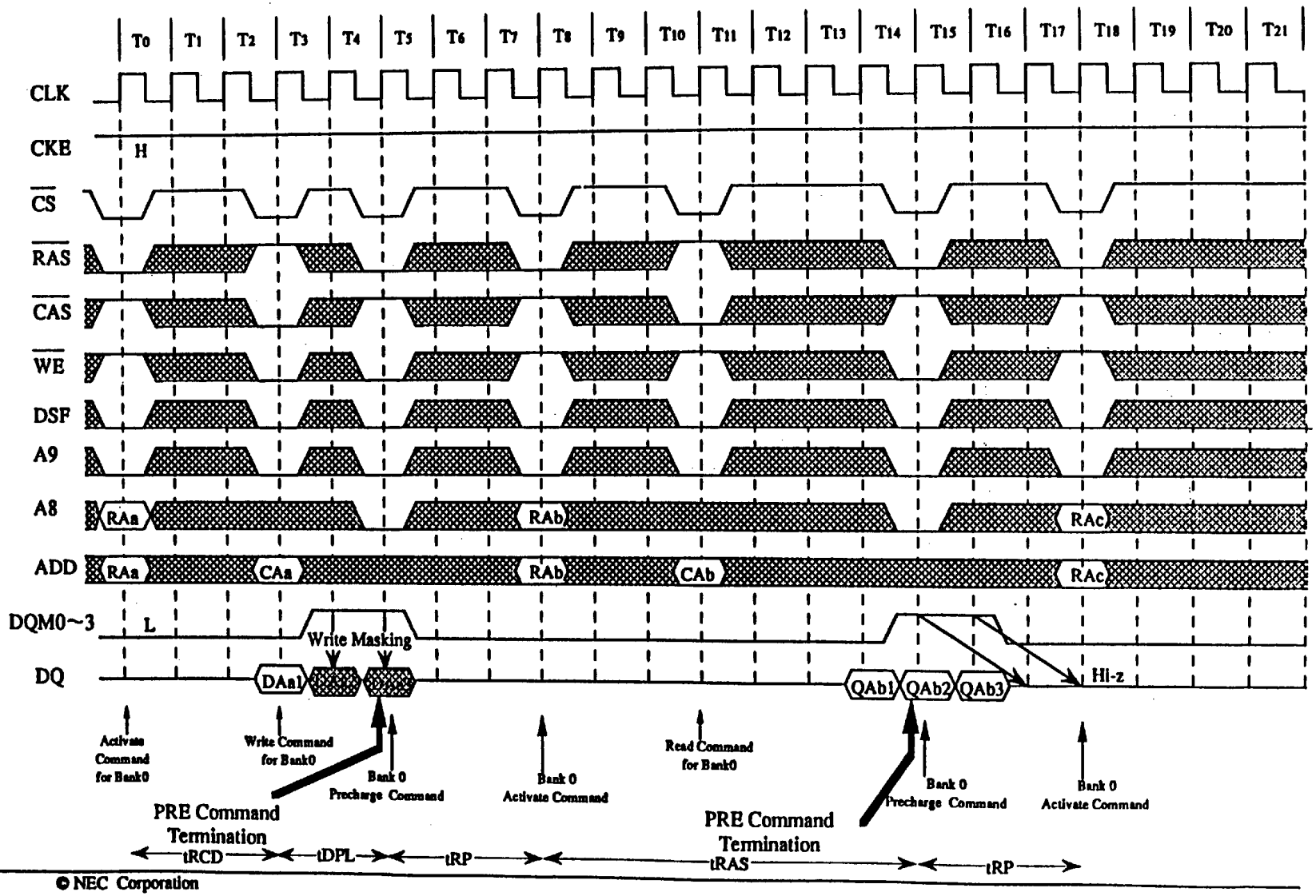
Burst Length = 2,4,8,FULL CAS Latency = 2



NON JEDEC STANDARD

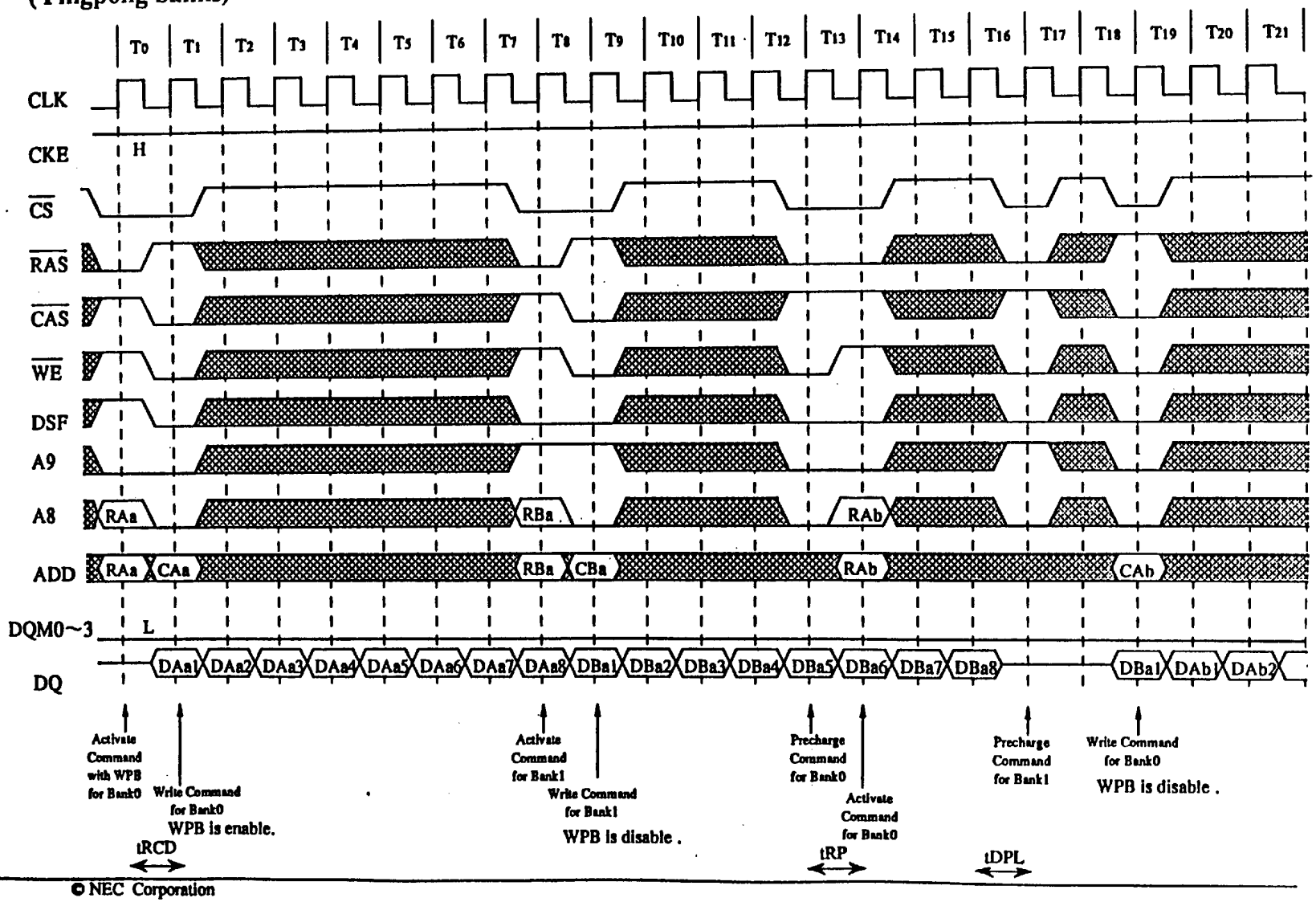
PRE(Precharge)Termination of Burst

Burst Length = 2,4,8,FULL CAS Latency = 3



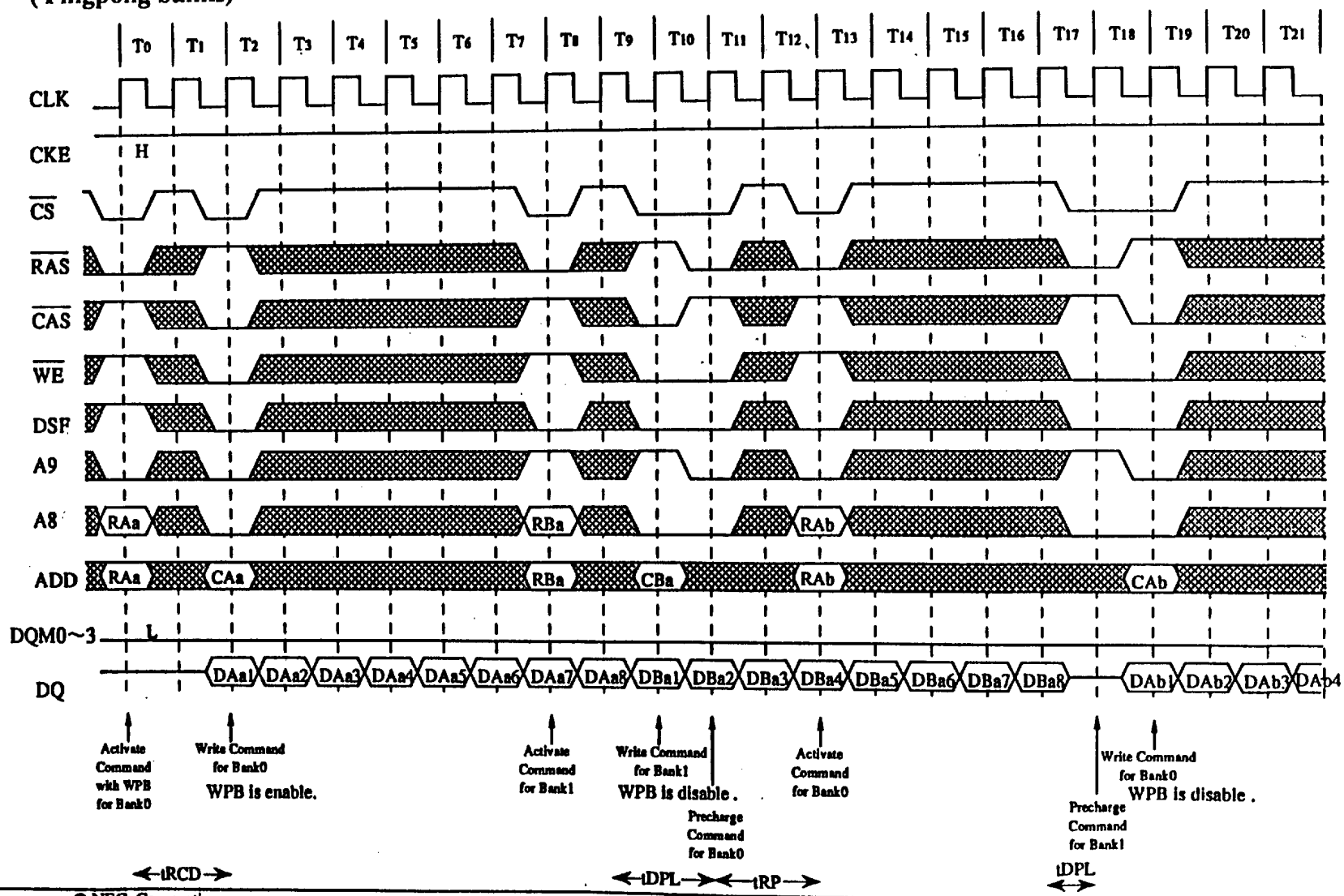
Random Row Write with WPB
(Pingpong banks)

Burst Length = 8 CAS Latency = 1



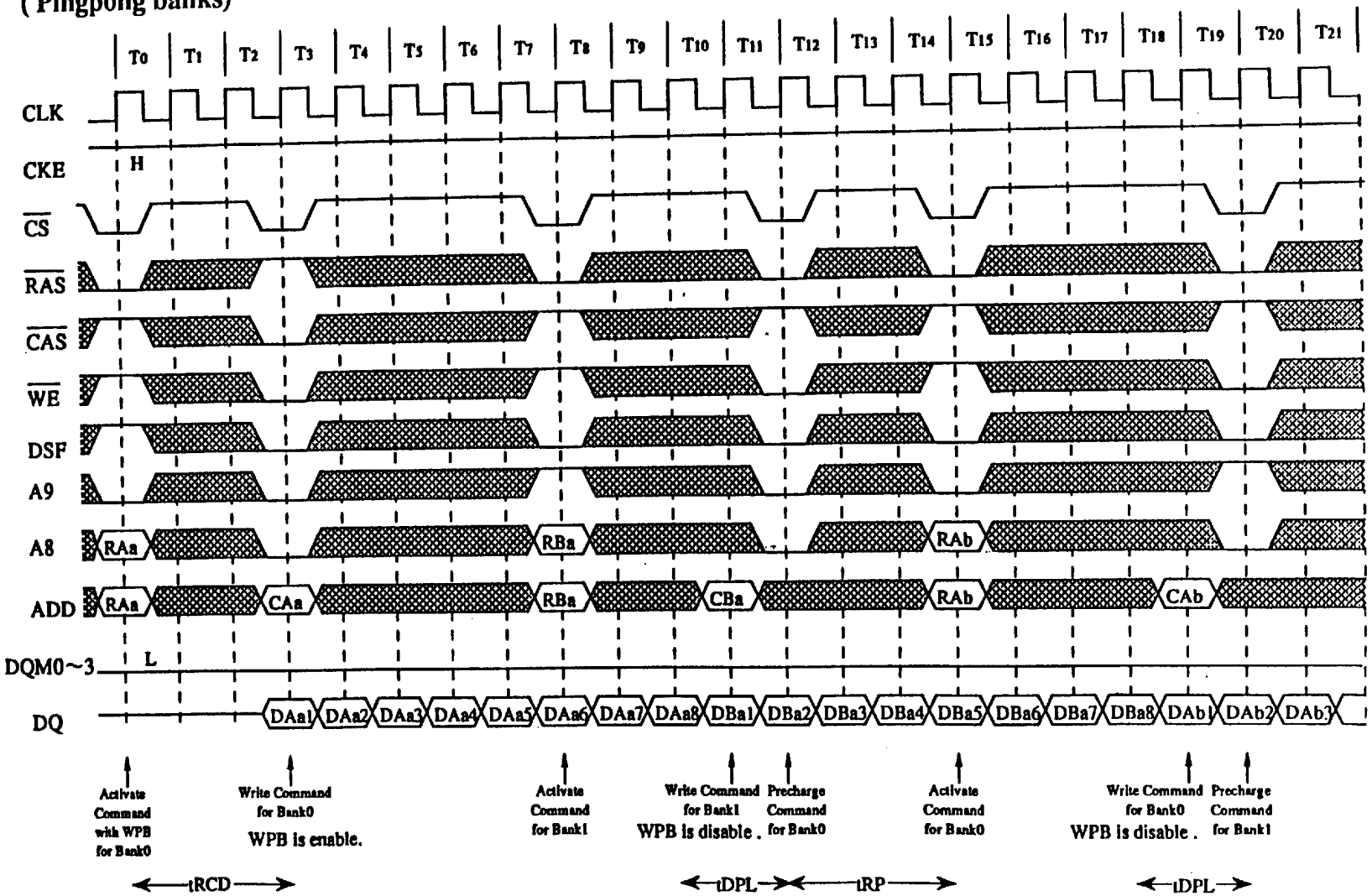
Random Row Write with WPB
(Pingpong banks)

Burst Length = 8 CAS Latency = 2



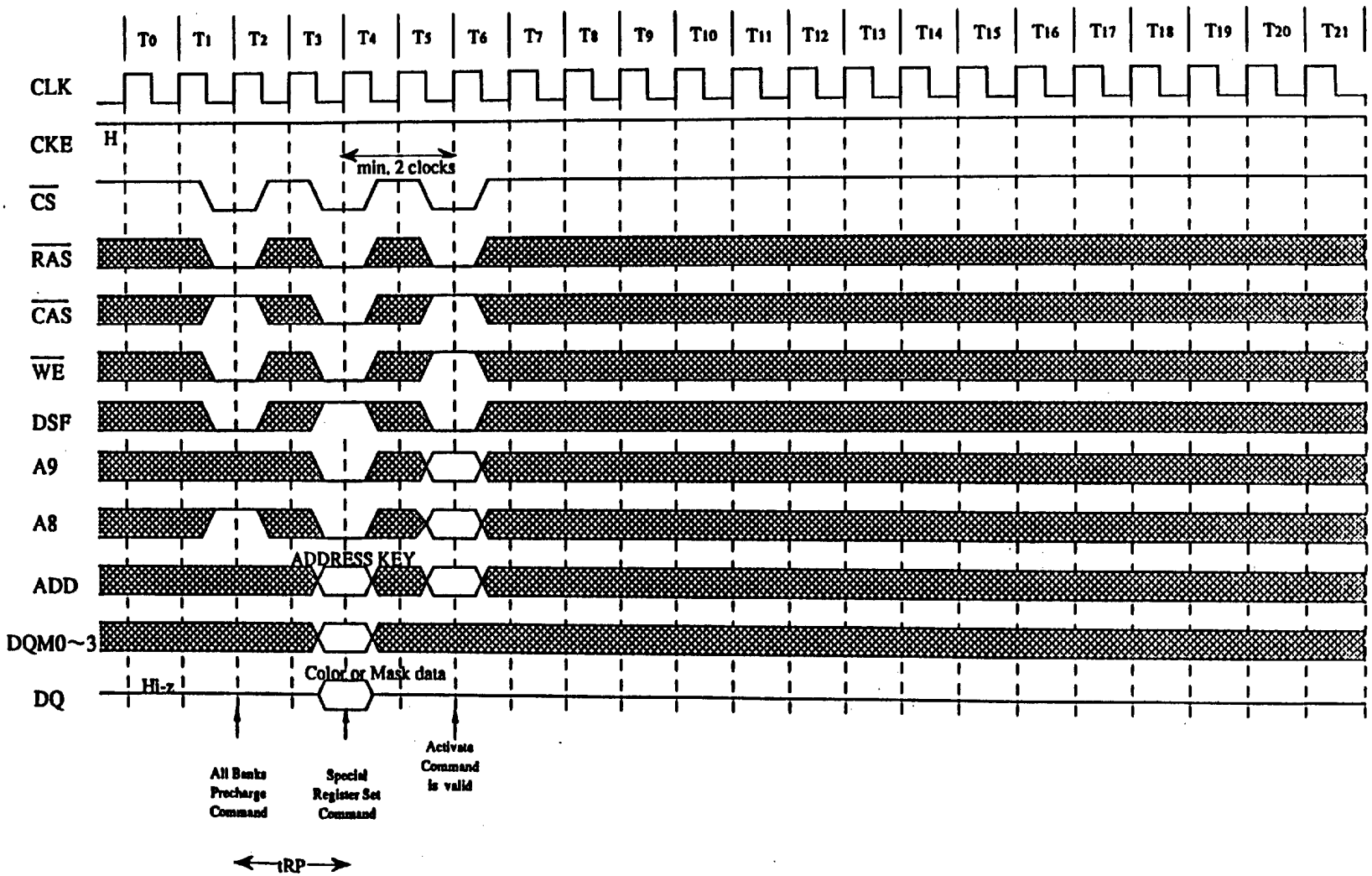
Random Row Write with WPB
(Pingpong banks)

Burst Length = 8 CAS Latency = 3



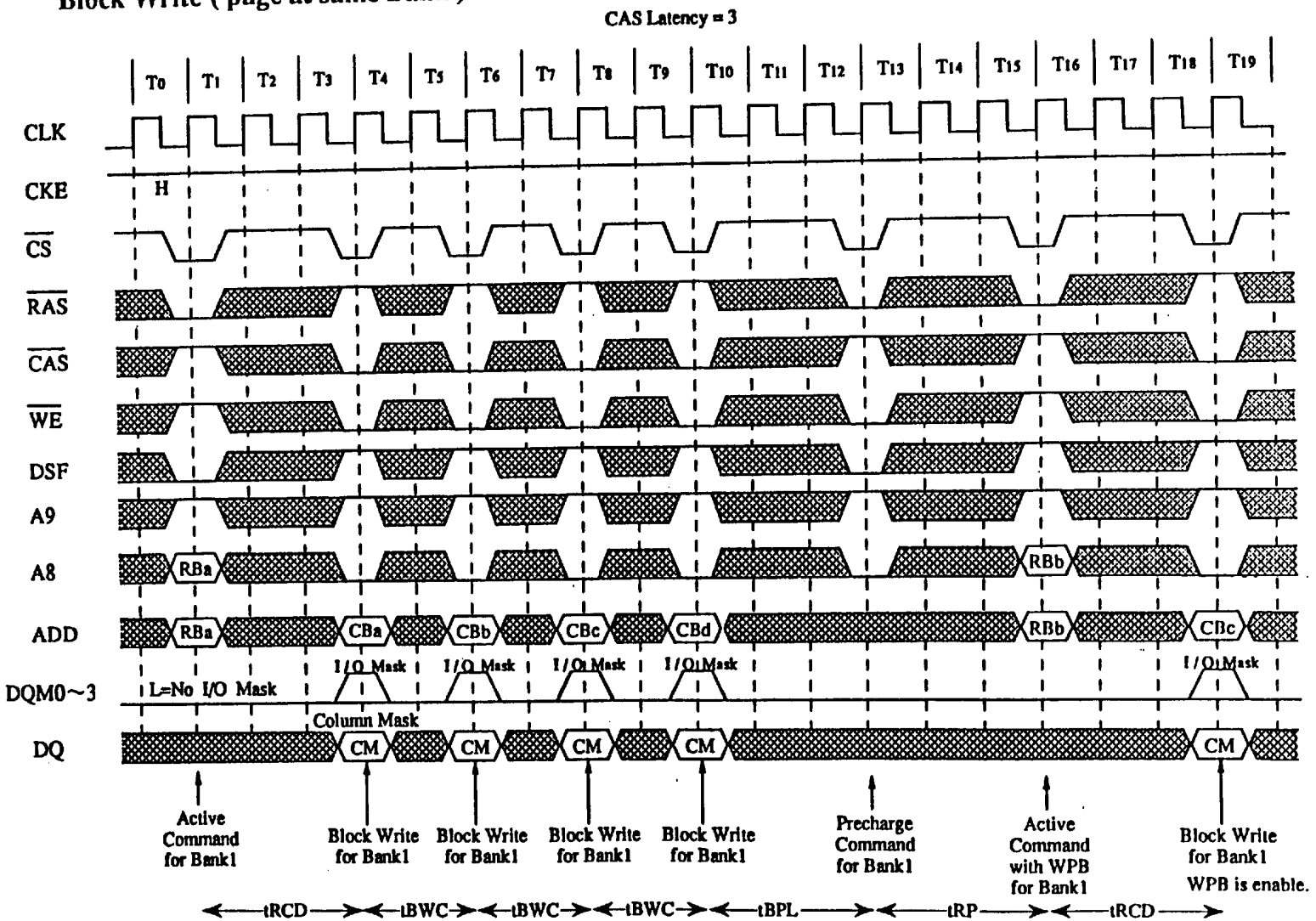
Special Register Set

Burst Length = 4 CAS Latency = 2

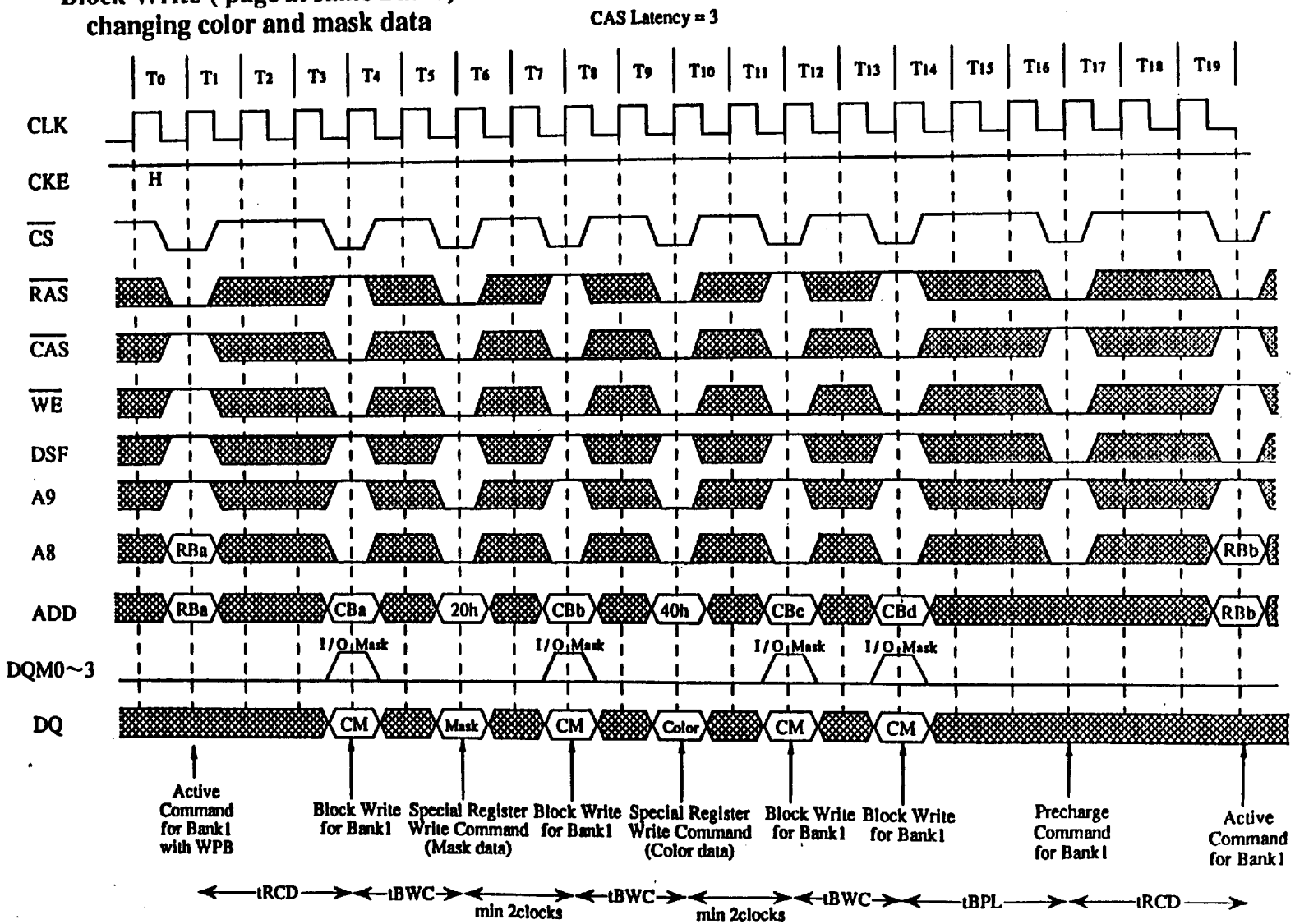


Note) Special Register Set command is able to input at any state.

Block Write (page at same Bank)



Block Write (page at same Bank) changing color and mask data



Interleaved Block Write

CAS Latency = 3