CY93422A/93L422A
CY93422/93L422

CYPRESS SEMICONDUCTOR

256 x 4 Static R/W RAM

Features

- **256 x 4 static RAM for control stores in high-speed computers**
- **Processed with high-speed CMOS for optimum speed/power**
- **Separate inputs and outputs**
- **Low power**
  - **— Standard power: 660 mW (commercial) 715 mW (military**
  - **— Low power: 440 mW (commercial) 495 mW (military)**
- **5-volt power supply ±10% tolerance both commercial and military**
- **Capable of withstanding greater than 2001V static discharge**

Functional Description

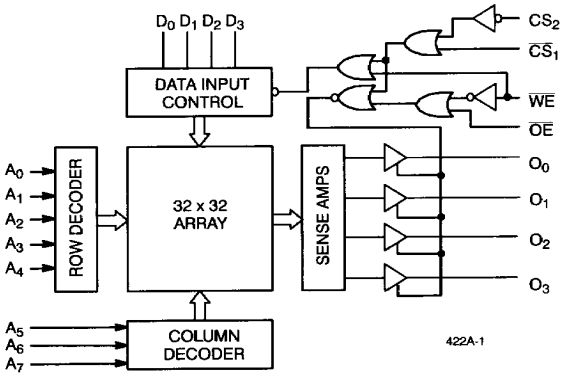
The CY93422 is a high-performance CMOS static RAM organized as 256 by 4 bits. Easy memory expansion is provided by an active LOW chip select one ($\overline{CS_1}$) input, an active HIGH chip select two (CS_2) input, and three-state outputs.

An active LOW write enable input ($\overline{WE}$) controls the writing/reading operation of the memory. When the chip select one ($\overline{CS_1}$) and write enable ($\overline{WE}$) inputs are LOW and the chip select two (CS_2) input is HIGH, the information on the four data inputs (D_0 to D_3) is written into the addressed memory word and the output circuitry is preconditioned so that the correct data is present at the outputs when the write cycle is complete. This preconditioning operation insures minimum write recovery times by eliminating the "write recovery glitch."

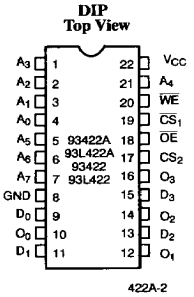
Reading is performed with the chip select one ($\overline{CS_1}$) input LOW, the chip select two input (CS_2) and write enable ($\overline{WE}$) inputs HIGH, and the output enable input ($\overline{OE}$) LOW. The information stored in the addressed word is read out on the four non-inverting outputs (O_0 to O_3).

The outputs of the memory go to an active high-impedance state whenever chip select one ($\overline{CS_1}$) is HIGH, chip select two (CS_2) is LOW, output enable ($\overline{OE}$) is HIGH, or during the writing operation when write enable ($\overline{WE}$) is LOW.

Logic Block Diagram



Pin Configuration



Selection Guide (For higher performance and lower power, refer to the CY7C122 data sheet.)

		93422A	93L422A	93422	93L422
Maximum Access Time (ns)	Commercial	35	45	45	60
	Military	45	55	60	75
Maximum Operating Current (mA)	Commercial	120	80	120	80
	Military	130	90	130	90

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage to Ground Potential (Pin 22 to Pin 8) ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Output State ..... − 0.5V to +V_{CC} Max.

DC Input Voltage ..... − 0.5V to + 5.5V

Output Current into Outputs (Low) ..... 20 mA

DC Input Current ..... − 30 mA to +5.0 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 75°C	5V ± 10%
Military[1]	− 55°C to + 125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

Parameters	Description	Test Conditions		93422 93422A Min.	93422 93422A Max.	93L422 93L422A Min.	93L422 93L422A Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 5.2 mA		2.4		2.4		V
V_{OL}	Output LOW Current	V_{CC} = Min., I_{OL} = 8.0 mA			0.45		0.45	V
V_{IH}	Input HIGH Level[3]	Guaranteed Input Logical HIGH Voltage for all Inputs		2.1		2.1		V
V_{IL}	Input LOW Level[3]	Guaranteed Input Logical LOW Voltage for all Inputs			0.8		0.8	V
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.4V			− 300		− 300	µA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 4.5V			40		40	µA
I_{SC}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = 0.0V			− 90		− 90	mA
I_{CC}	Power Supply Current	All Inputs = GND, V_{CC} = Max.	T_A = 125°C		110		70	mA
			T_A = 75°C		110		70	
			T_A = 0°C		120		80	
			T_A = − 55°C		130		90	
V_{CL}	Input Clamp Voltage			See Note 5		See Note 5		
I_{CEX}	Output Leakage Current	V_{OUT} = 2.4V			50		50	µA
		V_{OUT} = 0.5V, V_{CC} = Max.		− 50		− 50		

Capacitance[6]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	8	pF
C_{OUT}	Output Capacitance		8	pF

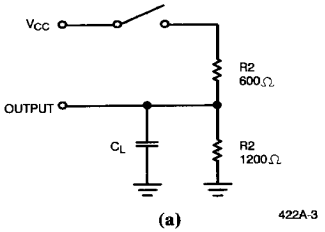
Function Table[7]

Inputs $\overline{CS_2}$	Inputs $\overline{CS_1}$	Inputs $\overline{WE}$	Inputs $\overline{OE}$	Inputs D_n	Outputs O_n	Mode
L	X	X	X	X	High Z	Not Selected
X	H	X	X	X	High Z	Not Selected
H	L	H	H	X	High Z	Output Disable
H	L	H	L	X	Selected Data	Read Data
H	L	L	X	L	High Z	Write "0"
H	L	L	X	H	High Z	Write "1"

Notes:

1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

AC Test Loads and Waveforms



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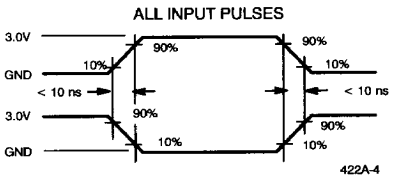

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Commercial Switching Characteristics Over the Operating Range[8, 9]

Parameters	Description	93422A		93L422A		93422		93L422		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$t_{PLH(A)}$[10] $t_{PHL(A)}$	Delay from Address to Output (Address Access Time)		35		45		45		60	ns
t_{PZH} ($\overline{CS_1}$, CS_2) t_{PZH} ($\overline{CS_1}$, CS_2)	Delay from Chip Select to Active Output and Correct Data		25		30		30		35	ns
t_{PZH} ($\overline{WE}$) t_{PZL} ($\overline{WE}$)	Delay from Write Enable to Active Output and Correct Data (Write Recovery)		25		40		40		45	ns
t_{PZH} ($\overline{OE}$) t_{PZL} ($\overline{OE}$)	Delay from Output Enable to Active Output and Correct Data		25		30		30		35	ns
t_S (A)	Set-Up Time Address (Prior to Initiation of Write)	5		5		10		5		ns
t_h (A)	Hold Time Address (After Termination of Write)	5		5		5		5		ns
t_S (DI)	Set-Up Time Data Input (Prior to Initiation of Write)	5		5		5		5		ns
t_h (DI)	Hold Time Data Input (After Termination of Write)	5		5		5		5		ns
t_S ($\overline{CS_1}$, CS_2)	Set-Up Time Chip Select (Prior to Initiation of Write)	5		5		5		5		ns
t_h ($\overline{CS_1}$, CS_2)	Hold Time Chip Select (After Termination of Write)	5		5		5		5		ns
t_{pw} ($\overline{WE}$)	Minimum Write Enable Pulse Width to Insure Write	20		40		30		45		ns
t_{PHZ} ($\overline{CS_1}$, CS_2) t_{PLZ} ($\overline{CS_1}$, CS_2)	Delay from Chip Select to Inactive Output (High Z)		30		40		30		45	ns
t_{PHZ} ($\overline{WE}$) t_{PLZ} ($\overline{WE}$)	Delay from Write Enable to Inactive Output (High Z)		30		40		30		45	ns
t_{PHZ} ($\overline{OE}$) t_{PLZ} ($\overline{OE}$)	Delay from Output Enable to Inactive Output (High Z)		30		40		30		45	ns

Military Switching Characteristics Over the Operating Range[8, 9]

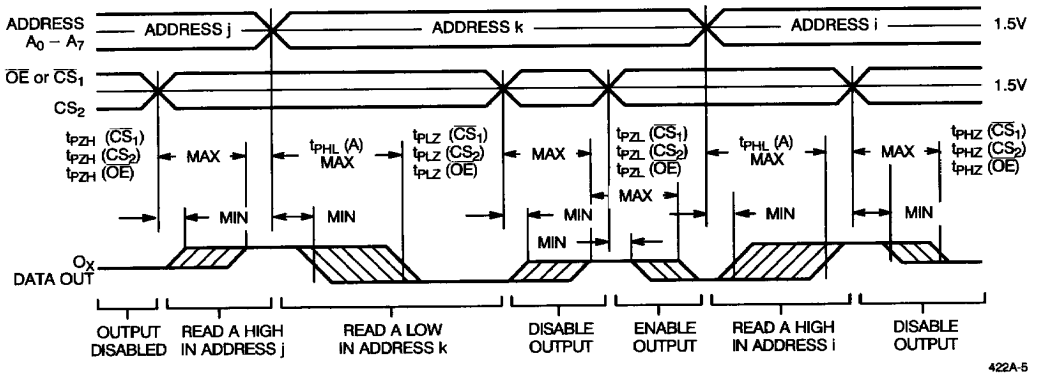
Parameters	Description	93422A		93L422A		93422		93L422		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$t_{PLH(A)}$[10] $t_{PHL(A)}$	Delay from Address to Output (Address Access Time)		45		55		60		75	ns
t_{PZH} ($\overline{CS_1}$, CS_2) t_{PZL} ($\overline{CS_1}$, CS_2)	Delay from Chip Select to Active Output and Correct Data		35		40		45		45	ns
t_{PZH} ($\overline{WE}$) t_{PZL} ($\overline{WE}$)	Delay from Write Enable to Active Output and Correct Data (Write Recovery)		40		45		50		50	ns
t_{PZH} ($\overline{OE}$) t_{PZL} ($\overline{OE}$)	Delay from Output Enable to Active Output and Correct Data		35		40		45		45	ns
t_S (A)	Set-Up Time Address (Prior to Initiation of Write)	5		10		10		10		ns
t_h (A)	Hold Time Address (After Termination of Write)	5		5		5		10		ns
t_S (DI)	Set-Up Time Data Input (Prior to Initiation of Write)	5		5		5		5		ns
t_h (DI)	Hold Time Data Input (After Termination of Write)	5		5		5		5		ns
t_S ($\overline{CS_1}$, CS_2)	Set-Up Time Chip Select (Prior to Initiation of Write)	5		5		5		5		ns
t_h ($\overline{CS_1}$, CS_2)	Hold Time Chip Select (After Termination of Write)	5		5		5		10		ns
t_{ph} ($\overline{WE}$)	Minimum Write Enable Pulse Width to Insure Write	35		40		40		45		ns
t_{PHZ} ($\overline{CS_1}$, CS_2) t_{PLZ} ($\overline{CS_1}$, CS_2)	Delay from Chip Select to Inactive Output (High Z)		35		40		45		45	ns
t_{PHZ} ($\overline{WE}$) t_{PLZ} ($\overline{WE}$)	Delay from Write Enable to Inactive Output (High Z)		40		40		45		45	ns
t_{PHZ} ($\overline{OE}$) t_{PLZ} ($\overline{OE}$)	Delay from Output Enable to Inactive Output (High Z)		35		40		45		45	ns

Notes:

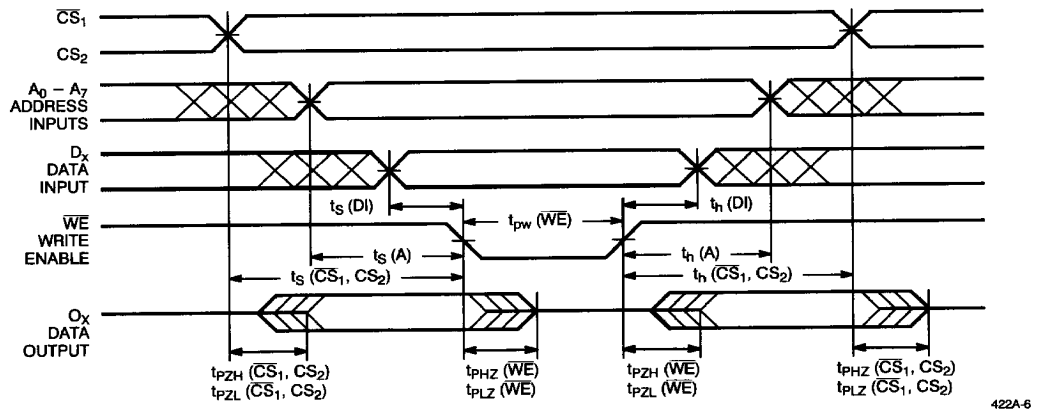
4. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
5. The CMOS process does not provide a clamp diode. However, the CY93422 is insensitive to −3V DC input levels and −5V undershoot pulses of less than 10 ns (measured at 50% point).
6. Tested initially and after any design or process changes that may affect these parameters.
7. H = High Voltage Level, L = Low Voltage Level, X = Don't Care. High Z implies outputs are disabled or off. This condition is defined as a high-impedance state for the CY93422.
8. V_{CC} = 5V ± 10% and T_A = 0°C to + 75°C unless otherwise noted.
9. t_{PZH} ($\overline{WE}$), t_{PZH} ($\overline{CS_1}$, CS_2), and t_{PZH} ($\overline{OE}$) are measured with S_1 open, C_L = 15 pF, and with both the input and output timing referenced to 1.5V. t_{PZL} ($\overline{WE}$), t_{PZL} ($\overline{CS_1}$, CS_2), and t_{PZL} ($\overline{OE}$) are measured with S_1 closed, C_L = 15 pF, and with both the input and output timing referenced to 1.5V. t_{PHZ} ($\overline{WE}$). t_{PHZ} ($\overline{CS_1}$, CS_2), and t_{PHZ} ($\overline{OE}$) are measured with S_1 open, C_L < 5 pF, and are measured between the 1.5V level on the input to the V_{OH} − 500 mV level on the output. t_{PLZ} ($\overline{WE}$), t_{PLZ} ($\overline{CS_1}$, CS_2), and t_{PLZ} ($\overline{OE}$) are measured with S_1 closed and C_L < 5 pF, and are measured between the 1.5V level on the input and the V_{OL} +500 mV level on the output.
10. $t_{PLH(A)}$ and $t_{PHL(A)}$ are tested with S_1 closed and C_L = 15 pF with both input and output timing referenced to 1.5V.
11. Switching delays from the address, output enable, and chip select inputs to the data output. The CY93422 disabled output in the "OFF" condition is represented by a single center line.

Switching Waveforms

Read Cycle[11]



Write Cycle (with $\overline{OE}$ = LOW)



Ordering Information

Speed (ns)	Ordering Code		Package Type	Operating Range
	Standard Power	Low Power		
35	CY93422APC		P7	Commercial
	CY93422ADC		D8	
45	CY93422PC	CY93L422APC	P7	Commercial
	CY93422DC	CY93L422ADC	D8	
	CY93422ADMB		D8	Military
55		CY93L422ADMB	D8	Military
60		CY93L422PC	P7	Commercial
		CY93L422DC	D8	
	CY93422DMB		D8	Military
75		CY93L422DMB	D8	Military

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IL}	1, 2, 3
I_{IH}	1, 2, 3
I_{CC}	1, 2, 3
I_{CEX}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
$t_{PLH(A)}$	7, 8, 9, 10, 11
$t_{PHL(A)}$	7, 8, 9, 10, 11
t_{PZH} ($\overline{CS_1}$, CS_2)	7, 8, 9, 10, 11
t_{PZL} ($\overline{CS_1}$, CS_2)	7, 8, 9, 10, 11
t_{PZH} ($\overline{WE}$)	7, 8, 9, 10, 11
t_{PZL} ($\overline{WE}$)	7, 8, 9, 10, 11
t_{PZH} ($\overline{OE}$)	7, 8, 9, 10, 11
t_{PZL} ($\overline{OE}$)	7, 8, 9, 10, 11
t_S (A)	7, 8, 9, 10, 11
t_h (A)	7, 8, 9, 10, 11
t_s (DI)	7, 8, 9, 10, 11
t_h (DI)	7, 8, 9, 10, 11
t_S ($\overline{CS_1}$, CS_2)	7, 8, 9, 10, 11
t_h ($\overline{CS_1}$, CS_2)	7, 8, 9, 10, 11
t_{pw} ($\overline{WE}$)	7, 8, 9, 10, 11

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