

**HYUNDAI**  
 SEMICONDUCTOR

**HYM591000**  
 1M×9-Bit CMOS DRAM MODULE

M441201C-JAN92

T46-23-18

## DESCRIPTION

The HYM591000M is a 1M words by 9 bits dynamic RAM module and consists of nine HY531000J Fast Page mode CMOS DRAM in 20/26 pin SOJ package mounted on a 30 pin glass-epoxy printed circuit board. 0.22μF decoupling capacitors are mounted under all the 1M DRAMs.

HYM591000M is suitable for easy interchange and addition of 1M bytes memory with parity RAM.

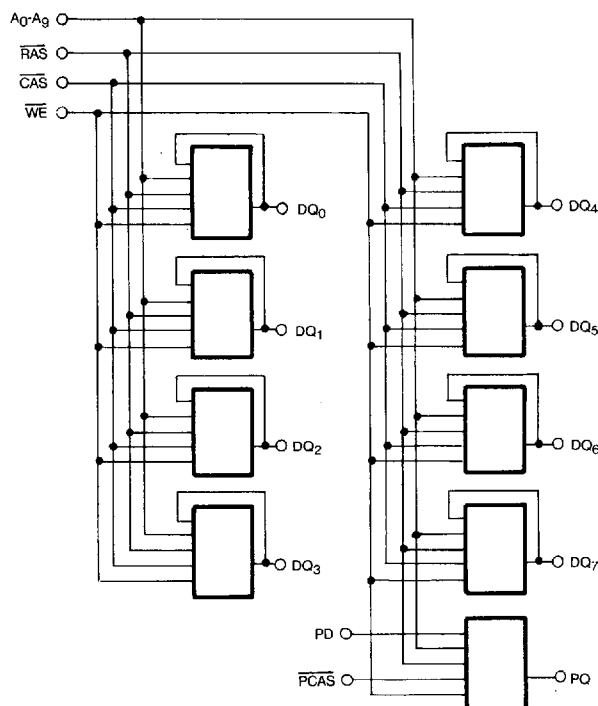
## FEATURES

- Fast Page Mode operation
- Fast access time

|               | t <sub>TRAC</sub> | t <sub>CAC</sub> | t <sub>PC</sub> |
|---------------|-------------------|------------------|-----------------|
| HYM591000M-60 | 60                | 20               | 40              |
| HYM591000M-70 | 70                | 20               | 40              |
| HYM591000M-80 | 80                | 20               | 45              |
| HYM591000M-10 | 100               | 25               | 55              |

- Single power supply of 5V±10%
- $\overline{\text{CAS}}$  Before  $\overline{\text{RAS}}$ ,  $\overline{\text{RAS}}$  only, Hidden Refresh
- Low power operating
  - 4.21W max (HYM591000M-60)
  - 3.71W max (HYM591000M-70)
  - 3.22W max (HYM591000M-80)
  - 2.72W max (HYM591000M-10)
- TTL compatible inputs and outputs
- 512 refresh cycles / 8ms

## BLOCK DIAGRAM



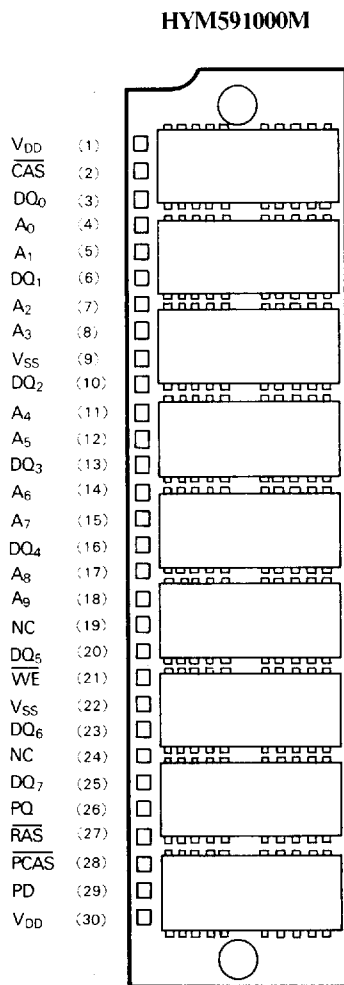
## PIN NAMES

|                                  |                                    |
|----------------------------------|------------------------------------|
| A <sub>0</sub> -A <sub>9</sub>   | ADDRESS INPUT                      |
| DQ <sub>0</sub> -DQ <sub>7</sub> | DATA INPUT/OUTPUT                  |
| PD                               | DATA IN FOR PARITY                 |
| PQ                               | DATA OUT FOR PARITY                |
| $\overline{\text{RAS}}$          | ROW ADDRESS STROBE                 |
| $\overline{\text{CAS}}$          | COLUMN ADDRESS STROBE              |
| $\overline{\text{PCAS}}$         | $\overline{\text{CAS}}$ FOR PARITY |
| $\overline{\text{WE}}$           | WRITE ENABLE                       |
| V <sub>DD</sub>                  | POWER( + 5V)                       |
| V <sub>SS</sub>                  | GROUND                             |

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## PIN CONNECTIONS



## NOTES :

1. Common  $\overline{\text{CAS}}$  control for eight data-in and data-out lines (DQ0-DQ7).
2. Separate  $\overline{\text{PCAS}}$  control for one separate pair of data-in (PD) and data-out (PQ) lines.
3. The common I/O feature dictates the use of only early write operations to prevent contention on data-in and data-out (DQ0-DQ7).

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## ABSOLUTE MAXIMUM RATINGS

| SYMBOL            | PARAMETER                                | RATING      | UNIT |
|-------------------|------------------------------------------|-------------|------|
| $T_A$             | Ambient Temperature                      | 0 to 70     | °C   |
| $T_{STG}$         | Storage Temperature(Plastic)             | -55 to 150  | °C   |
| $V_{IN}, V_{OUT}$ | Voltage on Any Pin Relative to $V_{SS}$  | -1.0 to 7.0 | V    |
| $V_{DD}$          | Voltage on $V_{DD}$ Relative to $V_{SS}$ | -1.0 to 7.0 | V    |
| $I_{OS}$          | Short Circuit Output Current             | 50          | mA   |
| $P_T$             | Power Dissipation                        | 5.4         | W    |

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

 $(T_A=0^{\circ}\text{C to }70^{\circ}\text{C})$ 

| SYMBOL   | PARAMETER          | MIN. | TYP. | MAX.       | UNIT |
|----------|--------------------|------|------|------------|------|
| $V_{DD}$ | Supply Voltage     | 4.5  | 5.0  | 5.5        | V    |
| $V_{IH}$ | Input High Voltage | 2.4  | -    | $V_{DD}+1$ | V    |
| $V_{IL}$ | Input Low Voltage  | -1.0 | -    | 0.8        | V    |

NOTE : All voltages are reference to  $V_{SS}$ .

## DC CHARACTERISTICS

 $(T_A=0^{\circ}\text{C to }70^{\circ}\text{C}, V_{DD}=5\text{V} \pm 10\%, V_{SS}=0\text{V}, \text{ unless otherwise noted})$ 

| SYMBOL     | PARAMETER                                                                                    | TEST CONDITIONS                                                                                            | SPEED | HYM591000M |      | UNIT          | NOTE |
|------------|----------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------|-------|------------|------|---------------|------|
|            |                                                                                              |                                                                                                            |       | MIN.       | MAX. |               |      |
| $ I_{LI} $ | Input Leakage Current(any input pin)                                                         | $V_{SS} \leq V_{IN} \leq V_{DD}$                                                                           |       |            | 90   | $\mu\text{A}$ |      |
| $ I_{LO} $ | Output Leakage Current for High Impedance State                                              | $V_{SS} \leq D_{OUT} \leq V_{DD}$<br>$\overline{\text{RAS}}, \overline{\text{CAS}}$ at $V_{IH}$            |       |            | 10   | $\mu\text{A}$ |      |
| $I_{DD1}$  | $V_{DD}$ Supply Current, Operating                                                           | $t_{RC}=t_{RC}(\text{min.})$                                                                               | -60   |            | 765  | mA            | 1, 2 |
|            |                                                                                              |                                                                                                            | -70   |            | 675  |               |      |
|            |                                                                                              |                                                                                                            | -80   |            | 585  |               |      |
|            |                                                                                              |                                                                                                            | -10   |            | 495  |               |      |
| $I_{DD2}$  | $V_{DD}$ Supply Current, TTL Standby                                                         | $\overline{\text{RAS}}, \overline{\text{CAS}}$ at $V_{IH}$<br>other inputs $\geq V_{SS}$                   |       |            | 18   | mA            |      |
| $I_{DD3}$  | $V_{DD}$ Supply Current,<br>$\overline{\text{RAS}}$ -only Refresh                            | $t_{RC}=t_{RC}(\text{min.})$                                                                               | -60   |            | 765  | mA            | 2    |
|            |                                                                                              |                                                                                                            | -70   |            | 675  |               |      |
|            |                                                                                              |                                                                                                            | -80   |            | 585  |               |      |
|            |                                                                                              |                                                                                                            | -10   |            | 495  |               |      |
| $I_{DD4}$  | $V_{DD}$ Supply Current,<br>Fast page mode                                                   | Minimum Cycle                                                                                              | -60   |            | 585  | mA            | 1, 2 |
|            |                                                                                              |                                                                                                            | -70   |            | 495  |               |      |
|            |                                                                                              |                                                                                                            | -80   |            | 405  |               |      |
|            |                                                                                              |                                                                                                            | -10   |            | 315  |               |      |
| $I_{DD5}$  | $V_{DD}$ Supply Current,<br>CMOS Standby                                                     | $\overline{\text{RAS}} \geq V_{DD}-0.2\text{V}, \overline{\text{CAS}}=V_{IH}$ , other inputs $\geq V_{SS}$ |       |            | 9    | mA            |      |
| $I_{DD6}$  | $V_{DD}$ Supply Current,<br>$\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$ Refresh | $t_{RC}=t_{RC}(\text{min.})$                                                                               | -60   |            | 765  | mA            | 2    |
|            |                                                                                              |                                                                                                            | -70   |            | 675  |               |      |
|            |                                                                                              |                                                                                                            | -80   |            | 585  |               |      |
|            |                                                                                              |                                                                                                            | -10   |            | 495  |               |      |
| $V_{OL}$   | Output Low Voltage                                                                           | $I_{OL}=4.2\text{mA}$                                                                                      |       |            | 0.4  | V             |      |
| $V_{OH}$   | Output High Voltage                                                                          | $I_{OH}=-5\text{mA}$                                                                                       |       | 2.4        |      | V             |      |

## NOTES :

- $I_{DD1}$  is dependent on output loading when the device output is selected, Specified  $I_{DD}(\text{max.})$  is measured with output open.
- $I_{DD}$  is dependent upon the number of address transitions, Specified  $I_{DD}(\text{max.})$  is measured with a maximum of two transitions per address cycle in fast page mode.

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## AC CHARACTERISTICS

(T<sub>A</sub>=0°C to 70°C, V<sub>DD</sub>=5V±10%, V<sub>SS</sub>=0V, unless otherwise noted.)

| #  | SYMBOL           | PARAMETER                                | HYM591000M |      |      |      |      |      |      |      | UNIT | NOTE  |
|----|------------------|------------------------------------------|------------|------|------|------|------|------|------|------|------|-------|
|    |                  |                                          | 60         |      | 70   |      | 80   |      | 10   |      |      |       |
|    |                  |                                          | MIN.       | MAX. | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. |      |       |
| 1  | t <sub>RAS</sub> | RAS Pulse Width                          | 60         | 10K  | 70   | 10K  | 80   | 10K  | 100  | 10K  | ns   |       |
| 2  | t <sub>RC</sub>  | Random Read or Write Cycle Time          | 120        |      | 130  |      | 150  |      | 180  |      | ns   |       |
| 3  | t <sub>RP</sub>  | RAS Precharge Time                       | 50         |      | 50   |      | 60   |      | 70   |      | ns   |       |
| 4  | t <sub>ASR</sub> | Row Address Set-up Time                  | 0          |      | 0    |      | 0    |      | 0    |      | ns   |       |
| 5  | t <sub>RAH</sub> | Row Address Hold Time                    | 10         |      | 10   |      | 10   |      | 15   |      | ns   |       |
| 6  | t <sub>RAI</sub> | Column Address to RAS Lead Time          | 30         |      | 35   |      | 40   |      | 50   |      | ns   |       |
| 7  | t <sub>RAD</sub> | RAS to Column Address Delay Time         | 15         | 30   | 15   | 35   | 15   | 40   | 20   | 50   | ns   | 1     |
| 8  | t <sub>ASC</sub> | Column Address Set-up Time               | 0          |      | 0    |      | 0    |      | 0    |      | ns   |       |
| 9  | t <sub>CAH</sub> | Column Address Hold Time                 | 15         |      | 15   |      | 15   |      | 20   |      | ns   |       |
| 10 | t <sub>RCD</sub> | RAS to CAS Delay                         | 20         | 40   | 20   | 50   | 20   | 60   | 25   | 75   | ns   | 2     |
| 11 | t <sub>RAC</sub> | Access Time From RAS                     |            | 60   |      | 70   |      | 80   |      | 100  | ns   | 3,4,5 |
| 12 | t <sub>AA</sub>  | Access Time From Column Address          |            | 30   |      | 35   |      | 40   |      | 50   | ns   | 5,7   |
| 13 | t <sub>CAC</sub> | Access Time From CAS                     |            | 20   |      | 20   |      | 20   |      | 25   | ns   | 5,6   |
| 14 | t <sub>CAS</sub> | CAS Pulse Width                          | 20         | 10K  | 20   | 10K  | 20   | 10K  | 25   | 10K  | ns   |       |
| 15 | t <sub>RSH</sub> | RAS Hold Time                            | 20         |      | 20   |      | 20   |      | 25   |      | ns   |       |
| 16 | t <sub>RCS</sub> | Read Command Set-up Time                 | 0          |      | 0    |      | 0    |      | 0    |      | ns   |       |
| 17 | t <sub>RCH</sub> | Read Command Hold Time Referenced to CAS | 0          |      | 0    |      | 0    |      | 0    |      | ns   | 8     |
| 18 | t <sub>RRH</sub> | Read Command Hold Time Referenced to RAS | 0          |      | 0    |      | 0    |      | 0    |      | ns   | 8     |
| 19 | t <sub>CRP</sub> | CAS to RAS Precharge Time                | 5          |      | 5    |      | 5    |      | 5    |      | ns   |       |
| 20 | t <sub>OFF</sub> | Output Buffer Turn Off Delay             | 0          | 20   | 0    | 20   | 0    | 20   | 0    | 20   | ns   | 9     |
| 21 | t <sub>WP</sub>  | Write Command Pulse Width                | 15         |      | 15   |      | 15   |      | 20   |      | ns   |       |
| 22 | t <sub>CP</sub>  | CAS Precharge Time                       | 10         |      | 10   |      | 10   |      | 10   |      | ns   |       |
| 23 | t <sub>AR</sub>  | Column Address Hold Time From RAS        | 50         |      | 55   |      | 60   |      | 75   |      | ns   |       |
| 24 | t <sub>WCR</sub> | Write Command Hold Time From RAS         | 50         |      | 55   |      | 60   |      | 75   |      | ns   |       |
| 25 | t <sub>WCS</sub> | Write Command Set-up Time                | 0          |      | 0    |      | 0    |      | 0    |      | ns   | 10    |
| 26 | t <sub>WCH</sub> | Write Command Hold Time                  | 15         |      | 15   |      | 15   |      | 20   |      | ns   |       |
| 27 | t <sub>DS</sub>  | Data-In Set-up Time                      | 0          |      | 0    |      | 0    |      | 0    |      | ns   | 11    |
| 28 | t <sub>DH</sub>  | Data-In Hold Time                        | 15         |      | 15   |      | 15   |      | 20   |      | ns   | 11    |
| 29 | t <sub>DHR</sub> | Data-In Hold Time Reference to RAS       | 50         |      | 55   |      | 60   |      | 75   |      | ns   |       |
| 30 | t <sub>CPA</sub> | Access Time From CAS Precharge           |            | 35   |      | 35   |      | 40   |      | 50   | ns   | 5,12  |
| 31 | t <sub>PC</sub>  | Fast page mode Cycle time                | 40         |      | 40   |      | 45   |      | 55   |      | ns   |       |
| 32 | t <sub>RWL</sub> | Write Command to RAS Lead Time           | 20         |      | 20   |      | 20   |      | 25   |      | ns   |       |
| 33 | t <sub>CWL</sub> | Write Command to CAS Lead Time           | 20         |      | 20   |      | 20   |      | 25   |      | ns   |       |
| 34 | t <sub>RPC</sub> | RAS to CAS Precharge Time                | 0          |      | 0    |      | 0    |      | 0    |      | ns   |       |
| 35 | t <sub>CSR</sub> | CAS Set-up Time(CAS Before RAS Cycle)    | 5          |      | 5    |      | 5    |      | 5    |      | ns   |       |

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| #  | SYMBOL            | PARAMETER                                  | HYM591000M |      |      |      |      |      |      |      | UNIT | NOTE  |
|----|-------------------|--------------------------------------------|------------|------|------|------|------|------|------|------|------|-------|
|    |                   |                                            | 60         |      | 70   |      | 80   |      | 10   |      |      |       |
|    |                   |                                            | MIN.       | MAX. | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. |      |       |
| 36 | t <sub>CHR</sub>  | CAS Hold Time(CAS Before RAS Cycle)        | 15         |      | 15   |      | 15   |      | 20   |      | ns   |       |
| 37 | t <sub>T</sub>    | Transition Time(Rise and Fall)             | 3          | 50   | 3    | 50   | 3    | 50   | 3    | 50   | ns   | 13,14 |
| 38 | t <sub>CLZ</sub>  | CAS to output in Low-z                     | 0          |      | 0    |      | 0    |      | 0    |      | ns   | 5     |
| 39 | t <sub>REF</sub>  | Refresh Interval(512 Cycle)                |            | 8    |      | 8    |      | 8    |      | 8    | ms   | 15    |
| 40 | t <sub>RASP</sub> | Fast page Mode RAS Pulse Width             | 60         |      | 70   |      | 80   |      | 100  |      | ns   |       |
| 41 | t <sub>CPT</sub>  | CAS Precharge Time(CBR Counter Test Cycle) | 40         |      | 40   |      | 40   |      | 50   |      | ns   |       |

## NOTES:

- Operation within the t<sub>RAD</sub>(max.) limit insures that t<sub>RAC</sub>(max.) can be met. t<sub>RAD</sub>(max.) is specified as a referenced point only. If t<sub>RAD</sub> is greater than the specified t<sub>RAD</sub>(max.) limit, then the access time is controlled by t<sub>AA</sub> and t<sub>CAC</sub>.
- Operation within the t<sub>RCD</sub>(max.) limit insures that t<sub>RAC</sub>(max.) can be met. t<sub>RCD</sub>(max.) is specified as a reference point only. If t<sub>RCD</sub> is greater than the specified t<sub>RCD</sub>(max.) limit, then the access time is controlled by t<sub>CAC</sub>.
- Assume t<sub>RAD</sub> ≤ t<sub>RAD</sub>(max.). If t<sub>RAD</sub> is greater than t<sub>RAD</sub>(max.) then t<sub>RAC</sub> will increase by the amount that t<sub>RAD</sub> exceeds t<sub>RAD</sub>(max.).
- Assume t<sub>RCD</sub> ≤ t<sub>RCD</sub>(max.). If t<sub>RCD</sub> is greater than t<sub>RCD</sub>(max.) then t<sub>RAC</sub> will increase by the amount that t<sub>RCD</sub> exceeds t<sub>RCD</sub>(max.).
- Measured with a load equivalent to two TTL loads and 100 pF.
- Assumes that t<sub>RCD</sub> ≥ t<sub>RCD</sub>(max.) and t<sub>RAD</sub> ≤ t<sub>RAD</sub>(max.).
- Assumes that t<sub>RCD</sub> ≤ t<sub>RCD</sub>(max.) and t<sub>RAD</sub> ≥ t<sub>RAD</sub>(max.).
- Either t<sub>RRH</sub> or t<sub>RCH</sub> must be satisfied for a read cycle.
- t<sub>OFF</sub> and t<sub>OH</sub> define the time at which the data output achieves the open circuit condition and is not referenced to the output voltage levels.
- t<sub>WCS</sub> is not a restrictive operating parameter. This is included in the data sheet as a electrical characteristic only. If t<sub>WCS</sub> ≥ t<sub>WCS</sub>(min.), the cycle is an early write cycle and the data out pin will remain open circuit(high impedance) throughout the entire cycle.
- t<sub>DS</sub> and t<sub>DH</sub> are referenced to the latter occurrence of CAS or WE.
- Access time is determined by the longer of t<sub>AA</sub>, t<sub>CAC</sub>, or t<sub>CPA</sub>.
- t<sub>T</sub> is measured between V<sub>IH</sub>(min.) and V<sub>IL</sub>(max.).
- AC measurements assume t<sub>T</sub>=5ns.
- An initial pause of 200μs is required after power-up and followed at least 8 initialization cycles(any combination of cycles containing a RAS clock such as RAS only refresh). 8 initialization cycles are required after extended period of bias without clocks.

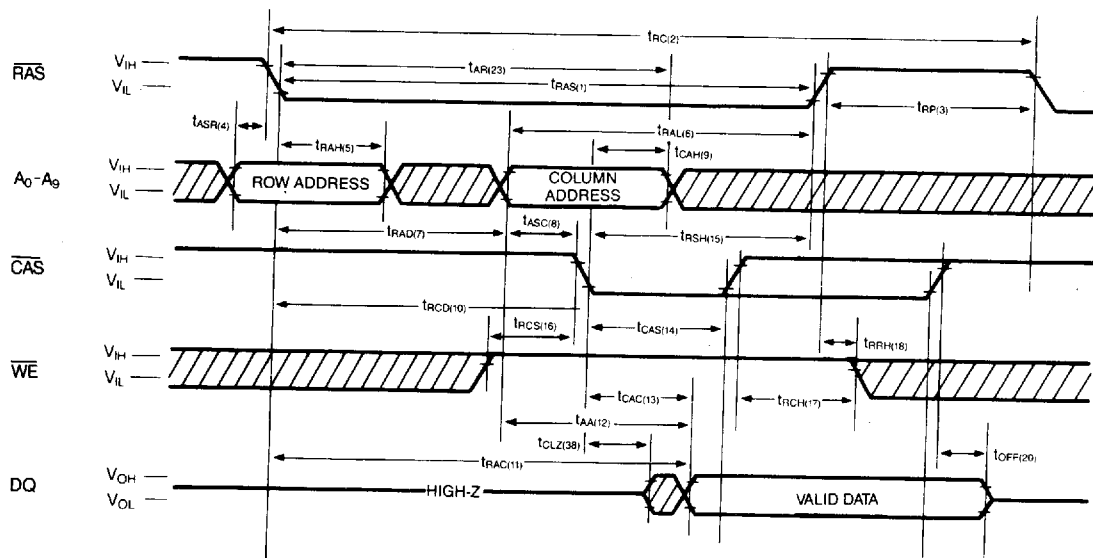
## CAPACITANCE

(T<sub>A</sub>=25°C, V<sub>DD</sub>=5V±10%, V<sub>SS</sub>=0V, unless otherwise noted)

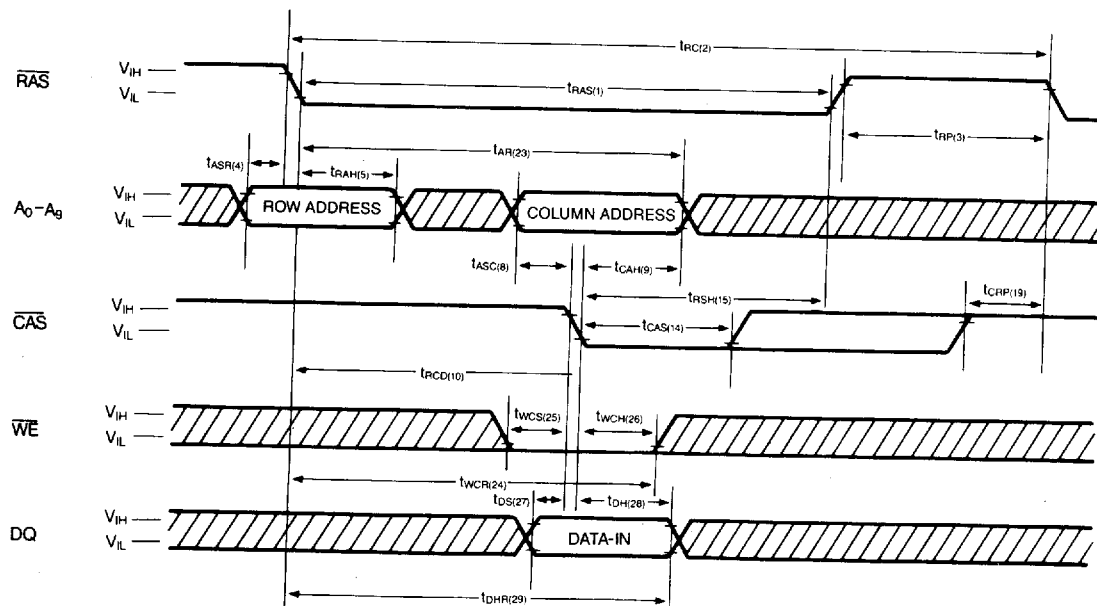
| SYMBOL           | PARAMETER                                                        | TYP. | MAX. | UNIT |
|------------------|------------------------------------------------------------------|------|------|------|
| C <sub>IN1</sub> | Input Capacitance(A <sub>0</sub> -A <sub>9</sub> , WE, CAS, RAS) | —    | 60   | pF   |
| C <sub>IN2</sub> | Input Capacitance(PD, PCAS)                                      | —    | 10   | pF   |
| C <sub>DQ</sub>  | I/O Capacitance(DQ <sub>0</sub> -DQ <sub>7</sub> )               | —    | 15   | pF   |
| C <sub>PQ</sub>  | Output Capacitance(PQ)                                           | —    | 10   | pF   |

## TIMING DIAGRAM

## READ CYCLE



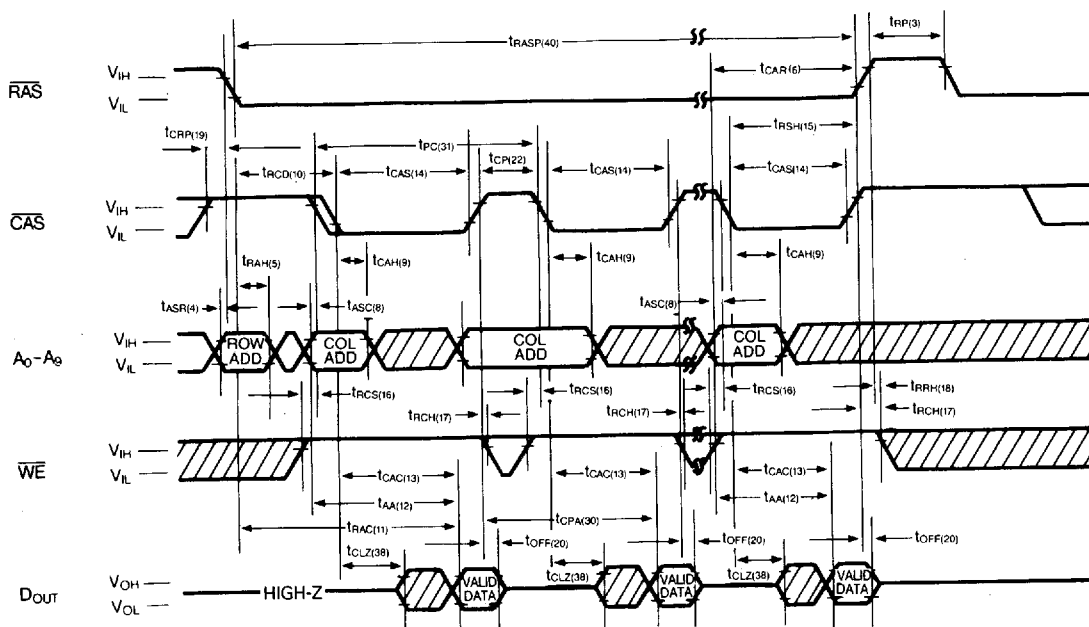
## EARLY WRITE CYCLE



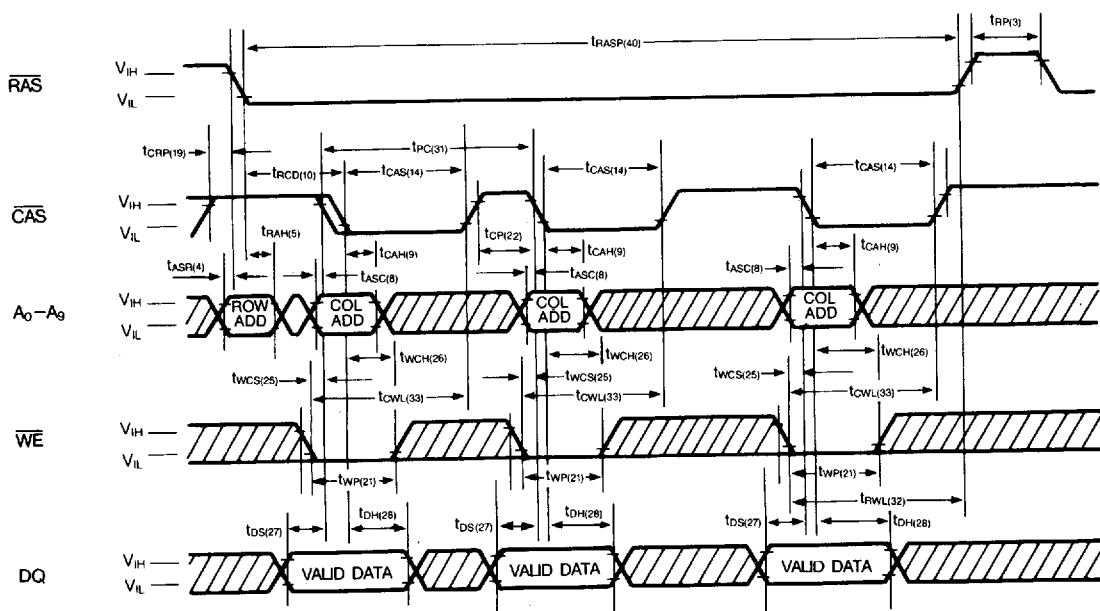
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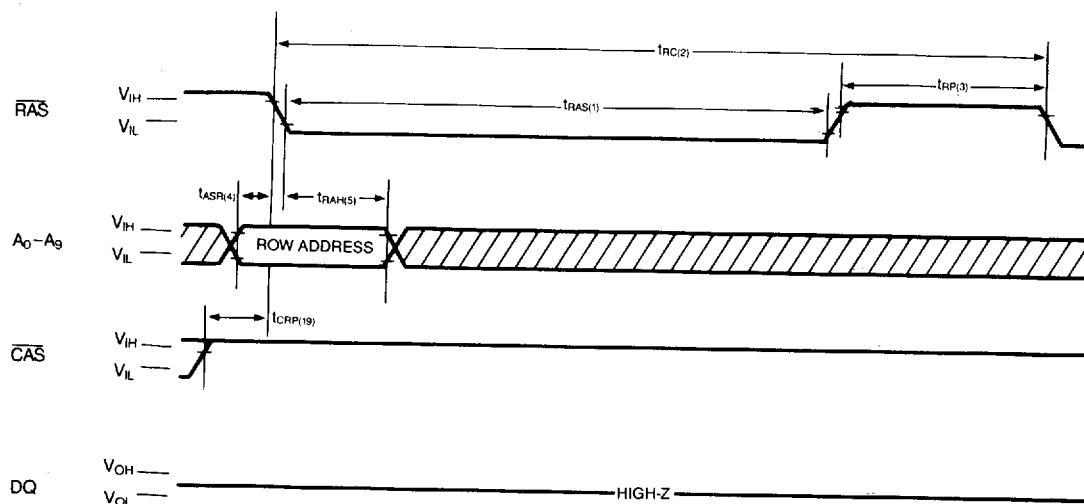
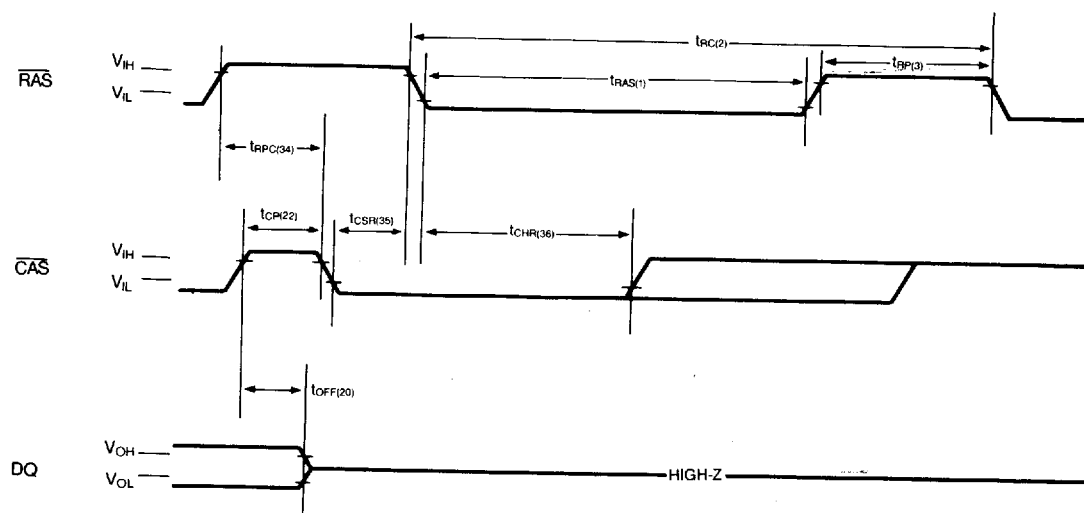
## FAST PAGE MODE READ CYCLE



## FAST PAGE MODE EARLY WRITE CYCLE



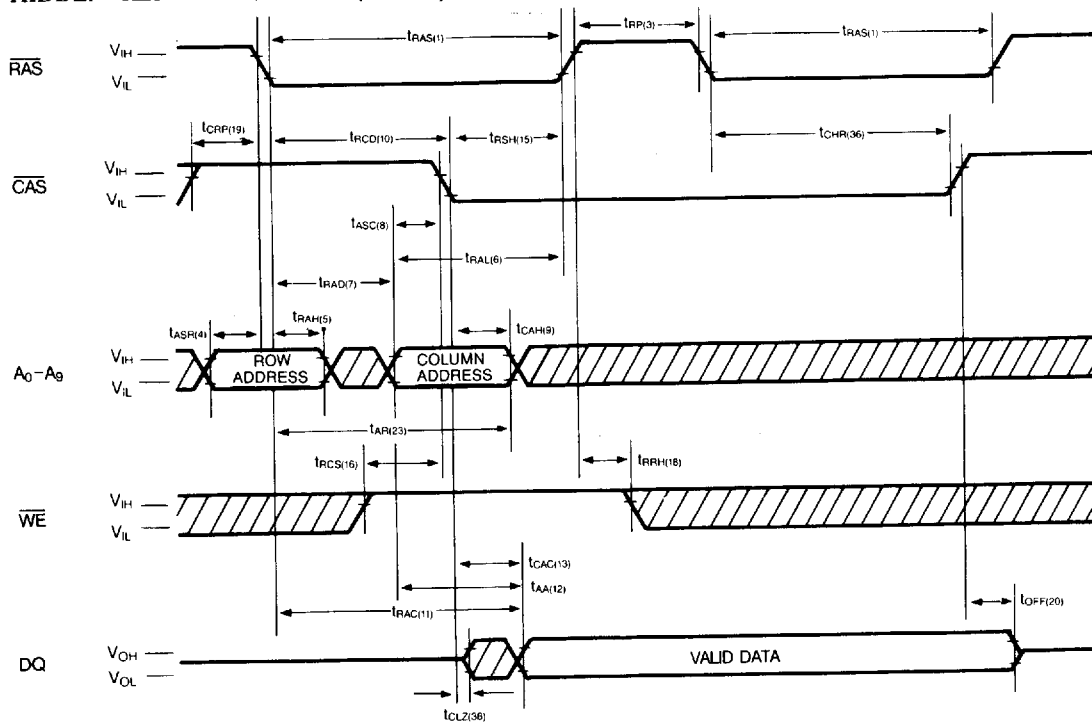
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**RAS-ONLY REFRESH CYCLE****CAS-BEFORE-RAS REFRESH CYCLE**

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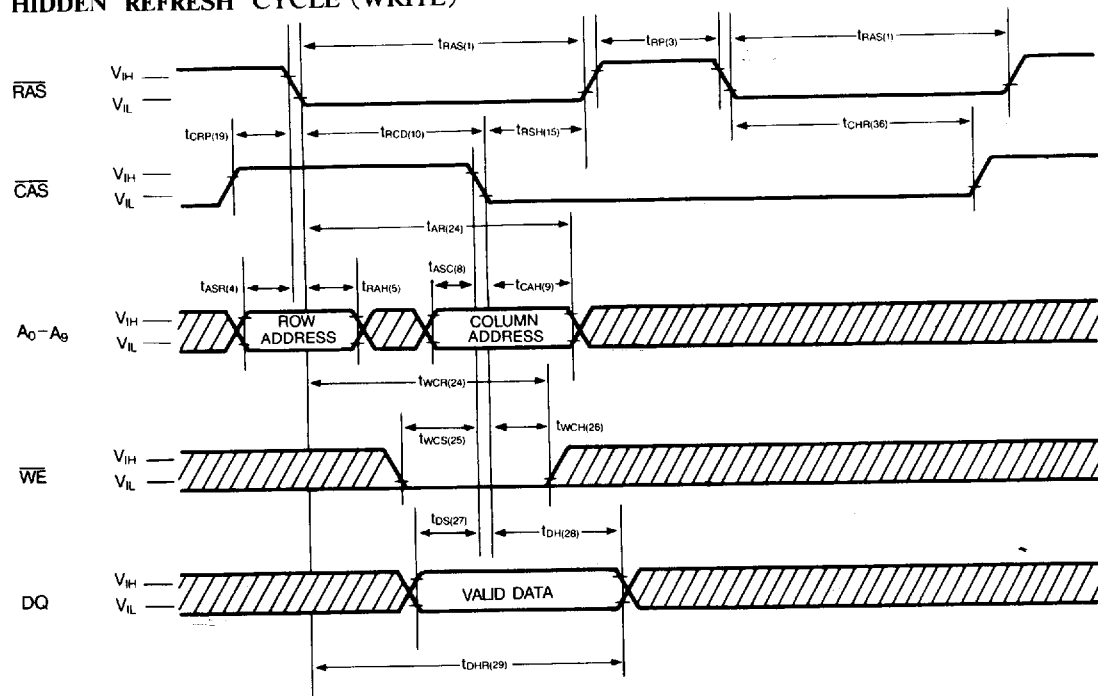
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## HIDDEN REFRESH CYCLE (READ)



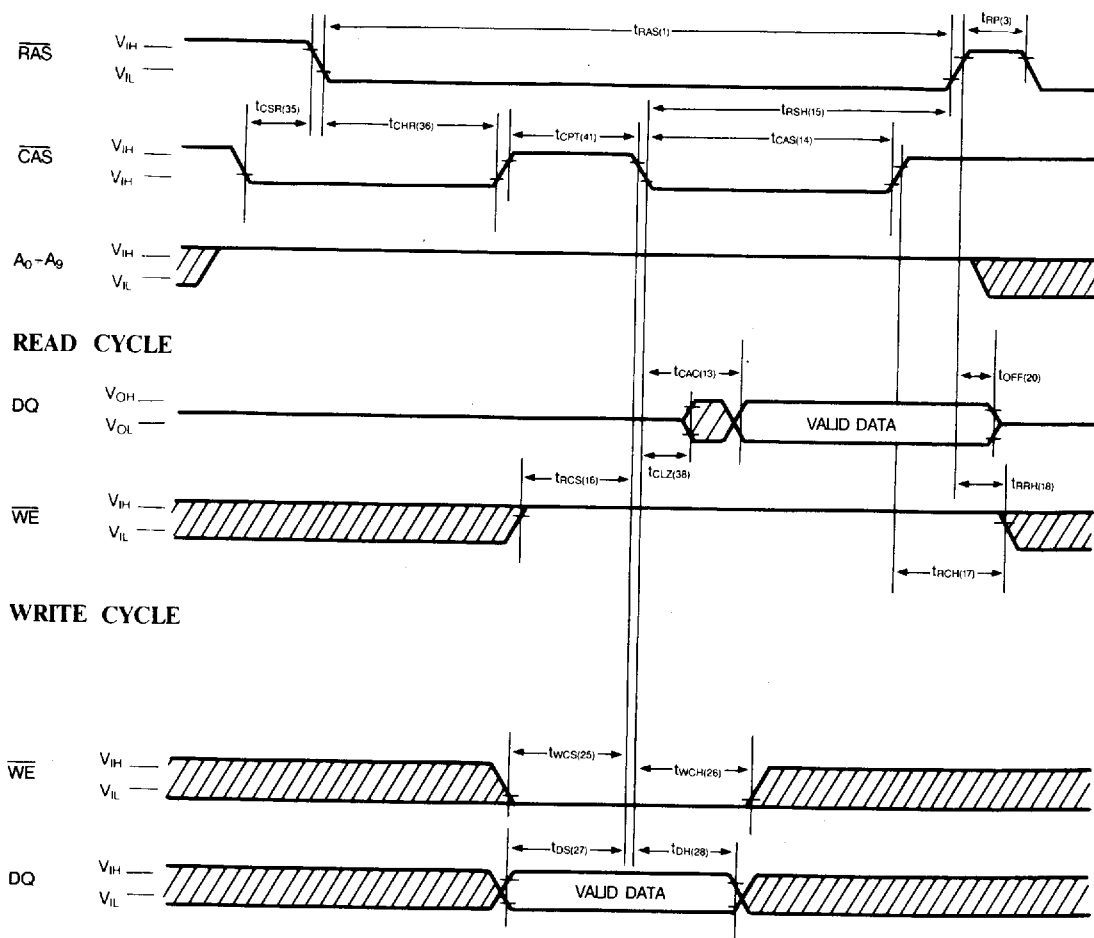
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## HIDDEN REFRESH CYCLE (WRITE)



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## CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



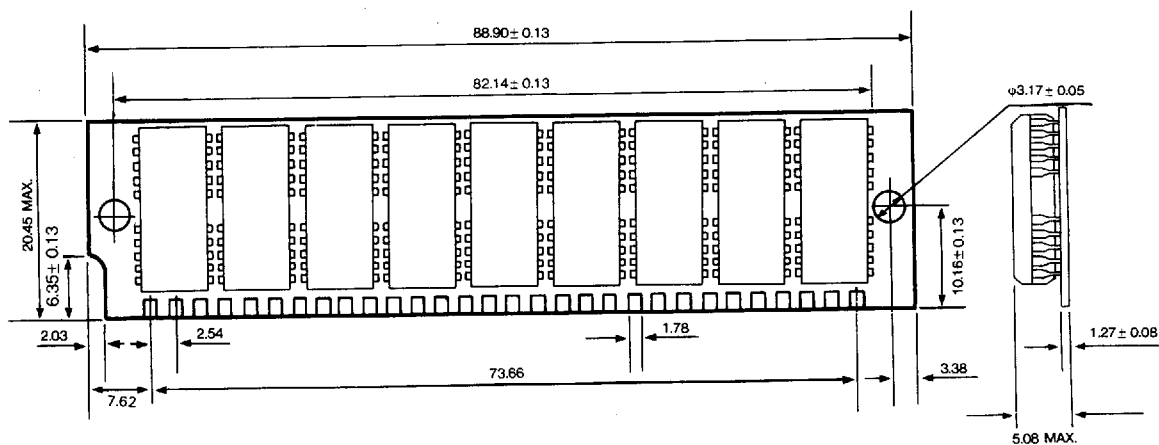
## HYM591000 1,048,576×9-Bit CMOS DRAM MODULE

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## PACKAGE INFORMATION

HYM591000M

UNIT : mm



## \* DETAIL OF CONTACTS

