GENERAL DESCRIPTION

The XRT94L33 is a highly integrated SONET/SDH terminator designed for E3/DS3/STS-1 mapping/de-mapping functions from either the STS-3 or STM-1 data stream. The XRT94L33 interfaces directly to the optical transceiver

The XRT94L33 processes the section, line and path overhead in the SONET/SDH data stream and also performs ATM and PPP PHY-layer processing. The processing of path overhead bytes within the STS-1s or TUG-3s includes 64 bytes for storing the J1 bytes. Path overhead bytes can be accessed through the microprocessor interface or via serial interface.

The XRT94L33 uses the internal E3/DS3 De-Synchronizer circuit with an internal pointer leak algorithm for clock smoothing as well as to remove the jitter due to mapping and pointer movements. These De-Synchronizer circuits do not need any external clock reference for its operation.

The SONET/SDH transmit blocks allow flexible insertion of TOH and POH bytes through both Hardware and Software. Individual POH bytes for the transmitted SONET/SDH signal are mapped either from the XRT94L33 memory map or from external interface. A1, A2 framing pattern, C1 byte and H1, H2 pointer byte are generated.

The SONET/SDH receive blocks receive SONET STS-3 signal or SDH STM-1 signal and perform the necessary transport and path overhead processing.

The XRT94L33 provides a line side APS (Automatic Protection Switching) interface by offering redundant receive serial interface to be switched at the frame boundary.

The XRT94L33 provides 3 mappers for performing STS-1/VC-3 to STS-1/DS3/E3 mapping function, one for each STS-1/DS3/E3 framers.

A PRBS test pattern generation and detection is implemented to measure the bit-error performance.

A general-purpose microprocessor interface is included for control, configuration and monitoring.

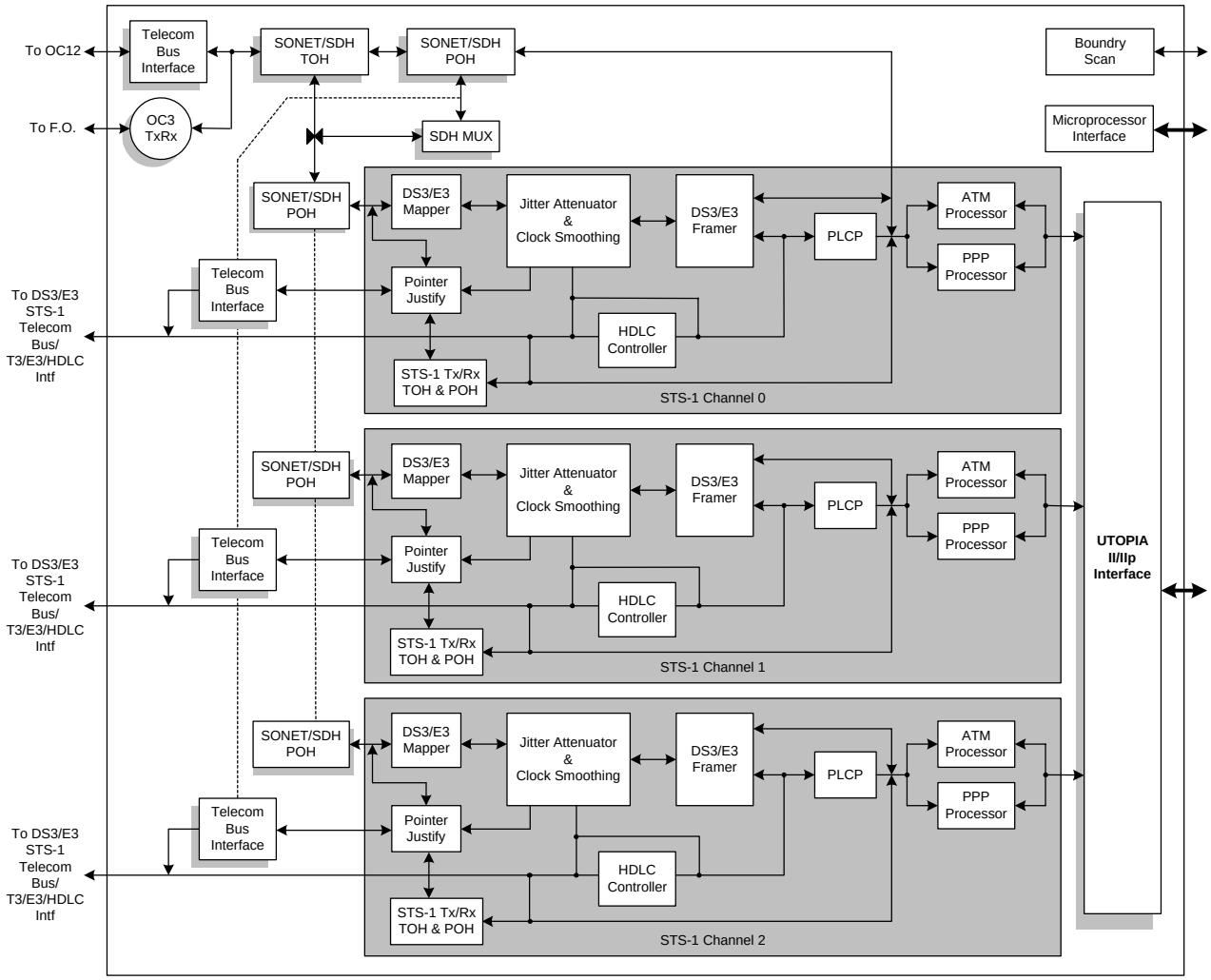
APPLICATIONS

- Network switches
- Add/Drop Multiplexer
- W-DCS Digital Cross Connect Systems

FEATURES

- Provides DS3/ E3 mapping/de-mapping for up to 3 tributaries through SONET STS-1 or SDH AU-3 and/or TUG-3/AU-4 containers
- Generates and terminates SONET/SDH section, line and path layers
- Integrated SERDES with Clock Recovery Circuit
- Provides SONET frame scrambling and descrambling
- Integrated Clock Synthesizer that generates 155 MHz and 77.76 MHz clock from an external 12.96/19.44/77.76 MHz reference clock
- Integrated 3 E3/DS3/STS-1 De-Synchronizer circuit that de-jitter gapped clock to meet 0.05UIpp jitter requirements
- Access to Line or Section DCC
- Level 2 Performance Monitoring for E3 and DS3
- Supports mixing of STS-1E and DS3 or E3 and DS3 tributaries
- UTOPIA Level 2 interface for ATM or level 2P for Packets
- E3 and DS3 framers for both Transmit and Receive directions
- Complete Transport/Section Overhead Processing and generation per Telcordia and ITU standards
- Single PHY and Multi-PHY operations supported
- Full line APS support for redundancy applications
- Loopback support for both SONET/SDH as well as E3/DS3/STS-1
- Boundary scan capability with JTAG IEEE 1149
- 8-bit microprocessor interface
- 3.3 V ± 5% Power Supply; 5 V input signal tolerance
- -40°C to +85°C Operating Temperature Range
- Available in a 504 Ball TBGA package

Block Diagram of the XRT94L33



ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE
XRT94L33IB	27 x 27 504 Lead TBGA	-40°C to +85°C

PIN DESCRIPTIONS of the XRT94L33

PIN #	SIGNAL NAME	I/O	SIGNAL TYPE	DESCRIPTION
				MICROPROCESSOR INTERFACE
Y22	PCLK	I	TTL	**Microprocessor Interface Clock Input:** This clock input signal is only used if the Microprocessor Interface has been configured to operate in one of the Synchronous Mode (e.g., Power PC 403 Mode). If the Microprocessor Interface is configured to operate in one of these modes, then it will use this clock signal to do the following. • To sample the CS*, WR*/R/W*, A[14:0], D[7:0], RD*/DS* and DBEN input pins, and • To update the state of D[7:0] and the RDY/DTACK output signals. ***NOTES:*** 1. The Microprocessor Interface can work with μPCLK frequencies ranging up to 33MHz. 2. This pin is inactive if the user has configured the Microprocessor Interface to operate in either the Intel-Asynchronous or the Motorola-Asynchronousl Modes. In this case, the user should tie this pin to GND.
AD25 AD23 AC21	PTYPE_0 PTYPE_1 PTYPE_2	I	TTL	**Microprocessor Type Select input:** These three input pins permit the user to configure the Microprocessor Interface block to readily support a wide variety of Microprocessor Interfaces. The relationship between the settings of these input pins and the corresponding Microprocessor Interface configuration is presented below. **PTYPE[2:0] Microprocessor Interface Mode** 000 Intel-Asynchronous Mode 001 Motorola – Asynchronous Mode 010 Intel X86 011 Intel I960 100 IDT3051/52 (MIPS) 101 Power PC 403 Mode 111 Motorola 860

PIN #	SIGNAL NAME	I/O	SIGNAL TYPE	DESCRIPTION
AD27 AB25 W23 Y24 AD26 AC25 AA24 Y23 AE24 AB20 AD22 AC20 AD21 AE23 AF24	PADDR_0 PADDR_1 PADDR_2 PADDR_3 PADDR_4 PADDR_5 PADDR_6 PADDR_7 PADDR_8 PADDR_9 PADDR_10 PADDR_11 PADDR_12 PADDR_13 PADDR_14	I	TTL	**Address Bus Input pins (Microprocessor Interface):** These pins permit the Microprocessor to identify on-chip registers and Buffer/Memory locations (within the XRT94L33) whenever it performs READ and WRITE operations with the XRT94L33.
AD20 AC19 AE22 AG24 AE21 AD19 AF23 AE20	PDATA_0 PDATA_1 PDATA_2 PDATA_3 PDATA_4 PDATA_5 PDATA_6 PDATA_7	I/O	TTL	**Bi-Directional Data Bus pins (Microprocessor Interface):** These pins are used to drive and receive data over the bi-directional data bus, whenever the Microprocessor performs READ and WRITE operations with the Microprocessor Interface of the XRT94L33.

PIN #	SIGNAL NAME	I/O	SIGNAL TYPE	DESCRIPTION
AF22	PWR_L/ R/W*	I	TTL	**Write Strobe/Read-Write Operation Identifier:** The exact function of this input pin depends upon which mode the Microprocessor Interface has been configured to operate in, as described below. **Intel-Asynchronous Mode – WR* - Write Strobe Input:** If the Microprocessor Interface is configured to operate in the Intel-Asynchronous Mode, then this input pin functions as the WR* (Active-Low WRITE Strobe) input signal from the Microprocessor. Once this active-low signal is asserted, then the input buffers (associated with the Bi-Directional Data Bus pins, D[7:0]) will be enabled. The Microprocessor Interface will latch the contents on the Bi-Directional Data Bus (into the "target" register or address location, within the XRT94L33) upon the rising of this input. **Motorola-Asynchronous Mode - R/W* - Read/Write Operation Identification Input Pin:** If the Microprocessor Interface is operating in the "Motorola-Asynchronous" Mode, then this pin is functionally equivalent to the "R/W*" input pin. In the Motorola Mode, a "READ" operation occurs if this pin is held at a logic "1", coincident to a falling edge of the RD/DS* (Data Strobe) input pin. **PowerPC 403 Mode – R/W* - Read/Write Operation Identification Input:** If the Microprocessor Interface is configured to operate in the PowerPC 403 Mode, then this input pin will function as the "Read/Write Operation Identification" input pin. Anytime the Microprocessor Interface samples this input signal at a logic "low" (while also sampling the CS* input pin "low") upon the rising edge of PCLK, then the Microprocessor Interface will (upon the very same rising edge of PCLK) latch the contents of the Address Bus (A]14:0]) into the Microprocessor Interface circuitry, in preparation for this forthcoming READ operation. At some point (later in this READ operation) the Microprocessor will also assert the DBEN*/OE* input pin, and the Microprocessor Interface will then place the contents of the "target" register (or address location within the XRT94L33) upon the Bi-Directional Dat Bus pins (D[7:0]), where it can be read by the Microprocessor. Anytime the Microprocessor Interface samples this input signal at a logic high (while also sampling the CS* input pin at a logic "low") upon the rising edge of PCLK, then the Microprocessor Interface will (upon the very same rising edge of PCLK) latch the contents of the Address Bus (A[14:0]) into the Microprocessor Interface circuitry, in preparation for the forthcoming WRITE operation. At some point (later in this WRITE operation) the Microprocessor will also assert the RD*/DS*/WE* input pin, and the Microprocessor Interface will then latch the contents of the Bi-Directional Data Bus (D[7:0]) into the contents of the "target" register or buffer location (within the XRT94L33).

PIN #	SIGNAL NAME	I/O	SIGNAL TYPE	DESCRIPTION
AC18	PRD_L/ DS*/ WE*	I	TTL	**READ Strobe /Data Strobe:** The exact function of this input pin depends upon which mode the Microprocessor Interface has been configured to operate in, as described below. **Intel-Asynchronous Mode – RD* - READ Strobe Input:** If the Microprocessor Interface is operating in the Intel-Asynchronous Mode, then this input pin will function as the RD* (Active Low READ Strobe) input signal from the Microprocessor. Once this active-low signal is asserted, then the XRT94L33 will place the contents of the addressed register (or buffer location) on the Microprocessor Bi-directional Data Bus (D[7:0]). When this signal is negated, the Data Bus will be tri-stated. **Motorola-Asynchronous (68K) Mode – DS* - Data Strobe Input:** If the Microprocessor Interface is operating in the Motorola Asynchronous Mode, then this input will function as the DS* (Data Strobe) input signal. **PowerPC 403 Mode – WE* - Write Enable Input:** If the Microprocessor Interface is operating in the PowerPC 403 Mode, then this input pin will function as the WE* (Write Enable) input pin. Anytime the Microprocessor Interface samples this active-low input signal (along with CS* and WR*/R/W*) also being asserted (at a logic level) upon the rising edge of PCLK, then the Microprocessor Interface will (upon the very same rising edge of PCLK) latch the contents on the Bi-Directional Data Bus (D[7:0]) into the “target” on-chip register or buffer location within the XRT94L33.

PIN #	SIGNAL NAME	I/O	SIGNAL TYPE	DESCRIPTION
AG23	ALE/ AS_L	I	TTL	**Address Latch Enable/Address Strobe:** The exact function of this input pin depends upon which mode the Microprocessor Interface has been configured to operate in, as described below. **Intel-Asynchronous Mode - ALE** If the Microprocessor Interface (of the XRT94L33) has been configured to operate in the Intel-Asynchronous Mode, then this active-high input pin is used to latch the address (present at the Microprocessor Interface Address Bus input pins (A[14:0]) into the XRT94L33 Microprocessor Interface block and to indicate the start of a READ or WRITE cycle. Pulling this input pin "high" enables the input bus drivers for the Address Bus input pins (A[14:0]). The contents of the Address Bus will be latched into the XRT94L33 Microprocessor Interface circuitry, upon the falling edge of this input signal. **Motorola-Asynchronous (68K) Mode – AS*** If the Microprocessor Interface has been configured to operate in the Motorola-Asynchronous Mode, then this active-low input pin is used to latch the data (residing on the Address Bus, A[14:0]) into the Microprocessor Interface circuitry of the XRT94L33. Pulling this input pin "low" enables the input bus drivers for the Address Bus input pins. The contents of the Address Bus will be latched into the Microprocessor Interface circuitry, upon the rising edge of this signal. **PowerPC 403 Mode – No Function – Tie to GND**: If the MIcroprocessor Interface has been configured to operate in the PowerPC 403 Mode, then this input pin has no role nor function and should be tied to GND.
AE19	PCS_L	I	TTL	**Chip Select Input:** The user must assert this active low signal in order to select the Microprocessor Interface for READ and WRITE operations between the Microprocessor and the XRT94L33 on-chip registers, LAPD and Trace Buffer locations.

PIN #	SIGNAL NAME	I/O	SIGNAL TYPE	DESCRIPTION

AD18	PRDY_L/
	DTACK*
	RDY
		O	CMOS	**READY or DTACK Output:**
				The exact function of this input pin depends upon wich mode the Microprocessor Interface has been configured to operate in, as described below.
				Intel Asynchronous Mode – RDY* - READY output:
				If the Microprocessor Interface has been configured to operate in the Intel-Asyncrhronous Mode, then this output pin will function as the “active-low” READY output.
				During a READ or WRITE cycle, the Microprocessor Interface block will toggle this output pin to the logic “low” level ONLY when it (the Microprocessor Interface) is ready to complete or terminate the current READ or WRITE cycle. Once the Microprocessor has determined that this input pin has toggled to the logic “low” level, then it is now safe for it to move on and execute the next READ or WRITE cycle.
				If (during a READ or WRITE cycle) the Microprocessor Interface block is holding this output pin at a logic “high” level, then the MIcroprocessor is expected to extend this READ or WRITE cycle, until it detect this output pin being toggled to the logic low level.
				Motorola Mode – DTACK* - Data Transfer Acknowledge Output:
				If the Microprocessor Interface has been configured to operate in the Motorola-Asynchronous Mode, then this output pin will function as the “active-low” DTACK* ouytput.
				During a READ or WRITE cycle, the Microprocessor Interface block will toggle this output pin to the logic low level, ONLY when it (the Microprocessor Interface) is ready to complete or terminate the current READ or WRITE cycle. Once the Microprocessor has determined that this input pin has toggled to the logic “low” leve, then it is now safe for it to move on and execute the next READ or WRITE cycle.
				If (during a READ or WRITE cycle) the Microprocessor Interface block is holding this output pin at a logic “high” level, then the MIcroprocessor is expected to extend this READ or WRITE cycle, until it detects this output pin being toggled to the logic low level.
				PowerPC 403 Mode – RDY – Ready Output:
				If the Microprocessor Interface has been configured to operate in the PowerPC 403 Mode, then this output pin will function as the “active-high” READY output.
				During a READ or WRITE cycle, the Microprocessor Interface block will toggle this output pin to the logic high level, ONLY when it (the Microprocessor Interface) is ready to complete or terminate the current READ or WRITE cycle. Once the Microprocessor has sampled this signal being at a logic “high” level (upon the rising edge of PCLK) then it is now safe for it to move on and execute the next READ or WRITE cycle.
				The Microprocessor Interface will update the state of this output pin upon the rising edge of PCLK.

PIN #	SIGNAL NAME	I/O	SIGNAL TYPE	DESCRIPTION
AF21	PDBEN_L	I	TTL	**Bi-directional Data Bus Enable Input pin:** This input pin permits the user to either enable or tri-state the Bi-Directional Data Bus pins (D[7:0]), as described below. Setting this input pin "low" enables the Bi-directional Data bus. Setting this input "high" tri-states the Bi-directional Data Bus.
AF20	PBLAST_L	I	TTL	**Last Burst Transfer Indicator input pin:** If the Microprocessor Interface is operating in the Intel-I960 Mode, then this input pin is used to indicate (to the Microprocessor Interface block) that the current data transfer is the last data transfer within the current burst operation. The Microprocessor should assert this input pin (by toggling it "Low") in order to denote that the current READ or WRITE operation (within a BURST operation) is the last operation of this BURST operation. ***Note:*** *The user should connect this input pin to GND whenever the Microprocessor Interface has been configured to operate in the Intel-Async, Motorola 68K and IBM PowerPC 403 modes.*
AG22	PINT_L	O	CMOS	**Interrupt Request Output:** This open-drain, active-low output signal will be asserted when the Mapper/Framer device is requesting interrupt service from the Microprocessor. This output pin should typically be connected to the "Interrupt Request" input of the Microprocessor.
AB24	RESET_L	I	TTL	**Reset Input:** When this "active-low" signal is asserted, the XRT94L33 will be asynchronously reset. When this occurs, all outputs will be "tri-stated" and all on-chip registers will be reset to their "default" values.
AE18	DIRECT_ADD_SEL	I	TTL	**Address Location Select input pin:** This input pin must be pulled "HIGH" in order to permit normal operation of the Microprocessor Interface.
SONET/SDH SERIAL LINE INTERFACE PINS				
T3	RXLDAT_P	I	LVPECL	**Receive STS-3/STM-1 Data – Positive Polarity PECL Input:** This input pin, along with RXLDAT_N functions as the Recovered Data Input, from the Optical Transceiver or as the Receive Data Input from the system back-plane ***Note:*** *For APS (Automatic Protection Switching) purposes, this input pin, along with "RXLDAT_N" functions as the "Primary" STS-3/STM-1 Receive Data Input Port.*
T2	RXLDAT_N	I	LVPECL	**Receive STS-3/STM-1 Data – Negative Polarity PECL Input:** This input pin, along with RXLDAT_P functions as the Recovered Data Input, from the Optical Transceiver or as the Receive Data Input from the system back-plane. ***Note:*** *For APS (Automatic Protection Switching) purposes, this input pin, along with "RXLDAT_P" functions as the "Primary Receive STS-3/STM-1 Data Input Port"*

PIN #	SIGNAL NAME	I/O	SIGNAL TYPE	DESCRIPTION
U2	RXLDAT_R_P	I	LVPECL	**Receive STS-3/STM-1 Data – Positive Polarity PECL Input – Redundant Port:** This input pin, along with "RXLDAT_R_N" functions as the Recovered Data Input, from the Optical Transceiver or as the Receive Data Input from the system back-plane. ***Note:*** *For APS (Automatic Protection Switching) purposes, this input pin, along with "RXLDAT_R_N" functions as the "Redundant Receive STS-3/STM-1 Data Input Port".*
U1	RXLDAT_R_N	I	LVPECL	**Receive STS-3/STM-1 Data – Negative Polarity PECL Input – Redundant Port:** This input pin, along with "RXLDAT_R_P" functions as the Recovered Data Input, from the Optical Transceiver or as the Receive Data Input from the system back-plane. ***Note:*** *For APS (Automatic Protection Switching) purposes, this input pin, along with "RXLDAT_R_N" functions as the "Redundant Receive STS-3/STM-1 Data Input Port".*
AE27	RXCLK_19MHZ	O	CMOS	**19.44MHz Recovered Output Clock:** This pin outputs a 19.44MHz clock signal that has been derived from the incoming STS-3/STM-1 line signal (via the Receive STS-3/STM-1 Clock and Data Recovery PLL). If the user wishes to operate the STS-3/STM-1 Interface in the "loop-timing" mode, then the user should route this particular signal through a "narrow-band" PLL (in order to attenuate any jitter within this signal) prior to routing it to the REFTTL input pin.
P3	REFCLK_P	I	LVPECL	**Transmit Reference Clock – Positive Polarity PECL Input:** This input pin, along with "REFCLK_N" and "REFTTL" can be configured to function as the timing source for the STS-3/STM-1 Transmit Interface Block. If the user configures these two input pins to function as the timing source, then the user must apply a 155.52MHz clock signal, in the form of a PECL signal to these input pins. The user can configure these two inputs to function as the timing source by writing the appropriate data into the "Transmit Line Interface Control Register " (Address Location = 0x0383) ***Note:*** *Users should set this pin to "1" if "REFTTL" clock input is used*
P2	REFCLK_N	I	LVPECL	**Transmit Reference Clock – Negative Polarity PECL Input:** This input pin, along with "REFCLK_P" and "REFTTL" can be configured to function as the timing source for the STS-3/STM-1 Transmit Interface Block. If the user configures these two input pins to function as the timing source, then the user must apply a 155.52MHz clock signal, in the form of a PECL signal to these input pins. The user can configure these two inputs to function as the timing source by writing the appropriate data into the "Transmit Line Interface Control Register " (Address Location = 0x0383) ***Note:*** *Users should set this pin to "0" if "REFTTL" clock input is used*

PIN #	SIGNAL NAME	I/O	SIGNAL TYPE	DESCRIPTION
P5	TXLDATO_P	O	LVPECL	**Transmit STS-3/STM-1 Data - Positive Polarity PECL Output:** This output pin, along with TXLDATO_N functions as the Transmit Data Output, to the Optical Transceiver or to the system back-plane. For "High-Speed" Back-Plane Applications, the user should note that data is output from these output pins upon the rising/falling edge of "TXLCLKO_P/TXLCLKO_N". ***Note:*** *For APS (Automatic Protection Switching) purposes, this output pin, along with "TXLDATO_N" functions as the "Primary" Transmit STS-3/STM-1 Data Output Port.*
P6	TXLDATO_N	O	LVPECL	**Transmit STS-3/STM-1 Data – Negative Polarity PECL Output:** This output pin, along with TXLDATO_P functions as the Transmit Data Output, to the Optical Transceiver or to the system back-plane. For "High-Speed" Back-Plane Applications, the user should note that data is output from these output pins upon the rising/falling edge of TXLCLKO_P/TXLCLKO_N. ***Note:*** *For APS (Automatic Protection Switching) purposes, this output pin, along with "TXLDATO_P" functions as the "Primary" Transmit STS-3/STM-1 Data Output Port.*
M4	TXLDATO_R_P	O	LVPECL	**Transmit STS-3/STM-1 Data - Positive Polarity PECL Output - Redundant Port:** This output pin, along with TXLDATO_R_N functions as the Transmit Data Output, to the Optical Transceiver or to the system back-plane. For "High-Speed" Back-Plane Applications, the user should note that data is output from these output pins upon the rising/falling edge of "TXLCLKO_R_P/TXLCLKO_R_N"). ***Note:*** *For APS (Automatic Protection Switching) purposes, this output pin, along with "TXLDATO_N" functions as the "Redundant" Transmit STS-3/STM-4 Data Output Port.*
M3	TXLDATO_R_N	O	LVPECL	**Transmit STS-3/STM-1 Data - Negative Polarity PECL Output - Redundant Port:** This output pin, along with TXLDATO_R_P functions as the Transmit Data Output, to the Optical Transceiver (for transmission to remote terminal equipment) or to the system back-plane (for transmission to some other System board) For "High-Speed" Back-Plane Applications, the user should note that data is output from these output pins upon the rising/falling edge of "TXLCLKO_R_P/TXLCLKO_R_N"). ***Note:*** *For APS (Automatic Protection Switching) purposes, this output pin, along with "TXLDATO_R_P" functions as the "Redundant" Transmit STS-3/STM-1 Data Output Port.*

PIN #	SIGNAL NAME	I/O	SIGNAL TYPE	DESCRIPTION
N6	TXLCLKO_P	O	LVPECL	**Transmit STS-3/STM-1 Clock – Positive Polarity PECL Output:** This output pin, along with TXLCLKO_N functions as the Transmit Clock Output signal. These output pins are typically used in "High-Speed" Back-Plane Applications. In this case, outbound STS-3/STM-1 data is output via the "TXLDATO_P/TXLDATO_N" output pins upon the rising edge of this clock signal. ***Note:*** *For APS (Automatic Protection Switching) purposes, this output pin, along with "TXLCLKO_N" functions as the "Primary Transmit Output Clock" signal.*
N5	TXLCLKO_N	O	LVPECL	**Transmit STS-3/STM-1 Clock – Negative Polarity PECL Output:** This output pin, along with TXLCLKO_P functions as the Transmit Clock Output signal. These output pins are typically used in "High-Speed" Back-Plane Applications. In this case, outbound STS-3/STM-1 data is output via the "TXLDATO_P/TXLDATO_N" output pins upon the falling edge of this clock signal. ***Note:*** *For APS (Automatic Protection Switching) purposes, this output pin, along with "TXLCLKO_N" functions as the "Primary Transmit Output Clock" signal.*
M1	TXLCLKO_R_P	O	LVPECL	**Transmit STS-3/STM-1 Clock – Positive Polarity PECL Output – Redundant Port:** This output pin, along with TXLCLKO_R_N functions as the Transmit Clock Output signal. These output pins are typically used in "High-Speed" Back-Plane Applications. In this case, outbound STS-3/STM-1 data is output via the "TXLDATO_R_P/TXLDATO_R_N" output pins upon the rising edge of this clock signal. ***Note:*** *For APS (Automatic Protection Switching) purposes, this output pin, along with "TXLCLKO_R_N" functions as the "Redundant Transmit Output Clock" signal.*
M2	TXLCLKO_R_N	O	LVPECL	**Transmit STS-3/STM-1 Clock – Negative Polarity PECL Output – Redundant Port:** This output pin, along with TXLCLKO_R_P functions as the Transmit Clock Output signal. These output pins are typically used in "High-Speed" Back-Plane Applications. In this case, outbound STS-3/STM-1 data is output via the "TXLDATO_R_P/TXLDATO_R_N" output pins upon the rising edge of this clock signal. ***Note:*** *For APS (Automatic Protection Switching) purposes, this output pin, along with "TXLCLKO_R_P" functions as the "Redundant Transmit Output Clock" signal.*

PIN #	SIGNAL NAME	I/O	SIGNAL TYPE	DESCRIPTION
P1	REFTTL	I	TTL	**19.44MHz or 77.76MHz Clock Synthesizer Reference Clock Input Pin:** The exact function of this input pin depends upon whether the user enables the "Clock Synthesizer" block or not. **If Clock Synthesizer is Enabled.** If the "Clock Synthesizer" block is enabled, then it will be used to generate the 155.52MHz, 19.44MHz and/or 77.76MHz clock signal for the STS-3/STM-1 block. In this mode, the user should apply a clock signal of either of the following frequencies to this input pin. • 19.44 MHz • 38.88 MHz • 51.84 MHz • 77.76 MHz Afterwards, the user needs to write the appropriate data into the "Transmit Line Interface Control Register" (Address Location = 0x0383) in order to (1) configure the Clock Synthesizer Block to accept any of the above-mentioned signals and generate a 155.52MHz, 19.44MHz or 77.76MHz clock signal, (2) to configure the Clock Synthesizer to function as the Clock Source for the STS-3/STM-1 block. **If Clock Synthesizer is NOT Enabled:** If the "Clock Synthesizer" block is NOT enabled, then it will NOT be used to generate the 19.44MHz and/or 77.76MHz clock signal, for the STS-3/STM-1 block. In this configuration seting, the user MUST apply a 19.44MHz clock signal to this input pin.
AG3	LOSTTL	I	TTL	**Loss of Optical Carrier Input – Primary:** The user is expected to connect the "Loss of Carrier" output (from the Optical Transceiver) to this input pin. If this input pin and the LOSPECL_P pin are pulled "high", or if both of these input pins are pulled "low", tthen the Receive STS-3 TOH Processor block will declare a "Loss of Optical Carrier" condition. ***Note:*** *This input pin is only active if the "Primary Port" is active. This input pin is inactive if the "Redundant Port" is active.*
AG25	LOSTTL_R	I	TTL	**Loss of Optical Carrier Input – Redundant:** The user is expected to connect the "Loss of Carrier" output (from the Optical Transceiver) to this input pin. If this input pin and the LOSPECL_R are pulled "high", or if both of these input pins are pulled "low", then the Receive STS-3 TOH Processor block will declare a "Loss of Optical Carrier" condition. ***Note:*** *This input pin is only active if the "Redundant Port" is active. This input pin is inactive if the "Primary Port" is active.*

PIN #	SIGNAL NAME	I/O	SIGNAL TYPE	DESCRIPTION
L4	LOSPECL_P	I	LVPECL	**Loss of PECL Interface Input – Primary:** If this input pin is pulled "high", then the Receive STS-3 TOH Processor block will declare a "Loss of PECL Interface" condition. ***Note:*** *This input pin is only active if the "Primary Port" is active. This input pin is inactive if the "Redundant Port" is active.*
L3	LOSPECL_R	I	LVPECL	**Loss of PECL Interface Input – Redundant:** If this input pin is pulled "high", then the Receive STS-3 TOH Processor block will declare a "Loss of PECL Interface" condition. ***Note:*** *This input pin is only active if the "Redundant Port" is active. This input pin is inactive if the "Primary Port" is active.*
V1	LOCKDET	O	CMOS	**Lock Detect Output Pin – Clock and Data Recovery PLL Block** This output pin indicates whether the Clock and data recovery PLL block has obtained lock to incoming STS-3/STM-1 signal or not. This pin pulses high if internal VCO frequency is within 0.05% of external reference clock This pin pulses low if internal VCO frequency is beyond 0.05% of external reference clock, and Loss of lock is declared.

STS-3/STM-1 TELECOM BUS INTERFACE – TRANSMIT DIRECTION				
E1	TXA_CLK/ TxAPSCLK	O I/O	CMOS	**Transmit STS-3/STM-1 Telecom Bus Interface - Clock Output Signal:** This output clock signal functions as the clock source for the Transmit STS-3/STM-1 Telecom Bus. All signals, that are output via the Transmit STS-3/STM-1 Telecom Bus Interface (e.g., TXA_C1J1, TXA_ALARM, TXA_DP, TXA_PL and TXA_D[7:0]) are updated upon the rising edge of this clock signal. This clock signal operates at 19.44MHz and is derived from the Clock Synthesizer block. **Transmit Payload APS Bus Interface Clock Input/Output signal – TxAPSCLK:** This pin can only be configured to operate in this mode if the XRT94L33 has been configured to operate in either the "ATM UNI" over "PPP over STS-3c" Mode.
F2	TXA_C1J1	O	CMOS	**Transmit STS-3/STM-1 Telecom Bus Interface - C1/J1 Byte Phase Indicator Output Signal:** This output pin pulses "high" under the following two conditions. • Whenever the C1 byte is being output via the "TxA_D[7:0]" output, and • Whenever the J1 byte is being output via the "TxA_D[7:0]" output. ***Notes:*** 1. The Transmit STS-3/STM-1 Telecom Bus Interface will indicate that it is currently transmitting the C1 byte (via the TXA_D[7:0] output pins), by pulsing this output pin "HIGH" (for one period of "TXA_CLKTXA_CK") and keeping the "TXA_PL" output pin pulled "LOW". 2. The Transmit STS-3/STM-1 Telecom Bus will indicate that it is currently transmitting the J1 byte (via the TXA_D[7:0] output pins), by pulsing this output pin "HIGH" (for one period of "TXA_CLKTXA_CK") while the "TXA_PL" output pin is pulled "HIGH". 3. This output pin is only active if the Transmit STS-3/STM-1 Telecom Bus Interface block is enabled and is configured to operate in the "Re-Phase OFF" Mode.

E2	TXA_ALARM/ TxAPSPAR	O I/O	CMOS TTL/ CMOS	**Transmit STS-3/STM-1 Telecom Bus Interface – Alarm Indicator Output signal:** This output pin pulses "high", coincident to the instant that the Transmit STS-3/STM-1 Telecom Bus Interface outputs an byte of any STS-1 or STS-3c signal (via the "TXD_D[7:0]" output pins) that is carrying an AIS-P indicator. This output pin is "low" for all other conditions. **NOTE:** This output pin is only active if the Transmit STS-3/STM-1 Telecom Bus Interface is enabled and has been configured to operate in the "Re-Phase OFF" Mode. **Transmit Payload APS Bus Interface – Parity Input/Output pin:** This pin can only be configured to operate in this role/function if the XRT94L33 has been configured to operate in the "ATM UNI" or the "PPP over STS-3c" Mode. Please see the "XRT94L33_Pin_Description_ATM_PPP.pdf" document for more information.
H3	TXA_DP	O	CMOS	**Transmit STS-3/STM-1 Telecom Bus Interface – Parity Output pin:** This output pin can be configured to function as either one of the following. The EVEN or ODD parity value of the bits which are output via the "TXA_D[7:0]" output pins. The EVEN or ODD parity value of the bits which are being output via the "TXA_D[7:0]" output pins and the states of the "TXA_PL" and "TXA_C1J1" output pins. *NOTES:* *a. The user can make any one of these configuration selections by writing the appropriate value into the "Telecom Bus Control" Register (Address Location = 0x0137).* b. *This output pin is only active if the XRT94L33 has been configured to output its STS-3/STM-1 or STS-3c data via the Transmit STS-3/STM-1 Telecom Bus Interface block.*

G4	TxSBFP	I	TTL	**Transmit STS-3/STM-1 Frame Alignment Sync Input:** The Transmit STS-3 TOH Processor Block can be configured to initiate its generation of a new "outbound" STS-3/STM-1 frame based upon an externally supplied 8kHz clock signal to this input pin. If the user opts to use this feature, then the Transmit STS-3/STM-1 Telecom Bus Interface will begin transmitting the very first byte of given STS-3 or STM-1 frame, upon sensing a rising edge (of the 8kHz signal) at this input pin. ***Notes:*** 1. If the user connects this input pin to GND, then the Transmit STS-3 TOH Processor block will generate its "outbound" STS-3/STM-1 frames asynchronously, with respect to any input signal. 2. This input signal must be synchronized with the signal that is supplied to the REFTTL input pin. Failure to insure this will result in bit errors being generated within the outbound STS-3/STM-1 signal. 3. The user must supply an 8kHz pulse (to this input pin) that has a width of approximately 51.4412.8ns (one 19.44MHz clock period). The user must not apply a 50% duty cycle 8kHz signal to this input pin. 4. Register "HRSYNC_DLY" (Address Location: 0x0135) defines the timing for TxSBFP input pin.
K5	TxA_PL/ TxAPSReq	O I/O	CMOS TTL/ CMOS	**Transmit STS-3/STM-1 Telecom Bus Interface – Payload Data Indicator Output Signal:** This output pin indicates whether the Transmit STS-3/STM-1 Telecom Bus Interface is currently placing a Transport Overhead byte or a "non-Transport Overhead Byte (e.g., STS-1 SPE, STS-3c SPE, VC-3 or VC-4 data) via the "TXA_D[7:0]" output pins. This output pin is pulled "low" for the duration that the Transmit STS-3/STM-1 Telecom Bus Interface is transmitting a Transport Overhead byte via the "TXA_D[7:0]" output pins. Conversely, this output pin is pulled "high" for the duration that the STS-3/STM-1 Transmit Telecom Bus is transmitting something other than a Transport Overhead byte via the "TXA_D[7:0]" output pins. **Transmit Payload APS Bus Interface – Request Input/Output pin:** This pin can only be configured to operate in this role if the XRT94L33 has been configured to operate in either the "ATM UNI" or "PPP over STS-3c" Mode.

J4 G3 D1 F3 J5 H4 D2 E3	TxA_D0/ TxAPSDat0 TxA_D1/ TxAPSDat1 TxA_D2/ TxAPSDat2 TxA_D3/ TxAPSDat3 TxA_D4/ TxAPSDat4 TxA_D5/ TxAPSDat5 TxA_D6/ TxAPSDat6 TxA_D7/ TxAPSDat7	O O I/O	CMOS CMOS CMOS/ TTL	**Transmit STS-3/STM-1 Telecom Bus Interface – Transmit Output Data Bus pins:** These 8 output pins function as the "Transmit STS-3/STM-1 Telecom Bus Interface" – Data bus output pins. If the STS-3/STM-1 Telecom Bus Interface is enabled, then all "outbound" STS-3/STM-1 data is output via these pins (in a byte-wide manner), upon the rising edge of the "TXA_CLK" output clock signal. **Transmit Payload APS Bus Interface – Data Input/Output pins:** These pins can only be configured to operate in this function/role if the XRT94L33 has been configured to operate in the "ATM UNI" or "PPP over STS-3c" Mode.

STS-3/STM-1 TELECOM BUS INTERFACE – RECEIVE DIRECTION				
W2	RxD_CLK/ RxAPSClk	I I I/O	TTL TTL TTL/ CMOS	**Receive STS-3/STM-1 Telecom Bus Interface - Clock Input Signal:** This input clock signal functions as the clock source for the Receive STS-3/STM-1 Telecom Bus Interface block. All input signals are sampled upon the falling edge of this input clock signal. This clock signal should operate at 19.44MHz. ***Note:*** *This input pin is only used if the "STS-3/STM-1 Telecom Bus" has been enabled. It should be connected to GND otherwise.* **Receive Payload APS Bus Interface - Clock input/output signal:** This input can only be configured to operate in this role/function if the XRT94L33 has been configured to operate in either the "ATM UNI" or "PPP over STS-3c" Mode.

AA3	RxD_PL	I	TTL	**Receive STS-3/STM-1 Telecom Bus Interface – Payload Data Indicator Output Signal:** This input pin indicates whether or not the Receive STS-3/STM-1 Telecom Bus Interface is currently receiving Transport Overhead bytes or "non-Transport Overhead bytes (e.g., STS-1 SPE, STS-3c SPE,VC-3 or VC-4 data) via the "RXD_D[7:0]" input pins. This input pin should be pulled "low" for the duration that "STS-3/STM-1 Receive STS-3/STM-1 Telecom Bus Interface is receiving a Transport Overhead byte via the "RXD_D[7:0]" input pins. Conversely, this input pin should be pulled "high" for the duration that the Receive STS-3/STM-1 Telecom Interface Bus is receiving something other than a Transport Overhead byte via the "RXD_D[7:0]" input pins. ***Note:*** *The user should connect this pin to GND if the STS-3/STM-1 Telecom Bus is NOT enabled.*
AD1	RxD_C1J1/ RxAPSVal	I I/O	TTL TTL/ CMOS	**Receive STS-3/STM-1 Telecom Bus Interface - C1/J1 Byte Phase Indicator Input Signal/Receive APS Valid Indicator Input/Output signal:** The exact function of this input pin depends upon (1) whether the STS-3/STM-1 Telecom Bus Interface has been enabled or not, and (2) whether the Payload APS Bus has been enabled or not. **If the STS-3/STM-1 Telecom Bus Interface has been enabled – RxD_C1J1:** This input pin should be pulsed "high" during both of the following conditions. a. Coincident to whenever the C1/J0 byte is being applied to the Receive STS-3/STM-1 Telecom Bus – Data Input pins (RXD_D[7:0]). b. b. Coincident to whenever the J1 byte is being applied to the Receive STS-3/STM-1 Telecom Bus – Data Input pins (RXD_D[7:0]) input. *NOTE: This input pin should be pulled "low" during all other times.* **Receive Payload APS Bus Interface – Data Valid Input/Output Signal:** This pin can only be configured to operate in this role if the XRT94L33 has been configured to operate in either the "ATM UNI" or "PPP over STS-3c" Mode.

AB3	RxD_DP	I	TTL	**Receive STS-3/STM-1 Telecom Bus Interface – Parity Input pin:** This input pin can be configured to function as one of the following. The EVEN or ODD parity value of the bits which are input via the "RXD_D[7:0]" input pins. The EVEN or ODD parity value of the bits which are being input via the "RXD_D[7:0]" input and the states of the "RXD_PL" and "RXD_C1J1" input pins. ***Notes:*** 1. The user can make any one of these configuration selections by writing the appropriate value into the "Telecom Bus Control" register (Address Location = 0x0137). 2. The user should connect this pin to GND if the STS-3/STM-1 Telecom Bus Interface is disabled.
W1	RxD_ALARM/ RxAPSPAR	I I/O	TTL TTL/ CMOS	**Receive STS-3/STM-1 Telecom Bus Interface – Alarm Indicator Input:** This input pin pulses "high" coincident to whether the Receive STS-3/STM-1 Telecom Bus Interface block is receiving a byte (via the "RxD_D[7:0] input pins) that is a part of any STS-1 or STS-3c signal that is carrying the AIS-P indicator. ***Note:*** *If the RxD_ALARM input signal pulses "HIGH" for any given STS-1 signal (within the "incoming" STS-3), then the corresponding Receive SONET POH Processor block will automatically declare the AIS-P defect condition.* **RxAPSParity – Receive Payload APS Bus Interface – Parity Input/Output Pin:** This pin can only be configured to operate in this role if the XRT94L33 has been configured to operate in either the "ATM UNI" or "PPP over STS-3c" Mode.

Y2	RxD_D0/ RxHRDat0/ RxAPSDat0	I I I/O	TTL TTL TTL/	**Receive STS-3/STM-1 Telecom Bus Interface – Receive Input Data Bus pins - RxD_D[7:0]:** These 8 input pins function as the Receive STS-3/STM-1 Telecom Bus Interface - Input data bus. All incoming STS-3/STM-1 data is sampled and latched (into the XRT94L33, via these input pins) upon the falling edge of the "RXD_CLK" input clock signal. **RxHRDat[7:0]: Receive data inputs for high-rate device** **Receive Payload APS Bus Interface – Data Bus Input/Output Pins:** These pins can only be configured to function in this role if the XRT94L33 has been configured to operate in the "ATM UNI" or "PPP over STS-3c" Mode. These pins cannot be configured to support "Payload APS" operation if the XRT94L33 has been configured to operate in an "Aggregation" role.
AD2	RxD_D1 RxHRDat1/ RxAPSDat1		CMOS	
AC3	RxD_D2 RxHRDat2/ RxAPSDat2			
AA4	RxD_D3 RxHRDat3/ RxAPSDat3			
AB4	RxD_D4 RxHRDat4/ RxAPSDat4			
Y1	RxD_D5 RxHRDat5/ RxAPSDat5			
AD3	RxD_D6 RxHRDat6/ RxAPSDat6			
AA5	RxD_D7 RxHRDat7/ RxAPSDat7			

SONET/SDH OVERHEAD INTERFACE – TRANSMIT DIRECTION				
H6	TxTOHClk	O	CMOS	**Transmit TOH Input Port – Clock Output:** This output pin, along with the "TxTOHEnable", "TxTOHFrame" output pins and the "TxTOH" and "TxTOHIns" input pins function as the "Transmit TOH Input Port". The Transmit TOH Input Port permits the user to externally insert his/her own value(s) for the TOH bytes (within the outbound STS-3/STM-1 signal). This output pin provides the user with a clock signal. If the "TxTOHEnable" output pin is "HIGH" and if the "TxTOHIns" input pin is pulled "HIGH", then the user is expected to provide a given bit (within the "TOH") to the "TxTOH" input pin, upon the falling edge of this clock signal. The data, residing on the "TxTOH" input pin will be latched into the XRT94L33 upon the rising edge of this clock signal. ***Note:*** *The Transmit TOH Input Port only supports the insertion of the TOH within the very first STS-1 of the outbound STS-3 signal.*
G5	TxTOHEnable	O	CMOS	**Transmit TOH Input Port – TOH Enable (or READY) indicator:** This output pin, along with the "TxTOHClk", "TxTOHFrame" output pins and the "TxTOH" and "TxTOHIns" input pins function as the "Transmit TOH Input Port". This output pin will toggle and remain "HIGH" anytime the "Transmit TOH Input Port" is ready to externally accept TOH data via the "TxOH" input pin. To externally insert user values of TOH into the "outbound" STS-3 data stream via the "Transmit TOH Input Port", do the following. • Continuously sample the state of "TxTOHFrame" and this output pin upon the rising edge of "TxTOHClk". • Whenever this output pin pulses "HIGH", then the user's external circuitry should drive the "TxTOHIns" input pin "HIGH". • Next, the user should output the next TOH bit, onto the "TxTOH" input pin, upon the rising edge of "TxTOHClk"

F8	TxTOH	I	TTL	**Transmit TOH Input Port – Input pin:** This input pin, along with the "TxTOHIns" input pin, the "TxTOHEnable" and "TxTOHFrame" and "TxTOHClk" output pins function as the "Transmit TOH Input Port". To externally insert user values of TOH into the outbound STS-3 data stream via the "Transmit TOH Input Port", do the following. • Continuously sample the state of "TxTOHFrame" and "TxTOHEnable" upon the rising edge of "TxTOHClk. • Whenever "TxTOHEnable" pulses "HIGH", then the user's external circuitry should drive the "TxTOHIns" input pin "HIGH". • Next, the user should output the next TOH bit, onto this input pin, upon the rising edge of "TxTOHClk". The "Transmit TOH Input Port" will sample the data (on this input pin) upon the falling edge of "TxTOHClk". ***Note:*** *Data at this input pin will be ignored (e.g., not sampled) unless the "TxTOHEnable" output pin is "HIGH" and the "TxTOHIns" input pin is pulled "HIGH".*
E8	TxTOHFrame	O	CMOS	**Transmit TOH Input Port – STS-3/STM-1 Frame Indicator:** This output pin, along with "TxTOHClk", "TxTOHEnable output pins, and the "TxTOH" and "TxTOHIns" input pins function as the "Transmit TOH Input Port". This output pin will pulse high (for one period of TxTOHClk), one "TxTOHClk" clock period prior to the first "TOH bit" of a given STS-3 frame, being expected via the "TxTOH" input pin. To externally insert user values of TOH into the "outbound" STS-3 data stream via the "Transmit TOH Input Port", do the following. • Continuously sample the state of "TxTOHEnable" and this output pin upon the rising edge of "TxTOHClk". • Whenever the "TxTOHEnable" output pin pulse "HIGH", then the user's external circuitry should drive the "TxTOHIns" input pin "HIGH". • Next, the user should output the next TOH bit, onto the "TxTOH" input pin, upon the rising edge of "TxTOHClk". ***Note:*** *The external circuitry (which is being interfaced to the "Transmit TOH Input Port" can use this particular output pin to denote the boundary of STS-3 frames.*

D6	TxTOHIns	I	TTL	**Transmit TOH Input Port – Insert Enable Input pin:** This input pin, along with the "TxTOH" input pin, and the "TxTOHEnable", "TxTOHFrame" and "TxTOHClk" output pins function as the "Transmit TOH Input Port". This input pin permits the user to either enable or disable the "Transmit TOH Input Port". If this input pin is "LOW", then the "Transmit TOH Input Port" will be disabled and will not sample and insert (into the "outbound" STS-3 data stream) any data residing on the "TxTOH" input, upon the rising edge of "TxTOHClk" If this input pin is "HIGH", then the "Transmit TOH Input Port" will be enabled. In this mode, whenever the "TxTOHEnable" output pin is also "HIGH", the "Transmit TOH Input Port" will sample and latch any data that is presented on the "TxTOH" input pin, upon the rising edge of "TxTOHClk". To externally insert user values of TOH into the "outbound" STS-3 data stream via the "Transmit TOH Input Port", do the following. • Continuously sample the state of "TxTOHFrame" and "TxTOHEnable" upon the rising edge of "TxTOHClk". • Whenever the "TxTOHEnable" output pin is sampled "high" then the user's external circuitry should drive this input pin "HIGH". • Next, the user should output the next TOH bit, onto the "TxTOH" input pin, upon the falling edge of "TxTOHClk". The "Transmit TOH Input Port" will sample the data (on this input pin) upon the falling edge of "TxTOHClk".] ***Notes:*** 1. Data applied to the "TxTOH" input pin will be sampled according to the following insertion priority scheme: 2. For DCC, E1, F1, E2 bytes, "TxTOH" input pin will be sampled if both "TxTOHEnable" and "TxTOHIns" are high. *1.* 3. For other TOH bytes, "TxTOH" input pin will be sampled if both "TxTOHEnable" and "TxTOHIns" are high or if both "TxTOHIns" and "Software Insertion Enabled" are "low".

B4	TxLDCCEnable	O	CMOS	**Transmit – Line DCC Input Port – Enable Output pin:** This output pin, along with the "TxTOHClk" output pin and the "TxLDCC" input pin permit the user to insert their value for the D4, D5, D6, D7, D8, D9, D10, D11 and D12 bytes into the Transmit STS-3 TOH Processor Block. The Transmit STS-3 TOH Processor block will accept this data and will insert into the D4, D5, D6, D7, D8, D9, D10, D11 and D12 byte-fields, within the "outbound" STS-3 data-stream. The Line DCC HDLC Controller circuitry (which is connected to the "TxTOHClk", the "TxSDCC" and this output pin, is suppose to do the following. It should continuously monitor the state of this output pin. Whenever this output pin pulses "HIGH", then the Line DCC HDLC Controller circuitry should place the next Line DCC bit (to be inserted into the "Transmit STS-3 TOH Processor" block) onto the "TxLDCC" input pin, upon the rising edge of "TxTOHClk". Any data that is placed on the "TxLDCC" input pin, will be sampled upon the falling edge of "TxOHClk".
D7	TxSDCCEnable	O	CMOS	**Transmit – Section DCC Input Port – Enable Output pin:** This output pin, along with the "TxTOHClk" output pin and the "TxSDCC" input pin permit the user to insert their value for the D1, D2 and D3 bytes, into the Transmit STS-3 TOH Processor Block. The Transmit STS-3 TOH Processor block will accept this data and will insert into the D1, D2 and D3 byte-fields, within the "outbound" STS-3 data-stream. The Section DCC HDLC Controller circuitry (which is connected to the "TxTOHClk", the "TxSDCC" and this output pin, is suppose to do the following. It should continuously monitor the state of this output pin. Whenever this output pin pulses "HIGH", then the Section DCC HDLC Controller circuitry should place the next Section DCC bit (to be inserted into the "Transmit STS-3 TOH Processor" block) onto the "TxSDCC" input pin, upon the rising edge of "TxTOHClk". Any data that is placed on the "TxSDCC" input pin, will be sampled upon the falling edge of "TxOHClk".

C5	TxSDCC	I	TTL	**Transmit - Section DCC Input Port – Input pin:** This input pin, along with the "TxSDCCEnable" and the "TxTOHClk" output pins permit the user to insert their value for the D1, D2 and D3 bytes, into the Transmit STS-3 TOH Processor Block. The Transmit STS-3 TOH Processor block will accept this data and insert it into the D1, D2 and D3 byte fields, within the "outbound" STS-3 data-stream. The Section DCC HDLC Circuitry that is interfaced to this input pin, the "TxSDCCEnable" and the "TxTOHClk" pins is suppose to do the following. It should continuously monitor the state of the "TxSDCCEnable" input pin. Whenever the "TxSDCCEnable" input pin pulses "HIGH", then the Section DCC HDLC Controller circuitry should place the next Section DCC bit (to be inserted into the "Transmit STS-3 TOH Processor" block) onto this input pin upon the rising edge of "TxTOHClk". Any data that is placed on the "TxSDCC" input pin, will be sampled upon the falling edge of "TxTOHClk". ***Note:*** *This pin should be connected to GND if it is not used.*
D8	TxLDCC	I	TTL	**Transmit - Line DCC Input Port:** This input pin, along with the "TxLDCCEnable" and the "TxTOHClk" pins permit the user to insert their value for the D4, D5, D6, D7, D8, D9, D10, D11 and D12 bytes, into the Transmit STS-3 TOH Processor Block. The Transmit STS-3 TOH Processor block will accept this data and insert it into the D4, D5, D6, D7, D8, D9, D10, D11 and D12 byte-fields, within the "outbound" STS-3 data-stream. Whatever Line DCC HDLC Controller Circuitry is interface to the this input pin, the "TxLDCCEnable" and the "TxTOHClk" is suppose to do the following. It should continuously monitor the state of the "TxLDCCEnable" input pin. Whenever the "TxLDCCEnable" input pin pulses "HIGH", then the Section DCC Interface circuitry should place the next Line DCC bit (to be inserted into the "Transmit STS-3 TOH Processor" block) onto the "TxLDCC" input pin, upon the rising edge of "TxTOHClk". Any data that is placed on the "TxLDCC" input pin, will be sampled upon the falling edge of "TxTOHClk". ***Note:*** *This pin should be connected to GND if it is not used.*

E9	TxE1F1E2Enable	O	CMOS	**Transmit E1-F1-E2 Byte Input Port – Enable (or Ready) Indicator Output pin:** This output pin, along with the "TxTOHClk" output pin and the "TxE1F1E2" input pin permit the user to insert their value for the E1, F1 and E2 bytes, into the Transmit STS-3 TOH Processor Block. The Transmit STS-3 TOH Processor block will accept this data and will insert into the E1, F1 and E2 byte-fields, within the "outbound" STS-3 data-stream. Whatever external circuitry (which is connected to the "TxTOHClk", the "TxE1F1E2" and this output pin), is suppose to do the following. It should continuously monitor the state of this output pin. Whenever this output pin pulses "HIGH", then the external circuitry should place the next "orderwire" bit (to be inserted into the "Transmit STS-3 TOH Processor" block) onto the "TxE1F1E2" input pin, upon the rising edge of "TxTOHClk". Any data that is placed on the "TxE1F1E2" input pin, will be sampled upon the falling edge of "TxOHClk".
C6	TxE1F1E2Frame	O	CMOS	**Transmit E1-F1-E2 Byte Input Port – Framing Output Pin.** This output pin pulses "HIGH" for one period of "TxTOHClk", one "TxTOHClk" bit-period prior to the "Transmit E1-F1-E2 Byte Input Port" expecting the very first byte of the E1 byte, within a given "outbound" STS-3 frame.
A4	TxE1F1E2	I	TTL	**Transmit E1-F1-E2 Byte Input Port – Input Pin:** This input pin, along with the "TxE1F1E2Enable" and the "TxTOHClk" output pins permit the user to insert their value for the E1, F1 and E2 bytes, into the Transmit STS-3 TOH Processor Block. The Transmit STS-3 TOH Processor block will accept this data and insert it into the E1, F1 and E2 byte fields, within the "outbound" STS-3 data-stream. Whatever external circuitry that is interfaced to this input pin, the "TxE1F1E2Enable" and the "TxTOHClk" pins is suppose to do the following. It should continuously monitor the state of the "TxE1F1E2Enable" input pin. Whenever the "TxE1F1E2Enable" input pin pulses "HIGH", then the external circuitry should place the next "orderwire" bit (to be inserted into the "Transmit STS-3 TOH Processor" block) onto this input pin upon the rising edge of "TxTOHClk". Any data that is placed on the "TxE1F1E2" input pin, will be sampled upon the falling edge of "TxTOHClk". ***Note:*** *This pin should be connected to GND if it is not used.*

C7	TXPOH	I	TTL	**Transmit Path Overhead Input Port – Input pin.** This pin is used for the Transmit AU-4/VC-4 Mapper POH Processor Block when TUG-3 mapping is used. This input pin permits the user to insert the POH data into the Transmit AU-4/VC-4 Mapper POH Processor blocks for insertion and transmission via the "outbound" STS-3 signal. In this mode, the external circuitry (which is being interfaced to the "Transmit Path Overhead Input Port" is suppose to monitor the following output pins; • TxPOHFrame_n • TxPOHEnable_n • TxPOHClk_n The "TxPOHFrame_n" output pin will toggle "high" upon the rising edge of "TxPOHClk_n" approximately one "TxPOHClk_n" period prior to the "TxPOH" port being ready to accept and process the first bit within J1 byte (e.g., the first POH byte). The "TxPOHFrame_n" output pin will remain "high" for eight consecutive "TxPOHClk_n" periods. The external circuitry should use this pin to note STS-1 SPE frame boundaries. The "TxPOHEnable_n" output pin will toggle "high" upon the rising edge of "TxPOHClk_n" approximately one "TxPOHClk_n" period prior to the "TxPOH" port being ready to accept and process the first bit within a given POH byte. To externally insert a given POH byte: (1) assert the "TxPOHIns_n" input pin by toggling it "high", and (2) place the value of the first bit (within this particular POH byte) on this input pin upon the very next rising edge of "TxPOHClk_n". This data bit will be sampled upon the very next falling edge of "TxPOHClk_n". The external circuitry should continue to keep the "TxPOHIns_n" input pin "high" and advancing the next bits (within the POH bytes) upon each rising edge of "TxPOHClk_n".
D9	TXPOHCLK	O	TTL	**Transmit Path Overhead Input Port – Clock Output pin:** This pin is used for the Transmit AU-4/VC-4 Mapper POH Processor Block when TUG-3 mapping is used. This output pin, along with "TxPOH", "TxPOHEnable", "TxPOHIns" and "TxPOHFrame" function as the "Transmit Path Overhead (TxPOH) Input Port". The "TxPOHFrame" and "TxPOHEnable" output pins are updated upon the falling edge this clock output signal. The "TxPOHIns" input pins and the data residing on the "TxPOH" input pins are sampled upon the next falling edge of this clock signal.

B5	TXPOHFRAME	O	TTL	**Transmit Path Overhead Input Port – Frame Output pin:** This pin is used for the Transmit AU-4/VC-4 Mapper POH Processor Block when TUG-3 mapping is used. This output pin, along with the "TxPOH", "TxPOHEnable", "TxPOHIns" and "TxPOHClk" function as the "Transmit Path Overhead Input Port". If the user is only inserting POH data via these input pins: ***Note:*** *In this mode, the "TxPOH" port will pulse these output pins "high" whenever it is ready to accept and process the J1 byte (e.g., the very first POH byte) via this port.*
C8	TXPOHINS	I	TTL	**Transmit Path Overhead Input Port – Insert Enable Input pin:** This pin is used for the Transmit AU-4/VC-4 Mapper POH Processor Block when TUG-3 mapping is used. These input pins, along with "TxPOH", "TxPOHEnable", "TxPOHFrame" and "TxPOHClk" function as the "Transmit Path Overhead (TxPOH) Input Port. These input pins permit the user to enable or disable the "TxPOH" input port. If these input pins are pulled "high", then the "TxPOH" port will sample and latch data via the corresponding "TxPOH" input pins, upon the falling edge of "TxPOHClk". ***Note:*** *Conversely, if these input pins are pulled "low", then the "TxPOH" port will NOT sample and latch data via the corresponding "TxPOH" input pins.*
B6	TXPOHENABLE	O	TTL	**Transmit Path Overhead Input Port – POH Indicator Output pin:** This pin is used for the Transmit AU-4/VC-4 Mapper POH Processor Block when TUG-3 mapping is used. These output pins, along with "TxPOH", "TxPOHIns", "TxPOHFrame" and "TxPOHClk" function as the "Transmit Path Overhead (TxPOH) Input Port". These output pins will pulse "high" anytime the "TxPOH" port is ready to accept and process POH bytes. These output pins will be "low" at all other times.

E10 B8 D11	TxPOH_0 TxPOH_1 TxPOH_2	I	TTL	**Transmit Path Overhead Input Port – Input pin.** These input pins permit the user to insert the POH data into each of the 3 Transmit SONET POH Processor blocks (for insertion and transmission via the "outbound" STS-3 signal. If the user is only inserting POH data via these input pins: In this mode, the external circuitry (which is being interfaced to the "Transmit Path Overhead Input Port" is suppose to monitor the following output pins; • TxPOHFrame_n • TxPOHEnable_n • TxPOHClk_n The "TxPOHFrame_n" output pin will toggle "high" upon the rising edge of "TxPOHClk_n" approximately one "TxPOHClk_n" period prior to the "TxPOH" port being ready to accept and process the first bit within J1 byte (e.g., the first POH byte). The "TxPOHFrame_n" output pin will remain "high" for eight consecutive "TxPOHClk_n" periods. The external circuitry should use this pin to note STS-1 SPE frame boundaries. The "TxPOHEnable_n" output pin will toggle "high" upon the rising edge of "TxPOHClk_n" approximately one "TxPOHClk_n" period prior to the "TxPOH" port being ready to accept and process the first bit within a given POH byte. To externally insert a given POH byte: (1) assert the "TxPOHIns_n" input pin by toggling it "high", and (2) place the value of the first bit (within this particular POH byte) on this input pin upon the very next rising edge of "TxPOHClk_n". This data bit will be sampled upon the very next falling edge of "TxPOHClk_n". The external circuitry should continue to keep the "TxPOHIns_n" input pin "high" and advancing the next bits (within the POH bytes) upon each rising edge of "TxPOHClk_n".
A5 A6 A7	TxPOHClk_0 TxPOHClk_1 TxPOHClk_2	O	CMOS	**Transmit Path Overhead Input Port – Clock Output pin:** These output pins, along with "TxPOH_n", "TxPOHEnable_n", "TxPOHIns_n" and "TxPOHFrame" function as the "Transmit Path Overhead (TxPOH) Input Port". The "TxPOHFrame" and "TxPOHEnable" output pins are updated upon the falling edge this clock output signal. The "TxPOHIns_n" input pins and the data residing on the "TxPOH_n" input pins are sampled upon the next falling edge of this clock signal.

C9 C10 A8	TxPOHFrame_0 TxPOHFrame_1 TxPOHFrame_2	O	CMOS	**Transmit Path Overhead Input Port – Frame Output pin:** These output pins, along with the "TxPOH_n", "TxPOHEnable_n", "TxPOHIns_n" and "TxPOHClk_n" function as the "Transmit Path Overhead Input Port". The exact function of these output pins depends upon whether the user inserting POH or TOH data via the "TxPOH_n" input pins. If the user is only inserting POH data via these input pins: The "TxPOH" port will pulse these output pins "high" whenever it is ready to accept and process the J1 byte (e.g., the very first POH byte) via this port. ***Notes:*** 1. The externally circuitry can determine whether the "TxPOH" port is expecting the A1 byte or the J1 byte, by checking the state of the corresponding "TxPOHEnable" output pin. If the "TxPOHEnable_n" output pin is "LOW" while the "TxPOHFrame_n" output pin is "HIGH", then the "TxPOH" port is ready to process the A1 (TOH) bytes. 2. If the "TxPOHEnable_n" output pin is "HIGH" while the "TxPOHFrame_n" output pin is "HIGH", then the "TxPOH" port is ready to process the J1 (POH) bytes.
D10 E11 C11	TxPOHIns_0 TxPOHIns_1 TxPOHIns_2	I	TTL	**Transmit Path Overhead Input Port – Insert Enable Input pin:** These input pins, along with "TxPOH_n", "TxPOHEnable_n", "TxPOHFrame_n" and "TxPOHClk_n" function as the Transmit Path Overhead (TxPOH) Input Port. These input pins permit the user to enable or disable the "TxPOH" input port. If these input pins are pulled "high", then the "TxPOH" port will sample and latch data via the corresponding "TxPOH" input pins, upon the falling edge of "TxPOHClk_n". Conversely, if these input pins are pulled "low", then the "TxPOH" port will NOT sample and latch data via the corresponding "TxPOH" input pins. ***Note:*** *If the "TxPOHIns_n" input pin is pulled "LOW", this setting will be overridden if the user has configured the "Transmit SONET/STS-1 POH Processor" or "Transmit STS-1 TOH Processor" blocks to accept certain POH or TOH overhead bytes via the external port.*
B7 B9 B10	TxPOHEnable_0 TxPOHEnable_1 TxPOHEnable_2	O	CMOS	**Transmit Path Overhead Input Port – POH Indicator Output pin:** These output pins, along with "TxPOH_n", "TxPOHIns_n", "TxPOHFrame_n" and "TxPOHClk_n" function as the "Transmit Path Overhead (TxPOH) Input Port". These output pins will pulse "high" anytime the "TxPOH" port is ready to accept and process POH bytes. These output pins will be "low" at all other times.

TRANSMIT LINE/ SYSTEM SIDE INTERFACE PINS				
C12	TXDS3CLK_0 TXE3CLK_0	I	TTL	**Transmit DS3/E3 Reference Clock Input – Channel 0 (Not used for Mapper Applications):** The exact manner in which the user should handle this input pin depends upon whether Channel 0 has been configured to operate in the Mapper Mode or in the ATM UNI/PPP Mode. **If Channel 0 is configured to operate in the Mapper Mode**: If Channel 0 has been configured to operate in the Mapper Mode, then this input pin supports no function, and should, therefore, be connected to GND. **If Channel 0 is configured to operate in the ATM UNI/PPP/Clear Channel Mode:** If Channel 0 (within the XRT94L33) has been configured to operate in the ATM UNI/PPP Mode, then this input pin will function as the timing reference clock signal for the Transmit STS-1/DS3/E3 Framer block circuitry, provided that Channel 0 has been configured to operate in the Local Timing Mode. If Channel 0 has been configured to operate in the DS3 Mode, then the user is expected to apply a 44.736MHz clock signal to this input pin. Likewise, if Channel 0 has been configured to operate in the E3 Mode, then the user is expected to apply a 34.368MHz clock signal to this input pin. ***Note:*** *For more information on using the XRT94L33 for ATM UNI/PPP applications, the user should consult the XRT94L33 1-Channel STS-3c/3-Channel DS3/E3/STS-1 ATM UNI/PPP Data Sheet.*
B20	TXDS3CLK_1 TXE3CLK_1	I	TTL	**Transmit DS3/E3 Reference Clock Input – Channel 1 (Not used for Mapper Applications):** The exact manner in which the user should handle this input pin depends upon whether Channel 1 has been configured to operate in the Mapper Mode or in the ATM UNI/PPP Mode. **If Channel 1 is configured to operate in the Mapper Mode**: If Channel 1 has been configured to operate in the Mapper Mode, then this input pin supports no function, and should, therefore, be connected to GND. **If Channel 1 is configured to operate in the ATM UNI/PPP Mode:** If Channel 1 (within the XRT94L33) has been configured to operate in the ATM UNI/PPP Mode, then this input pin will function as the timing reference clock signal for the Transmit STS-1/DS3/E3 Framer block circuitry, provided that Channel 1 has been configured to operate in the Local Timing Mode. If Channel 1 has been configured to operate in the DS3 Mode, then the user is expected to apply a 44.736MHz clock signal to this input pin. Likewise, if Channel 1 has been configured to operate in the E3 Mode, then the user is expected to apply a 34.368MHz clock signal to this input pin. ***Note:*** *For more information on using the XRT94L33 for ATM UNI/PPP applications, the user should consult the XRT94L33 1-Channel STS-3c/3-Channel DS3/E3/STS-1 ATM UNI/PPP Data Sheet.*

AF17	TXDS3CLK_2 TXE3CLK_2	I	TTL	**Transmit DS3/E3 Reference Clock Input – Channel 2 (Not used for Mapper Applications):** The exact manner in which the user should handle this input pin depends upon whether Channel 2 has been configured to operate in the Mapper Mode or in the ATM UNI/PPP Mode. **If Channel 2 is configured to operate in the Mapper Mode**: If Channel 2 has been configured to operate in the Mapper Mode, then this input pin supports no function, and should, therefore, be connected to GND. **If Channel 2 is configured to operate in the ATM UNI/PPP Mode:** If Channel 2 (within the XRT94L33) has been configured to operate in the ATM UNI/PPP Mode, then this input pin will function as the timing reference clock signal for the Transmit STS-1/DS3/E3 Framer block circuitry, provided that Channel 2 has been configured to operate in the Local Timing Mode. If Channel 2 has been configured to operate in the DS3 Mode, then the user is expected to apply a 44.736MHz clock signal to this input pin. Likewise, if Channel 2 has been configured to operate in the E3 Mode, then the user is expected to apply a 34.368MHz clock signal to this input pin. ***Note:*** *For more information on using the XRT94L33 for ATM UNI/PPP applications, the user should consult the XRT94L33 1-Channel STS-3c/3-Channel DS3/E3/STS-1 ATM UNI/PPP Data Sheet.*
B11 A22 AD16	TxOHClk_0 TxOHClk_1 TxOHClk_2	O	CMOS	**Transmit Overhead Clock Output:** This output pin functions as the “Transmit Overhead Clock” output for the transmit system side interface when the XRT94L33 is configured to operate in STS-1/DS3/E3 mode, however, it functions as the “Transmit STS-1 Overhead” clock output when the device is configured to operate in the STS-1 mode. **When configured to operate in DS3/E3 mode:** This output pin functions as the “Transmit Overhead Data Input Interface clock signal. If the user enables the “Transmit Overhead Data Input Interface” block by asserting the “TxOHIns” input pin, then the Transmit Overhead Data Input Interface block will sample and latch the data (residing on the “TxOH_n” input pin) upon the falling edge of this signal. **When configured to operate in STS-1 mode:** These output pins, along with “TxOH_n”, “TxOHEnable_n”, “TxOHIns_n” and “TxOHFrame” function as the “Transmit Path Overhead (TxOH) Input Port”. The “TxOHFrame” and “TxOHEnable” output pins are updated upon the falling edge this clock output signal. The “TxOHIns_n” input pins and the data residing on the “TxOH_n” input pins are sampled upon the falling edge of this clock signal.

D12 C18 AC16	TxOHENABLE_0 TxOHENABLE_1 TxOHENABLE_2	O	CMOS	**Transmit Overhead Enable Output indicator** This output pin functions as the "Transmit Overhead Enable" output indicator for the transmit system side interface when the XRT94L33 is configured to operate in STS-1/DS3/E3 mode, however, it functions as the "Transmit STS-1 Overhead Enable" output when the device is configured to operate in the STS-1 mode. **When configured to operate in DS3/E3 mode:** The Channel will assert this output pin, for one "TxInClk" period, just prior to the instant that the Transmit Overhead Data Input Interface will be sampling and processing an overhead bit. If the local terminal equipment intends to insert its own value for an overhead bit, into the outbound DS3 or E3 data stream, then it is expected to sample the state of this signal, upon the falling edge of "TxInClk". Upon sampling the "TxOHEnable_n" signal high, the local terminal equipment should (1) place the desired value of the overhead bit, onto the "TxOH_n" input pin and (2) assert the "TxOHIns_n" input pin. The Transmit Overhead Data Input Interface block will sample and latch the data on the "TxOH_n" signal, upon the rising edge of the very next "TxInClk_n" input signal. **When configured to operate in STS-1 mode:** These output pins, along with "TxOH_n", "TxOHIns_n", "TxOHFrame_n" and "TxOHClk_n" function as the "Transmit Path Overhead (TxOH) Input Port". These output pins will pulse "high" anytime the "TxOH" port is ready to accept and process POH bytes. These output pins will be "low" at all other times.

E12 E17 AB16	TxOH_0 TxOH_1 TxOH_2	I	TTL	**Transmit Overhead Data Input:** This input pin functions as the "Transmit Overhead Data" output indicator for the transmit system side interface when the XRT94L33 is configured to operate in STS-1/DS3/E3 mode, however, it functions as the "Transmit STS-1 Overhead Enable" output when the device is configured to operate in the STS-1 mode. **When configured to operate in DS3/E3 mode:** The Transmit Overhead Data Input Interface accepts overhead via these input pins, and insert this data into the "overhead" bit positions within the outbound DS3 or E3 frames. If the "TxOHIns_n" input pin is pulled "high", then the Transmit Overhead Data Input Interface will sample the overhead data, via this input pin, upon the falling edge of the TxOHClk_n output signal. Conversely, if the TxOHIns_n input pin is NOT pulled "high", then the Transmit Overhead Data Input Interface block will be inactive and will not accept any overhead data via the TxOH_n input pin. **When configured to operate in STS-1 mode:** These input pins permit the user to do the following. 1. To insert the POH data into each of the 3 Transmit STS-1 POH Processor blocks (for insertion and transmission via each of the "outbound" STS-1 signals). 2. To insert the TOH data into each of the 3 Transmit STS-1 TOH Processor blocks (for insertion and transmission via each of the "outbound" STS-1 signals). The exact function of these input pins, depend upon whether the user have opted to insert the TOH data into the 3 Transmit STS-1 TOH Processor blocks, or not.

E12 E17 AB16	TxOH_0 TxOH_1 TxOH_2	I	TTL	**Continued** **If the user is only inserting POH data via these input pins:** In this mode, the external circuitry (which is being interfaced to the "Transmit Path Overhead Input Port" is suppose to monitor the following output pins. • TxOHFrame_n • TxOHEnable_n • TxOHClk_n The "TxOHFrame_n" output pin will toggle "high" upon the falling edge of "TxOHClk_n" approximately one "TxOHClk_n" period prior to the "TxOH" port being ready to accept and process the first bit within J1 byte (e.g., the first POH byte). The "TxOHFrame_n" output pin will remain "high" for eight consecutive "TxOHClk_n" periods. The external circuitry should use this pin to note STS-1 SPE frame boundaries. The "TxOHEnable_n" output pin will toggle "high" upon the falling edge of "TxOHClk_n" approximately one "TxOHClk_n" period prior to the "TxOH" port being ready to accept and process the first bit within a given POH byte. If the user wishes to externally insert a given POH byte; (1) assert the "TxOHIns_n" input pin by toggling it "high", and **(2)** place the value of the first bit (within this particular POH byte) on this input pin upon the very next falling edge of "TxOHClk_n". This data bit will be sampled upon the very next falling edge of "TxOHClk_n". The external circuitry should continue to keep the "TxOHIns_n" input pin "high" and advancing the next bits (within the POH bytes) upon each rising edge of "TxOHClk_n".

E12 E17 AB16	TxOH_0 TxOH_1 TxOH_2	I	TTL	**Continued** **If the user is inserting both POH and TOH data via these input pins:** In this mode, the external circuitry (which is being interfaced to the "Transmit Path Overhead Input Port" is suppose to monitor the following output pins. • TxOHFrame_n • TxOHEnable_n • TxOHClk_n The "TxOHFrame_n" output pin will toggle "high" twice during a given STS-1 frame period. First, this output pin will toggle high coincident with the "TxOH" port being ready to accept and process the A1 byte (e.g., the very first TOH byte). Second, this output pin will toggle "high" coincident with the "TxOH" port being ready to accept and process the J1 byte (e.g., the very first POH byte). If the externally circuitry samples the "TxOHFrame_n" output pin "high", and the "TxOHEnable_n" output pin "low", then the "TxOH" port is now ready to accept and process the very first TOH byte. If the externally circuitry samples the "TxOHFrame_n" output pin "high" and the "TxOHEnable_n" output pin "high", then the "TxOH" port is now ready to accept and process the very first POH byte. To externally insert a given POH or TOH byte; (1) assert the "TxOHIns_n" input pin by toggling it "high", and (2) place the value of the first bit (within this particular POH or TOH byte) on this input upon the very next falling edge of "TxOHClk_n" This data bit will be sampled upon the very next falling edge of "TxOHClk_n". The external circuitry should continue to keep the "TxOHIns_n" input pin "high" and advancing the next bits (within the POH bytes) upon each rising edge of "TxOHClk_n".

F12 B19 AG19	TxOHINS_0 TxOHINS_1 TxOHINS_2	I	TTL	**Transmit Overhead Data Insert Input:** This input pin functions as the "Transmit Overhead Data Insert" input indicator for the transmit system side interface when the XRT94L33 is configured to operate in STS-1/DS3/E3 mode, however, it functions as the "Transmit STS-1 Overhead Enable" output when the device is configured to operate in the STS-1 mode. **When configured to operate in DS3/E3 mode:** This input pin permits the user to either enable or disable the "Transmit Overhead Data Input Interface" block within the DS3/E3 Frame Generator block. If the Transmit Overhead Data Input Interface block is enabled, then the DS3/E3 Frame Generator block will accept overhead data (from the local terminal equipment) via the "TxOH_n" input pin; and insert this data into the overhead bit positions within the outbound DS3 or E3 data stream. Conversely, if the Transmit Overhead Data Input Interface block is disabled, then the DS3/E3 Frame Generator block it will NOT accept overhead data from the local terminal equipment. Pulling this input pin "high" enables the "Transmit Overhead Data Input Interface" block. Pulling this input pin "low" disables the "Transmit Overhead Data Input Interface" block **When configured to operate in STS-1 mode:** These input pins, along with "TxOH_n", "TxOHEnable_n", "TxOHFrame_n" and "TxOHClk_n" function as the "Transmit Overhead (TxOH) Input Port. These input pins permit the user to enable or disable the "TxOH" input port. If these input pins are pulled "high", then the "TxOH" port will sample and latch data via the corresponding "TxOH" input pins, upon the falling edge of "TxOHClk_n". Conversely, if these input pins are pulled "low", then the "TxOH" port will NOT sample and latch data via the corresponding "TxOH" input pins. ***Note:*** *If the "TxOHIns_n" input pin is pulled "LOW", this setting will be overridden if the user has configured the "Transmit SONET/STS-1 POH Processor" or "Transmit STS-1 TOH Processor" blocks to accept certain POH or TOH overhead bytes via the external port.*

A9 D17 AF18	TxOHFRAME_0 TxOHFRAME_1 TxOHFRAME_2	O	CMOS	**Transmit Overhead Framing Pulse:** This input pin functions as the "Transmit Overhead Framing" Pulse for the transmit system side interface when the XRT94L33 is configured to operate in DS3/E3 mode, however, it functions as the "Transmit STS-1 Overhead Enable" output when the device is configured to operate in the STS-1 mode. **When configured to operate in DS3/E3 mode:** This output pin pulses high (for one TxOHClk_n" period) coincident with the instant that the DS3/E3 Frame Generator block will be accepting the very first overhead bit within an outbound DS3 or E3 frame (via Transmit Overhead Data Input Interface). **When configured to operate in STS-1 mode:** These output pins, along with the "TxOH_n", "TxOHEnable_n", "TxOHIns_n" and "TxOHClk_n" function as the "Transmit Overhead Input Port". The exact function of these output pins depends upon whether the user inserting POH or TOH data via the "TxOH_n" input pins. **If the user is only inserting POH data via these input pins:** In this mode, the "TxOH" port will pulse these output pins "high" whenever it is ready to accept and process the J1 byte (e.g., the very first POH byte) via this port. **If the user is inserting both POH and TOH data via these input pins:** In this mode, the "TxOH" port will pulse these output pins "high" coincident with the following. Whenever the "TxOH" port is ready to accept and process the A1 byte (e.g., the very first TOH byte) via this port. Whenever the "TxOH" port is ready to accept and process the J1 byte (e.g., the very first POH byte) via this port. ***Notes:*** 1. The externally circuitry can determine whether the "TxOH" port is expecting the A1 byte or the J1 byte, by checking the state of the corresponding "TxOHEnable" output pin. If the "TxOHEnable_n" output pin is "LOW" while the "TxOHFrame_n" output pin is "HIGH", then the "TxOH" port is ready to process the A1 (TOH) bytes. 2. If the "TxOHEnable_n" output pin is "HIGH" while the "TxOHFrame_n" output pin is "HIGH", then the "TxOH" port is ready to process the J1 (POH) bytes.

AF19 AG21 AE17	STUFFCNTL_0/ TXHDLC_CLK_0/ STUFFCNTL_1/ TXHDLC_CLK_1/ STUFFCNTL_2/ TXHDLC_CLK_2/	I/O	TTL/CMOS	**Transmit PLCP Processor Block – Nibble Trailer Stuff Control Input pin/Transmit High-Speed HDLC Controller Input Interface – Clock Output pin – Channel n:** The exact function of this input pin depends upon (1) whether the XRT94L33 has been configured to operate in the ATM UNI/PLCP Mode and (2) whether a given DS3/E3 Framer block/Channel has been configured to operate in the "High-Speed HDLC Controller" Mode, as described below. **ATM UNI Mode - STUFFCNT_n: Transmit PLCP Processor block Nibble-Trailer Stuff Control Input pin – Channel n - STUFFCNT_n:** This pin only functions in this particular role if the XRT94L33 has been configured to operate in the ATM UNI Mode. For more information on this pin operating in this mode, please see the XRT94L33 Pin Description for ATM UNI/PPP Applications. **High-Speed HDLC Controller Mode – Transmit HDLC Controller Input Interace Block - Clock output signal – Channel n – TxHDLCClk_n:** This output signal functions as the "demand" clock for the Transmit High-Speed HDLC Controller Input Interface block, associated with the DS3/E3 Framer blocks. Whenever the user pulls the "Snd_Msg_n" input pin "high" then the Transmit High-Speed HDLC Controller block will begin to sample and latch the contents of the "TxHDLCDat[7:0] input pins upon the falling edge of this clock signal. The user is advised to configure their terminal equipment circuitry to output (or place) data onto the "TxHDLCDat[7:0] bus upon the rising edge of this clock signal. Since the Transmit HDLC Controller block is sampling and latching 8-bits of data at a given time, it may be assumed that the frequency of the TxHDLC_CLK_n output signal is either 34.368MHz/8 or 44.736MHz/8. In general, this presumption is true. However, because the Transmit HDLC Controller block is also performing "Zero-Stuffing" of the user data that it accepts from the Terminal Equipment, the frequency of this signal may be slower. ***Note:*** *The user should tie this pin to GND if the DS3/E3 Framer block has NOT been configured to operate in the "High-Speed HDLC Controller" Mode.*

AC17 AD17 AG20	EIGHTKHZSYNC_0/ RXHDLC_CLK_0/ EIGHTKHZSYNC_1/ RXHDLC_CLK_1/ EIGHTKHZSYNC_2/ RXHDLC_CLK_2/	I/O	TTL/CMOS	**Transmit PLCP Processor Block – 8kHz Framing Alignment Input/Receive High-Speed HDLC Controller Output Interface Block – Clock Output – Channel n:** The exact function of this input pin depends upon (1) whether the XRT94L33 has been configured to operate in the ATM UNI/PLCP Mode and (2) whether Channel n has been configured to operate in the "High-Speed HDLC Controller" Mode, as described below. **ATM UNI Mode - EIGHTKHZSYNC_n: Transmit PLCP Processor Block 8kHz Framing Alignment Input:** This pin only functions in this particular role if the XRT94L33 has been configured to operate in the ATM UNI Mode. For more information on this pin operating in this mode, please see the XRT94L33 Pin Description for ATM UNI/PPP Applications. **High-Speed HDLC Controller Mode - Receive High-Speed HDLC Controller Output Interface Block - Clock output signal – Channel n – RxHDLCClk_n:** This output pin functions as the "Receive High-Speed HDLC Controller Output Interface block – clock output signal for Channel n. The Receive High-Speed HDLC Controller Output Interface block outputs the contents of all received HDLC frames and flag sequence octets via the Receive High-Speed HDLC Controller Output Interface block – Data Bus output pins (RxHDLCDat_n[7:0]) upon the rising edge of this clock signal. The user is advised to configure the terminal equipment to sample the contents of the RxHDLCDat_n[7:0] output pins upon the falling edge of this clock signal. ***Note:*** *The user should tie this pin to GND if the DS3/E3 Framer block has NOT been configured to operate in the "High-Speed HDLC Controller" Mode.*
D27	TXPERR	I	TTL	**For Mapper applications, please connect this pin to GND.**
G25	TxPEOP	I	TTL	**For Mapper applications, please connect this pin to GND.**
F25	TxMOD_0	I	TTL	**For Mapper applications, please connect this pin to GND.**
J24	TxUPRTY/ TxPPRTY	I	TTL	**For Mapper applications, please connect this pin to GND.**

H27 G27 L24 J26 L23 K25 F27 H26 G26 K24 J25 E27 K23 F26 H25 E26	TxUDATA_0/ TxPDATA_0 TxUDATA_1/ TxPDATA_1 TxUDATA_2/ TxPDATA_2 TxUDATA_3/ TxPDATA_3 TxUDATA_4/ TxPDATA_4 TxUDATA_5/ TxPDATA_5 TxUDATA_6/ TxPDATA_6 TxUDATA_7/ TxPDATA_7 TxUDATA_8/ TxPDATA_8 TxUDATA_9/ TxPDATA_9 TxUDATA_10/ TxPDATA_10 TxUDATA_11/ TxPDATA_11 TxUDATA_12/ TxPDATA_12 TxUDATA_13/ TxPDATA_13 TxUDATA_14/ TxPDATA_14 TxUDATA_15/ TxPDATA_15	I	TTL	**For Mapper applications, please connect these input pins to GND.**
M24 M23 J27 K26 L25	TxUADDR_0 TxUADDR_1 TxUADDR_2 TxUADDR_3 TxUADDR_4	I	TTL	**For Mapper applications, please connect these input pins to GND.**
L26	TxUClav/TxPPA	O	CMOS	**For Mapper applications, please leave this pin open.**
M25	TxUSOC/ TXPSOP/ TXPSOC	I	TTL	**For Mapper applications, please connect this pin to GND.**
K27	TxTSX / TXPSOF	I	TTL	**For Mapper applications, please connect this pin to GND.**
M26	TXUENB_L/ TXPENB_L	I	TTL	**For Mapper applications, please connect this pin to VDD.**
L27	TXUCLKO/ TXPCLKO	O	CMOS	**For Mapper applications, please leave this pin open.**
M27	TXUCLK/ TXPCLK	I	TTL	**For Mapper applications, please connect this pin to GND.**
STS-1 TELECOM BUS INTERFACE – TRANSMIT DIRECTION				

C14	STS1TXA_CK_0 TXSENDFCS_0 TXGFCCLK_0	I I O	TTL TTL CMOS	**STS-1 Transmit Telecom Bus Clock Input pin/Transmit HDLC Control Block Send FCS Command Input pin – Channel 0:** The exact function of this input pin depends upon whether the STS-1 Telecom Bus Interface for Channel 0 has been enabled or not. **If STS-1 Telecom Bus (Channel 0) has been enabled – STS1TXA_CLK_0 - "STS-1 Transmit Telecom Bus" Transmit Clock Input – Channel 0:** This input clock signal functions as the clock source for the STS-1 Transmit Telecom Bus, associated with Channel 0. All input signals (e.g., STS1TXA_ALARM_0, STS1TXA_D_0[7:0], STS1TXA_DP_0, STS1TXA_PL_0, STS1TXA_C1J1_0) are sampled upon the falling edge of this input clock signal. This clock signal should operate at 19.44MHz. (For STS-3 mode) or 6.48MHz (for STS-1 mode) **If STS-1 Telecom Bus (Channel 0) has NOT been enabled:** If STS-1 Telecom Bus (Channel 0) has not been enabled, then this particular pin can be configured to function in either of the following roles. **TXSENDFCS_0 (Transmit HDLC Controller block Send FCS Command Input – High Speed HDLC Controller Mode Only)** The user's terminal equipment is expected to control both this input pin and the "TXSENDMSG_0" input pin during the construction and transmission of each outbound HDLC frame. This input pin permits the user to command the Transmit HDLC Controller block to compute and insert the computed FCS value into the back-end of the "outbound" HDLC frame as a trailer. If the user has configured the Transmit HDLC Controller to compute and insert a CRC-16 value into the "outbound" HDLC frame, then the terminal equipment is expected to pull this input pin "high" for two periods of TxHDLCClk_0. Likewise, if the user has configured the Transmit HDLC Controller to compute and insert a CRC-32 value into the "outbound" HDLC frame, then the terminal equipment is expected to pull this input pin "high" for four periods of TxHDLCClk_0. **TXGFCCLK_0 (Transmit GFC Nibble-Field Input Port clock signal Input) – ATM Applications ONLY.** This pin only functions in this particular role if the XRT94L33 has been configured to operate in the ATM UNI Mode. ***Note:*** *The user should tie this pin to GND the DS3/E3 Framer block has NOT been configured to operate in the "High-Speed HDLC Controller" Mode.*

E19	STS1TXA_CK_1 TXSENDFCS_1 TXGFCCLK_1	I I O	TTL TTL CMOS	**STS-1 Transmit Telecom Bus Clock Input pin/Transmit HDLC Control Block Send FCS Command Input pin – Channel 1:** The exact function of this input pin depends upon whether the STS-1 Telecom Bus Interface for Channel 1 has been enabled or not. **If STS-1 Telecom Bus (Channel 1) has been enabled** – **STS1TXA_CLK_1 -** "STS-1 Transmit Telecom Bus" Clock Input – Channel 1: This input clock signal functions as the clock source for the STS-1 Transmit Telecom Bus, associated with Channel 1. All input signals, (e.g., STS1TXA_ALARM_1, STS1TXA_D_1[7:0], STS1TXA_DP_1, STS1TXA_PL_1, STS1TXA_C1J1_1) are sampled upon the falling edge of this input clock signal. This clock signal should operate at 19.44MHz. (For STS-3 mode) or 6.48MHz (for STS-1 mode) **If STS-1 Telecom Bus (Channel 1) has NOT been enabled:** If STS-1 Telecom Bus (Channel 1) has not been enabled, then this particular pin can be configured to function in either of the following roles. **TXSENDFCS_1 (Transmit HDLC Controller block Send FCS Command Input – High Speed HDLC Controller Mode Only)** The user's terminal equipment is expected to control both this input pin and the "TXSENDMSG_1" input pin during the construction and transmission of each outbound HDLC frame. This input pin permits the user to command the Transmit HDLC Controller block to compute and insert the computed FCS value into the back-end of the "outbound" HDLC frame as a trailer. If the user has configured the Transmit HDLC Controller to compute and insert a CRC-16 value into the "outbound" HDLC frame, then the terminal equipment is expected to pull this input pin "high" for two periods of TxHDLCClk_1. Likewise, if the user has configured the Transmit HDLC Controller to compute and insert a CRC-32 value into the "outbound" HDLC frame, then the terminal equipment is expected to pull this input pin "high" for four periods of TxHDLCClk_1. **TXGFCCLK_1 (Transmit GFC Nibble-Field Input Port clock signal Input) – ATM Applications ONLY.** This pin only functions in this particular role if the XRT94L33 has been configured to operate in the ATM UNI Mode. *NOTE: The user should tie this pin to GND if the DS3/E3 Framer block has NOT been configured to operate in the "High-Speed HDLC Controller" Mode.*

AC14	STS1TXA_CK_2 TXSENDFCS_2 TXGFCCLK_2	IO	TTL CMOS CMOS	**STS-1 Transmit Telecom Bus Clock Input pin/Transmit HDLC Control Block Send FCS Command Input pin – Channel 2:** The exact function of this input pin depends upon whether the STS-1 Telecom Bus Interface for Channel 2 has been enabled or not. **If STS-1 Telecom Bus (Channel 2) has been enabled** – **STS1TXA_CLK_2 –** "STS-1 Transmit Telecom Bus" Transmit Clock Input – Channel 2: This input clock signal functions as the clock source for the STS-1 Transmit Telecom Bus, associated with Channel 2. All input signals, (e.g., STS1TXA_ALARM_2, STS1TXA_D_2[7:0]", STS1TXA_DP_2, STS1TXA_PL_2, STS1TXA_C1J1_2) are sampled upon the falling edge of this input clock signal. This clock signal should operate at 19.44MHz. (For STS-3 mode) or 6.48MHz (for STS-1 mode) **If STS-1 Telecom Bus (Channel 1) has NOT been enabled:** If STS-1 Telecom Bus (Channel 1) has not been enabled, then this particular pin can be configured to function in either of the following roles. **TXSENDFCS_2 (Transmit HDLC Controller block Send FCS Command Input – High Speed HDLC Controller Mode Only)** The user's terminal equipment is expected to control both this input pin and the "TXSENDMSG_2" input pin during the construction and transmission of each outbound HDLC frame. This input pin permits the user to command the Transmit HDLC Controller block to compute and insert the computed FCS value into the back-end of the "outbound" HDLC frame as a trailer. If the user has configured the Transmit HDLC Controller to compute and insert a CRC-16 value into the "outbound" HDLC frame, then the terminal equipment is expected to pull this input pin "high" for two periods of TxHDLCClk_2. Likewise, if the user has configured the Transmit HDLC Controller to compute and insert a CRC-32 value into the "outbound" HDLC frame, then the terminal equipment is expected to pull this input pin "high" for four periods of TxHDLCClk_2. **TXGFCCLK_2 (Transmit GFC Nibble-Field Input Port clock signal Input) – ATM Applications ONLY.** This pin only functions in this particular role if the XRT94L33 has been configured to operate in the ATM UNI Mode. *NOTE: The user should tie this pin to GND if the DS3/E3 Framer block has NOT been configured to operate in the "High-Speed HDLC Controller" Mode.*

E14	STS1TXA_PL_0 TXSENDMSG_0	I	TTL	**STS-1 Transmit Telecom Bus – Payload Indicator Signal input/Transmit HDLC Controller block Send Message Command Input pin – Channel 0:** The exact function of this input depends upon whether the STS-1 Telecom Bus Interface for Channel 0 has been enabled or not. **If STS-1 Telecom Bus (Channel 0) has been enabled – STS1TXA_PL_0 - STS-1 Transmit Telecom Bus – Payload Indicator Signal – Channel 0:** This input pin indicates whether or not "Transport Overhead" (TOH) bytes are being input via the "TXA_D_0[7:0]" input pins. This input pin should be pulled "low" for the duration that the "STS-1 Transmit Telecom Bus is receiving a TOH byte, via the "TXA_D_0[7:0]" input pins. Conversely, this input pin should be pulled "high" at all other times. ***Note:*** *This input signal is sampled upon the falling edge of "STS1TXA_CK_0".* **If STS-1 Telecom Bus (Channel 0) has NOT been enabled:** If STS-1 Telecom Bus (Channel 0) has not been enabled, then this particular pin can either be configured to function as the "TxSENDMSG_0" input pin (if the DS3/E3 Framer block within Channel 0 has been configured to operate in the "High-Speed HDLC Controller Mode), or the user should simply tie this input pin to GND. The details of this pin's role as the "TxSENDMSG_0" input pin is described below. **TXSENDMSG_0 (Transmit HDLC Controller block Send Message Command Input – High Speed HDLC Controller Mode Only)** This input pin permits the user to command the Transmit HDLC Controller block (associated with Channel 0) to begin sampling and latching the data which is being applied to the "TxHDLCDat_0[7:0]" input pins. If the user pulls this input pin "high", then the Transmit HDLC Controller block samples and latches the data which is applied to the "TxHDLCDat_0[7:0]" input pins upon the rising edge of "TxHDLCClk_0". Each byte of this sampled data will ultimately be encapsulated into an outbound HDLC frame and will be mapped into the payload bits within the outbound DS3/E3 frames via the DS3/E3 Framer Generator block. If the user pulls this input pin "low" then the Transmit HDLC Controller block will NOT sample and latch the contents on the "TxHDLCDat_0[7:0]" input pins, and the Transmit HDLC Controller block will simply generate a continuous stream of flag sequence octets (0x7E). ***Note:*** *The user should tie this pin to GND if the DS3/E3 Framer block* has NOT been configured *to operate in the "High-Speed HDLC Controller" Mode.*

C22	STS1TXA_PL_1 TXSENDMSG_1:	I	TTL	***STS-1 Transmit Telecom Bus – Payload Indicator Signal input/Transmit HDLC Controller block Send Message Command Input pin – Channel 1:*** *The exact function of this input pin depends upon whether the STS-1 Telecom Bus Interface for Channel 1 has been enabled or not.* ***If STS-1 Telecom Bus (Channel 1) has been enabled – STS1TXA_PL_1 - STS-1 Transmit Telecom Bus – Payload Indicator Signal – Channel 1:*** *This input pin indicates whether or not "Transport Overhead" (TOH) bytes are being input via the "TXA_D_1[7:0]" input pins.* *This input pin should be pulled "low" for the duration that the STS-1 Transmit Telecom Bus is receiving a TOH byte, via the "TXA_D_1[7:0]" input pins. Conversely, this input pin should be pulled "high" at all other times.* ***Note:*** *This input signal is sampled upon the falling edge of "STS1TXA_CK_1".* ***If STS-1 Telecom Bus (Channel 1) has NOT been enabled:*** *If STS-1 Telecom Bus (Channel 1) has not been enabled, then this particular pin can either be configured to function as the "TxSENDMSG_1" input pin (if the DS3/E3 Framer block within Channel 1 has been configured to operate in the "High-Speed HDLC Controller Mode), or the user should simply tie this input pin to GND. The details of this pin's role as the "TxSENDMSG_1" input pin is described below.* ***TXSENDMSG_1 (Transmit HDLC Controller block Send Message Command Input – High Speed HDLC Controller Mode ONLY)*** *This input pin permits the user to command the Transmit HDLC Controller block (associated with Channel 1) to begin sampling and latching the data which is being applied to the "TxHDLCDat_1[7:0]" input pins.* *If the user pulls this input pin "high", then the Transmit HDLC Controller block samples and latches the data which is applied to the "TxHDLCDat_1[7:0]" input pins upon the rising edge of "TxHDLCClk_1". Each byte of this sampled data will ultimately be encapsulated into an outbound HDLC frame and will be mapped into the payload bits within the outbound DS3/E3 frames via the DS3/E3 Frame Generator block.* *If the user pulls this input pin "low" then the Transmit HDLC Controller block will NOT sample and latch the contents on the "TxHDLCDat_1[7:0]" input pins, and the Transmit HDLC Controller block will simply generate a continuous stream of flag sequence octets (0x7E).* ***Note:*** *The user should tie this pin to GND if the DS3/E3 Framer block has NOT been configured to operate in the "High-Speed HDLC Controller" Mode.*

AD14	STS1TXA_PL_2 TXSENDMSG_2:	I	TTL	***STS-1 Transmit Telecom Bus – Payload Indicator Signal input/Transmit HDLC Controller block Send Message Command Input pin – Channel 2:*** *The exact function of this input pin depends upon whether the STS-1 Telecom Bus Interface for Channel 2 has been enabled or not.* ***If STS-1 Telecom Bus (Channel 2) has been enabled** – STS-1 Transmit Telecom Bus – Payload Indicator Signal – Channel 2:* *This input pin indicates whether or not "Transport Overhead" (TOH) bytes are being input via the "TXA_D_2[7:0]" input pins.* *This input pin should be pulled "low" for the duration that the STS-1 Transmit Telecom Bus is receiving a TOH byte, via the "TXA_D_2[7:0]" input pins. Conversely, this input pin should be pulled "high" at all other times.* ***Note:** This input signal is sampled upon the falling edge of "STS1TXA_CK_2".* ***If STS-1 Telecom Bus (Channel 2) has NOT been enabled:*** *If STS-1 Telecom Bus (Channel 2) has not been enabled, then this particular pin can either be configured to function as the "TxSENDMSG_2" input pin (if the DS3/E3 Framer block within Channel 2 has been configured to operate in the "High-Speed HDLC Controller Mode), or the user should simply tie this input pin to GND. The details of this pin's role as the "TxSENDMSG_2" input pin is described below.* ***TXSENDMSG_2 (Transmit HDLC Controller block Send Message Command Input – High Speed HDLC Controller Mode ONLY)*** *This input pin permits the user to command the Transmit HDLC Controller block (associated with Channel 2) to begin sampling and latching the data which is being applied to the "TxHDLCDat_2[7:0]" input pins.* *If the user pulls this input pin "high", then the Transmit HDLC Controller block samples and latches the data which is applied to the "TxHDLCDat_2[7:0]" input pins upon the rising edge of "TxHDLCClk_2". Each byte of this sampled data will ultimately be encapsulated into an outbound HDLC frame and will be mapped into the payload bits within the outbound DS3/E3 frames via the DS3/E3 Frame Generator block.* *If the user pulls this input pin "low" then the Transmit HDLC Controller block will NOT sample and latch the contents on the "TxHDLCDat_2[7:0]" input pins, and the Transmit HDLC Controller block will simply generate a continuous stream of flag sequence octets (0x7E).* ***Note:** The user should tie this pin to GND if the DS3/E3 Framer block has NOT been configured to operate in the "High-Speed HDLC Controller" Mode.*

D14	STS1TXA_C1J1_0 RXDS3LINECLK_0	I	TTL	**STS-1 Transmit Telecom Bus C1/J1 Byte Phase Indicator Input Signal/Receive DS3/E3/STS-1 Clock Input from LIU (Channel 0):** The exact function of this pin depends upon whether the STS-1 Telecom Bus Interface for Channel 0 has been enabled or not. **If STS-1 Telecom Bus (Channel 0) has been enabled - STS-1 Transmit Telecom Bus C1/J1 Byte Phase Indicator Input Signal (Channel 0):** This input pin should be pulsed “high” during both of the following conditions. Whenever the C1 byte is being input to the STS-1 Transmit Telecom Bus (TXA_D_0[7:0]) input pins. Whenever the J1 byte is being input to the STS-1 Transmit Telecom Bus (TXA_D_0[7:0]) input pins. This input pin should be pulled “low” at all other times. **If STS-1 Telecom Bus (Channel 0) has NOT been enabled - RXDS3LINECLK_0 (Receive DS3/E3/STS-1 clock input from LIU)** The DS3/E3 Framer block and the Receive STS-1 TOH Processor block (associated with Channel 0) uses this input pin to sample and latch the data that is present on the RxDS3POS_0 and RxDS3NEG_0 (for Dual-Rail Operation only) inputs. This input clock signal also functions as the timing source for the Ingress Direction signal and circuitry within the DS3/E3 Framer block of Channel 0. The user is expected to connect this input to the Recovered Clock Output of a DS3/E3/STS-1 LIU IC.

A24	STS1TXA_C1J1_1 RXDS3LINECLK_1/ RxSTS1LineClk_1	I	TTL	**Transmit STS-1 Telecom Bus Interface - C1/J1 Byte Phase Indicator Input Signal – Channel 1/Receive DS3/E3/STS-1 Clock Input from LIU – Channel 1:** The exact function of this pin depends upon whether the STS-1 Telecom Bus Interface for Channel 1 has been enabled or not. **If the STS-1 Telecom Bus (Channel 1) has been enabled - Transmit STS-1 Telecom Bus Interface - C1/J1 Byte Phase Indicator Input Signal (Channel 1):** This input pin should be pulsed “high” during both of the following conditions. Whenever the C1 byte is being input to the Transmit STS-1 Telecom Bus Interface input pins (TXA_D_1[7:0]). Whenever the J1 byte is being input to the Transmit STS-1 Telecom Bus Interface input pins (TXA_D_1[7:0]). This input pin should be pulled “low” at all other times. **If the STS-1 Telecom Bus (Channel 1) has NOT been enabled - RXDS3LINECLK_1 (Receive DS3/E3/STS-1 clock input from LIU)** The DS3/E3 Framer block and the Receive STS-1 TOH Processor block (associated with Channel 1) uses this input pin to sample and latch the data that is present on the RxDS3POS_1 and RxDS3NEG_1 (for Dual-Rail Operation only) inputs. This input clock signal also functions as the timing source for the Ingress Direction signal and circuitry within the DS3/E3 Framer block of Channel 1. The user is expected to connect this input to the Recovered Clock Output pin of an off chip DS3/E3/STS-1 LIU IC.

AF14	STS1TXA_C1J1_2 RXDS3LINECLK_2	I	TTL	**STS-1 Transmit Telecom Bus C1/J1 Byte Phase Indicator Input Signal/Receive DS3/E3/STS-1 Clock Input from LIU (Channel 2):** The exact function of this pin depends upon whether the STS-1 Telecom Bus Interface for Channel 2 has been enabled or not. **If STS-1 Telecom Bus (Channel 2) has been enabled** - STS-1 Transmit Telecom Bus C1/J1 Byte Phase Indicator Input Signal (Channel 2): This input pin should be pulsed “high” during both of the following conditions. Whenever the C1 byte is being input to the STS-1 Transmit Telecom Bus (TXA_D_2[7:0]) input pins. Whenever the J1 byte is being input to the STS-1 Transmit Telecom Bus (TXA_D_2[7:0]) input pins. This input pin should be pulled “low” at all other times. **Is STS-1 Telecom Bus (Channel 2) has NOT been enabled - RXDS3LINECLK_2 (Receive DS3/E3/STS-1 clock input from LIU)** The DS3/E3 Framer block and the Receive STS-1 TOH Processor block (associated with Channel 2) uses this input pin to sample and latch the data that is present on the RxDS3POS_2 and RxDS3NEG_2 (for Dual-Rail Operation only) inputs. This input clock signal also functions as the timing source for the Ingress Direction signal and circuitry within the DS3/E3 Framer block of Channel 2. The user is expected to connect this input to the Recovered Clock Output of a DS3/E3/STS-1 LIU IC.

B14	STS1TXA_DP_0 RXDS3POS_0	I	TTL	**STS-1 Transmit Telecom Bus – Parity Input pin/Receive DS3/E3/STS-1 Positive-Polarity Data Input from LIU – Channel 0:** The exact function of this pin depends upon whether the STS-1 Telecom Bus Interface for Channel 0 has been enabled or not. **If STS-1 Telecom Bus (Channel 0) has been enabled – STS1TXA_DP_0 - STS-1 Transmit Telecom Bus Interface # 0 – Parity Input Pin:** This input pin can be configured to function as one of the following. The EVEN or ODD parity value of the bits which are input via the "STS1TXA_D_0[7:0]" input pins. The EVEN or ODD parity value of the bits which are being input via the "STS1TXA_D_0[7:0]" input, and the states of the "STS1TXA_PL_0" and "STS1TXA_C1J1_0" input pins. ***Note:*** *The user can make any one of these configuration selections by writing the appropriate value into the "Interface Control Register – Byte 0" register (Address Location = 0x013B).* **If STS-1 Telecom Bus (Channel 0) has NOT been enabled - RXDS3POS_0 (Receive DS3/E3/STS-1 Positive-Polarity data input from LIU)** The DS3/E3 Framer block and the Receive STS-1 TOH Processor block (associated with Channel 0) will sample the data being applied to this input pin upon the user-selected edge of the "RXDS3LINECLK_0" input signal. If the user has configured Channel 0 to operate in the STS-1 Mode, or in the Single-Rail Mode (if also configured to operate in the DS3/E3 Mode), then all Recovered DS3, E3 or STS-1 data (from the DS3/E3/STS-1 LIU IC) should be applied to this input pin. If the user has configured Channel 0 to operate in both the DS3/E3 and the Dual-Rail Mode, then only the "positive-polarity" portion of the Recovered DS3/E3 data should be applied to this input pin.

C21	STS1TXA_DP_1 RXDS3POS_1	I	TTL	**STS-1 Transmit Telecom Bus – Parity Input pin/Receive DS3/E3/STS-1 Positive-Polarity Data Input from LIU – Channel 1:** The exact function of this input pin depends upon whether STS-1 Telecom Bus Interface # 1 has been enable or not. **If STS-1 Telecom Bus (Channel 1) has been enabled – STS1TXA_DP_1: STS-1 Transmit Telecom Bus Interface # 1 – Parity Input pin:** This input pin can be configured to function as one of the following. The EVEN or ODD parity value of the bits which are input via the "STS1TXA_D_1[7:0]" input pins. The EVEN or ODD parity value of the bits which are being input via the "STS1TXA_D_1[7:0]" input and the states of the "STS1TXA_PL_1" and "STS1TXA_C1J1_1" input pins. ***Note:*** *The user can make any one of these configuration selections by writing the appropriate value into the "Interface Control Register – Byte 1" register (Address Location = 0x013A).* **If STS-1 Telecom Bus (Channel 1) has NOT been enabled - RXDS3POS_1 (Receive DS3/E3/STS-1 Positive-Polarity data input from LIU – Channel 1)** The DS3/E3 Framer block and the Receive STS-1 TOH Processor block (associated with Channel 1) will sample the data being applied to this input pin upon the user-selected edge of the "RXDS3LINECLK_1" input signal. If the user has configured Channel 1 to operate in the STS-1 Mode, or in the Single-Rail Mode (if also configured to operate in the DS3/E3 Mode), then all Recovered DS3, E3 or STS-1 data (from the DS3/E3/STS-1 LIU IC) should be applied to this input pin. If the user has configured Channel 1 to operate in both the DS3/E3 and the Dual-Rail Mode, then only the "positive-polarity" portion of the Recovered DS3/E3 data should be applied to this input pin.

AG15	STS1TXA_DP_2 RXDS3POS_2	I	TTL	**STS-1 Transmit Telecom Bus – Parity Input pin/Receive DS3/E3/STS-1 Positive-Polarity Data Input from LIU – Channel 2;** The exact function of this pin depends upon whether the STS-1 Telecom Bus Interface for Channel 2 has been enabled or not. **If STS-1 Telecom Bus (Channel 2) has been enabled – STS1TXA_DP_2: STS-1 Transmit Telecom Bus Interface # 2 – Parity Input Pin:** This input pin can be configured to function as one of the following. The EVEN or ODD parity value of the bits which are input via the "STS1TXA_D_2[7:0]" input pins. The EVEN or ODD parity value of the bits which are being input via the "STS1TXA_D_2[7:0]" input and the states of the "STS1TXA_PL_2" and "STS1TXA_C1J1_2" input pins. ***Note:*** *The user can make any one of these configuration selections by writing the appropriate value into the "Interface Control Register – Byte 2" register (Address Location = 0x0139).* **If STS-1 Telecom Bus (Channel 2) has NOT been enabled RXDS3POS_2 (Receive DS3/E3/STS-1 Positive-Polarity data input from LIU)** The DS3/E3 Framer block and the Receive STS-1 TOH Processor block (associated with Channel 2) will sample the data being applied to this input pin upon the user-selected edge of the "RXDS3LINECLK_2" input signal. If the user has configured Channel 2 to operate in the STS-1 Mode, or in the Single-Rail Mode (if also configured to operate in the DS3/E3 Mode), then all Recovered DS3, E3 or STS-1 data (from the DS3/E3/STS-1 LIU IC) should be applied to this input pin. If the user has configured Channel 2 to operate in both the DS3/E3 and the Dual-Rail Mode, then only the "positive-polarity" portion of the Recovered DS3/E3 data should be applied to this input pin.

A13	STS1TXA_ALARM_0 RXDS3NEG_0 RxLCV_0	I	TTL	**Transmit STS-1 Telecom Bus – Alarm Indicator Input/Receive DS3/E3 Negative-Polarity Data Input from LIU/Receive DS3/E3 Line Code Violation Input from LIU – Channel 0;** The exact function of this pin depends upon whether the STS-1 Telecom Bus Interface for Channel 0 has been enabled or not. **If STS-1 Telecom Bus (Channel 0) has been enabled** – STS-1 Transmit Telecom Bus – Alarm Indicator Input: This input pin pulses "high" coincident to any STS-1 signal (which is carrying the AIS-P indicator) being applied to the STS1TXA_D_0[7:0] input data bus. ***Note:*** *If the STS1TXA_ALARM_0 input signal pulses "HIGH" for any given STS-1 signal (within the "incoming" STS-1), then the XRT94L33 will automatically declare the AIS-P defect condition for that particular STS-1 channel.* **If STS-1 Telecom Bus (Channel 0) has NOT been enabled:** If the STS-1 Telecom Bus (Channel 0) has NOT been enabled, then the role that this particular input pin plays depends upon whether Channel 0 is operating in the STS-1 Mode, the DS3/E3 Single-Rail Mode or in the DS3/E3 Dual-Rail Mode, as described below. **If Channel 0 is operating in the STS-1 Mode** If Channel 0 is operating in the STS-1 Mode, then the user should tie this pin to GND. **If Channel 0 is operating in the DS3/E3 Single-Rail Mode – Receive LCV Input from LIU** If Channel 0 is operating in both the DS3/E3 and Single-Rail Modes, then this input pin will function as the LCV (Line Code Violation) input. In this mode, the user is expected to connect the "LCV" output pin from the LIU IC to this input pin. The DS3/E3 Framer block will sample this input pin upon the "user-configured" edge of the "RXDS3LINECLK_0" clock signal, and the Primary Frame Synchronizer block (corresponding with Channel 0) will increment the PMON LCV or EXZ Event Count registers based upon the data sampled at this input pin. **If Channel 0 is operating in the DS3/E3 Dual-Rail Mode – Receive DS3/E3 Negative-Polarity Data Input from LIU** If the user has configured Channel 0 to operate in both the DS3/E3 and the Dual-Rail Mode, then only the "negative-polarity" portion of the Receive DS3/E3 data should be applied to this input pin.

D19	STS1TXA_ALARM_1 RXDS3NEG_1 RxLCV_1	I	TTL	**Transmit STS-1 Telecom Bus – Alarm Indicator Input/Receive DS3/E3 Negative-Polarity Data Input from LIU/Receive DS3/E3 Line Code Violation Input from LIU – Channel 1:** The exact function of this pin depends upon whether the STS-1 Telecom Bus Interface for Channel 1 has been enabled or not. **If STS-1 Telecom Bus (Channel 1) has been enabled** – STS-1 Transmit Telecom Bus – Alarm Indicator Input: This input pin pulses "high" coincident to any STS-1 signal (which is carrying the AIS-P indicator) being applied to the STS1TXA_D_1[7:0] input data bus. ***Note:*** *If the STS1TXA_ALARM_1 input signal pulses "HIGH" for any given STS-1 signal (within the "incoming" STS-1), then the XRT94L33 will automatically declare the AIS-P defect condition for that particular STS-1 channel.* **If STS-1 Telecom Bus (Channel 1) has NOT been enabled:** If the STS-1 Telecom Bus (Channel 1) has NOT been enabled, then the role that this particular input pin plays depends upon whether Channel 1 is operating in the STS-1 Mode, the DS3/E3 Single-Rail Mode or in the DS3/E3 Dual-Rail Mode, as described below. **If Channel 1 is operating in the STS-1 Mode** If Channel 1 is operating in the STS-1 Mode, then the user should tie this pin to GND. **If Channel 1 is operating in the DS3/E3 Single-Rail Mode – Receive LCV Input from LIU** If Channel 1 is operating in both the DS3/E3 and Single-Rail Modes, then this input pin will function as the LCV (Line Code Violation) input. In this mode, the user is expected to connect the "LCV" output pin from the LIU IC to this input pin. The DS3/E3 Framer block will sample this input pin upon the "user-configured" edge of the "RXDS3LINECLK_1" clock signal, and the Primary Frame Synchronizer block (corresponding with Channel 1) will increment the PMON LCV or EXZ Event Count registers based upon the data sampled at this input pin. **If Channel 1 is operating in the DS3/E3 Dual-Rail Mode – Receive DS3/E3 Negative-Polarity Data Input from LIU** If the user has configured Channel 1 to operate in both the DS3/E3 and the Dual-Rail Mode, then only the "negative-polarity" portion of the Receive DS3/E3 data should be applied to this input pin.

AF15	STS1TXA_ALARM_2 RXDS3NEG_2 RxLCV_2	I	TTL	**Transmit STS-1 Telecom Bus – Alarm Indicator Input/Receive DS3/E3 Negative-Polarity Data Input from LIU/Receive DS3/E3 Line Code Violation Input from LIU – Channel 2:** The exact function of this pin depends upon whether the STS-1 Telecom Bus Interface for Channel 2 has been enabled or not. **If STS-1 Telecom Bus (Channel 2) has been enabled** – STS-1 Transmit Telecom Bus – Alarm Indicator Input: This input pin pulses "high" coincident to any STS-1 signal (which is carrying the AIS-P indicator) being applied to the STS1TXA_D_2[7:0] input data bus. ***Note:*** *If the STS1TXA_ALARM_2 input signal pulses "HIGH" for any given STS-1 signal (within the "incoming" STS-1), then the XRT94L33 will automatically declare the AIS-P defect condition for that particular STS-1 channel.* **If STS-1 Telecom Bus (Channel 2) has NOT been enabled:** If the STS-1 Telecom Bus (Channel 2) has NOT been enabled, then the role that this particular input pin plays depends upon whether Channel 2 is operating in the STS-1 Mode, the DS3/E3 Single-Rail Mode or in the DS3/E3 Dual-Rail Mode, as described below. **If Channel 2 is operating in the STS-1 Mode** If Channel 2 is operating in the STS-1 Mode, then the user should tie this pin to GND. **If Channel 2 is operating in the DS3/E3 Single-Rail Mode – Receive LCV Input from LIU** If Channel 2 is operating in both the DS3/E3 and Single-Rail Modes, then this input pin will function as the LCV (Line Code Violation) input. In this mode, the user is expected to connect the "LCV" output pin from the LIU IC to this input pin. The DS3/E3 Framer block will sample this input pin upon the "user-configured" edge of the "RXDS3LINECLK_2" clock signal, and the Primary Frame Synchronizer block (corresponding with Channel 1) will increment the PMON LCV or EXZ Event Count registers based upon the data sampled at this input pin. **If Channel 2 is operating in the DS3/E3 Dual-Rail Mode – Receive DS3/E3 Negative-Polarity Data Input from LIU** If the user has configured Channel 2 to operate in both the DS3/E3 and the Dual-Rail Mode, then only the "negative-polarity" portion of the Receive DS3/E3 data should be applied to this input pin.

B13	STS1TXA_D0_0 TXHDLCDAT_0_0 TXGFCMSB_0	I/O	TTL/CMOS	**Transmit STS-1 Telecom Bus – Channel 0 – Input Data Bus pin number 0** The exact function of this pin depends upon whether the STS-1 Telecom Bus Interface, associated with Channel 0 is enabled or not. **If STS-1 Telecom Bus (Channel 0) has been enabled** – STS-1 Transmit Telecom Bus – Input Data Bus pin number 0: This input pin along with "STS1TXA_D_0[7:1]" function as the "STS-1 Transmit (Add) Telecom Bus – Input Data Bus for Channel 0. This particular input pin functions as the LSB (Least Significant Bit) input pin on the Transmit (Add) Telecom Bus – Input Data Bus. The STS-1 Telecom Bus interface will sample and latch this pin upon the falling edge of "STS1TXA_CK_0". The LSB of any byte, which is being input into the "STS-1 Transmit Telecom Bus – Data Bus (for Channel 0) should be input via this pin. **TXHDLCDAT_0_0 (Transmit HDLC block data – Channel 0 – Input data pin 0)** If Channel 0 has been configured to operate in the "High-Speed HDLC Controller" Mode, then the System-Side Terminal Equipment will be provided with a "byte-wide" Transmit HDLC Controller byte-wide **TXGFCMSB_0 (Transmit GFC MSB Indicator – Channel 0) – ATM Applications ONLY.** This pin only functions in this particular role if the XRT94L33 has been configured to operate in the ATM UNI Mode.
C13	STS1TXA_D1_0 TXHDLCDAT_1_0 TXGFC_0	I	TTL	**Transmit STS-1 Telecom Bus – Channel 0 – Input Data Bus pin number 1:** The exact function of this pin depends upon whether the STS-1 Telecom Bus Interface, associated with Channel 0 is enabled or not. **If STS-1 Telecom Bus (Channel 0) has been enabled** – STS-1 Transmit Telecom Bus – Input Data Bus pin number 1: This input pin along with "STS1TXA_D_0[7:2]" and "STS1TXA_D0_0 function as the "STS-1 Transmit (Add) Telecom Bus – Input Data Bus for Channel 0. The STS-1 Telecom Bus interface will sample and latch this pin upon the falling edge of "STS1TXA_CK_0". **TXHDLCDAT_1_0 (Transmit HDLC block data – Channel 0 – Input data pin 1)** **TXGFC_0 (Transmit GFC data – Channel 0)**

D13	STS1TXA_D2_0 TXHDLCDAT_2_0 TXCELLTXED_0	I	TTL/CMOS	**Transmit STS-1 Telecom Bus – Channel 0 – Input Data Bus pin number 2:** The exact function of this pin depends upon whether the STS-1 Telecom Bus Interface, associated with Channel 0 is enabled or not. **If STS-1 Telecom Bus (Channel 0) has been enabled** – STS-1 Transmit Telecom Bus – Input Data Bus pin number 2: STS1TXA_D2_0 This input pin along with "STS1TXA_D_0[7:3]" and "STS1TXA_D_0[1:0] function as the "STS-1 Transmit (Add) Telecom Bus – Input Data Bus for Channel 0. The STS-1 Telecom Bus interface will sample and latch this pin upon the falling edge of "STS1TXA_CK_0". **TXHDLCDAT_2_0 (Transmit HDLC block data – Channel 0 – Input data pin 2)** **TXCELLTXED_0 (Cell Transmitted – Channel 0)**
E13	STS1TXA_D3_0 TXHDLCDAT_3_0 SSI_CLK	I/O	TTL/CMOS	**Transmit STS-1 Telecom Bus – Channel 0 – Input Data Bus pin number 3:** The exact function of this pin depends upon whether the STS-1 Telecom Bus Interface, associated with Channel 0 is enabled or not. **If STS-1 Telecom Bus (Channel 0) has been enabled** – STS-1 Transmit Telecom Bus – Input Data Bus pin number 2: STS1TXA_D3_0: This input pin along with "STS1TXA_D_0[7:4]" and "STS1TXA_D_0[2:0] function as the "STS-1 Transmit (Add) Telecom Bus – Input Data Bus for Channel 0. The STS-1 Telecom Bus interface will sample and latch this pin upon the falling edge of "STS1TXA_CK_0". **TXHDLCDAT_3_0 (Transmit HDLC block data – Channel 0 – Input data pin 3** **SSI_CLK (Slow Speed Interface for Ingress Path Clock)**
A12	STS1TXA_D4_0 TXHDLCDAT_4_0 TXDS3OHIND_0	IO	TTL/CMOS	**Transmit STS-1 Telecom Bus – Channel 0 – Input Data Bus pin number 4:** The exact function of this pin depends upon whether the STS-1 Telecom Bus Interface, associated with Channel 0 is enabled or not. **If STS-1 Telecom Bus (Channel 0) has been enabled** – STS-1 Transmit Telecom Bus – Input Data Bus pin number 4: STS1TXA_D4_0: This input pin along with "STS1TXA_D_0[7:5]" and "STS1TXA_D_0[3:0] function as the "STS-1 Transmit (Add) Telecom Bus – Input Data Bus for Channel 0. The STS-1 Telecom Bus interface will sample and latch this pin upon the falling edge of "STS1TXA_CK_0". **TXHDLCDAT_4_0 (Transmit HDLC block data – Channel 0 – Input data pin 4)** **TXDS3OHIND_0 (Transmit DS3 Overhead Indicator – Channel 0)**

A11	STS1TXA_D5_0 TXHDLCDAT_5_0 TXDS3FP_0	I/O	TTL/CMOS	**Transmit STS-1 Telecom Bus – Channel 0 – Input Data Bus pin number 5:** The exact function of this pin depends upon whether the STS-1 Telecom Bus Interface, associated with Channel 0 is enabled or not. **If STS-1 Telecom Bus (Channel 0) has been enabled** – STS-1 Transmit Telecom Bus – Input Data Bus pin number 5: STS1TXA_D5_0: This input pin along with "STS1TXA_D_0[7:6]" and "STS1TXA_D_0[4:0] function as the "STS-1 Transmit (Add) Telecom Bus – Input Data Bus for Channel 0. The STS-1 Telecom Bus interface will sample and latch this pin upon the falling edge of "STS1TXA_CK_0". **TXHDLCDAT_5_0** (Transmit HDLC block data – Channel 0 – Input data pin 5) TXDS3FP_0 (Transmit DS3 Frame Pulse – Channel 0) TXSBDATA_5_0
B12	STS1TXA_D6_0 TXHDLCDAT_6_0 TXDS3DATA_0 TXSBDATA_6_0	I	TTL	Transmit STS-1 Telecom Bus – Channel 0 – Input Data Bus pin number 6: The exact function of this pin depends upon whether the STS-1 Telecom Bus Interface, associated with Channel 0 is enabled or not. If STS-1 Telecom Bus (Channel 0) has been enabled – STS-1 Transmit Telecom Bus – Input Data Bus pin number 6: STS1TXA_D6_0: This input pin along with "STS1TXA_D7_0" and "STS1TXA_D_0[5:0]" function as the "STS-1 Transmit (Add) Telecom Bus – Input Data Bus for Channel 0. The STS-1 Telecom Bus interface will sample and latch this pin upon the falling edge of "STS1TXA_CK_0". If STS-1 Telecom Bus (Channel 0) is disabled – TXHDLCDAT_6_0 (Transmit HDLC block data – Channel 0 – Input data pin 6) TXDS3DATA_0 (Transmit DS3 Data – Channel 0) TXSBDATA_6_0

A10	STS1TXA_D7_0 TXHDLCDAT_7_0 TXAISEN_0 TXSBDATA_7_0	I	TTL	Transmit STS-1 Telecom Bus – Channel 0 – Input Data Bus pin number 7: The exact function of this pin depends upon whether the STS-1 Telecom Bus Interface, associated with Channel 0 is enabled or not. If STS-1 Telecom Bus (Channel 0) has been enabled – STS-1 Transmit Telecom Bus – Input Data Bus pin number 7: STS1TXA_D7_0: This input pin along with "STS1TXA_D_0[6:0]" function as the "STS-1 Transmit (Add) Telecom Bus – Input Data Bus for Channel 0. The STS-1 Telecom Bus interface will sample and latch this pin upon the falling edge of "STS1TXA_CK_0". ***Note:*** *This input pin functions as the MSB (Most Significant Bit) of the Transmit (Add) Telecom Bus, for Channel 0.* If STS-1 Telecom Bus (Channel 0) is disabled – TXHDLCDAT_7_0 **(Transmit HDLC block data – Channel 0 – Input data pin 7)** **TXAISEN_0 (Transmit AIS Enable – Channel 0)**
B23	STS1TXA_D0_1 TXHDLCDAT_0_1 TXGFCMSB_1	I/O	TTL/CMOS	**Transmit STS-1 Telecom Bus – Channel 1 – Input Data Bus pin number 0:** The exact function of this pin depends upon whether the STS-1 Telecom Bus Interface, associated with Channel 1 is enabled or not. **If STS-1 Telecom Bus (Channel 1) has been enabled** – STS-1 Transmit Telecom Bus – Input Data Bus pin number 0: This input pin along with "STS1TXA_D_1[7:1]" function as the "STS-1 Transmit (Add) Telecom Bus – Input Data Bus for Channel 1. This particular input pin functions as the LSB (Least Significant Bit) input pin on the Transmit (Add) Telecom Bus – Input Data Bus. The STS-1 Telecom Bus interface will sample and latch this pin upon the falling edge of "STS1TXA_CK_1". The LSB of any byte, which is being input into the "STS-1 Transmit Telecom Bus – Data Bus (for Channel 1) should be input via this pin. **TXHDLCDAT_0_1 (Transmit HDLC block data – Channel 1 – Input data pin 0)** **TXGFCMSB_1 (Transmit GFC MSB Indicator – Channel 1)**

C20	STS1TXA_D1_1 TXHDLCDAT_1_1 TXGFC_1	I	TTL	**Transmit STS-1 Telecom Bus – Channel 1 – Input Data Bus pin number 1:** The exact function of this pin depends upon whether the STS-1 Telecom Bus Interface, associated with Channel 1 is enabled or not. **If STS-1 Telecom Bus (Channel 1) has been enabled** – STS-1 Transmit Telecom Bus – Input Data Bus pin number 1: This input pin along with "STS1TXA_D_1[7:2]" and "STS1TXA_D0_1 function as the "STS-1 Transmit (Add) Telecom Bus – Input Data Bus for Channel 1. The STS-1 Telecom Bus interface will sample and latch this pin upon the falling edge of "STS1TXA_CK_1". **TXHDLCDAT_1_1 (Transmit HDLC block data – Channel 1 – Input data pin 1)** **TXGFC_1 (Transmit GFC data – Channel 1)**
B22	STS1TXA_D2_1 TXHDLCDAT_2_1 TXCELLTXED_1	I/O	TTL/CMOS	**Transmit STS-1 Telecom Bus – Channel 1 – Input Data Bus pin number 2:** The exact function of this pin depends upon whether the STS-1 Telecom Bus Interface, associated with Channel 1 is enabled or not. **If STS-1 Telecom Bus (Channel 1) has been enabled** – STS-1 Transmit Telecom Bus – Input Data Bus pin number 2: STS1TXA_D2_1 This input pin along with "STS1TXA_D_1[7:3]" and "STS1TXA_D_1[1:0] function as the "STS-1 Transmit (Add) Telecom Bus – Input Data Bus for Channel 1. The STS-1 Telecom Bus interface will sample and latch this pin upon the falling edge of "STS1TXA_CK_1". **TXHDLCDAT_2_1 (Transmit HDLC block data – Channel 1 – Input data pin 2)** **TXCELLTXED_1 (Cell Transmitted – Channel 1)**
E18	STS1TXA_D3_1 TXHDLCDAT_3_1 SSI_POS	I/O	TTL/CMOS	**Transmit STS-1 Telecom Bus – Channel 1 – Input Data Bus pin number 3:** The exact function of this pin depends upon whether the STS-1 Telecom Bus Interface, associated with Channel 1 is enabled or not. **If STS-1 Telecom Bus (Channel 1) has been enabled** – STS-1 Transmit Telecom Bus – Input Data Bus pin number 3: STS1TXA_D3_1: This input pin along with "STS1TXA_D_1[7:4]" and "STS1TXA_D_1[2:0] function as the "STS-1 Transmit (Add) Telecom Bus – Input Data Bus for Channel 1. The STS-1 Telecom Bus interface will sample and latch this pin upon the falling edge of "STS1TXA_CK_1". **TXHDLCDAT_3_1 (Transmit HDLC block data – Channel 1 – Input data pin 3)** **SSI_POS (Slow Speed Interface Data Positive for Ingress Path)**

A23	STS1TXA_D4_1 TXHDLCDAT_4_1 TXDS3OHIND_1	I/O	TTL/CMOS	**Transmit STS-1 Telecom Bus – Channel 1 – Input Data Bus pin number 4:** The exact function of this pin depends upon whether the STS-1 Telecom Bus Interface, associated with Channel 1 is enabled or not. **If STS-1 Telecom Bus (Channel 1) has been enabled** – STS-1 Transmit Telecom Bus – Input Data Bus pin number 4: STS1TXA_D4_1: This input pin along with "STS1TXA_D_1[7:5]" and "STS1TXA_D_1[3:0] function as the "STS-1 Transmit (Add) Telecom Bus – Input Data Bus for Channel 1. The STS-1 Telecom Bus interface will sample and latch this pin upon the falling edge of "STS1TXA_CK_1". **If STS-1 Telecom Bus (Channel 1) has NOT been enabled:** If STS-1 Telecom Bus (Channel 1) has not been enabled, then this particular pin can be configured to function in either of the following roles **TXHDLCDAT_4_1 (Transmit HDLC block data – Channel 1 – Input data pin 4)** This input pin will function as a part of the "Transmit HDLC Controller" byte-wide data input bus, whenever the user configures the DS3/E3 Framer block (associated with Channel 1) to operate in the "High-Speed HDLC Controller" Mode. This pin will function as Data Input Pin # 4. **TXDS3OHIND_1 (Transmit DS3 Overhead Indicator – Channel 1)** This output pin will pulse "high" one bit-period prior to the time that the DS3/E3 Frame Generator block (within Channel 1) will be processing an Overhead bit. The purpose of this outpout pin is to warn the Terminal Equipment that, during the very next bit-period, the DS3/E3 Frame Generator block is going to be processing an Overhead Bit and will be ignoring any data that is applied to to the TxSer input pin. *NOTE: The user can ignore this output pin provide that that either the Primary or Secondary Frame Synchronizer block is always "up-stream" from the DS3/E3 Frame Generator block.*

C19	STS1TXA_D5_1 TXHDLCDAT_5_1 TXDS3FP_1	I/O	TTL/CMOS	**Transmit STS-1 Telecom Bus – Channel 1 – Input Data Bus pin number 5:** The exact function of this pin depends upon whether the STS-1 Telecom Bus Interface, associated with Channel 1 is enabled or not. **If STS-1 Telecom Bus (Channel 1) has been enabled** – STS-1 Transmit Telecom Bus – Input Data Bus pin number 5: STS1TXA_D5_1: This input pin along with "STS1TXA_D_1[7:6]" and "STS1TXA_D_1[4:0] function as the "STS-1 Transmit (Add) Telecom Bus – Input Data Bus for Channel 1. The STS-1 Telecom Bus interface will sample and latch this pin upon the falling edge of "STS1TXA_CK_1". **TXHDLCDAT_5_1 (Transmit HDLC block data – Channel 1 – Input data pin 5)** **TXDS3FP_1 (Transmit DS3 Frame Pulse – Channel 1)**
D18	STS1TXA_D6_1 TXHDLCDAT_6_1 TXDS3DATA_1	I	TTL	**Transmit STS-1 Telecom Bus – Channel 1 – Input Data Bus pin number 6:** The exact function of this pin depends upon whether the STS-1 Telecom Bus Interface, associated with Channel 1 is enabled or not. **If STS-1 Telecom Bus (Channel 1) has been enabled** – STS-1 Transmit Telecom Bus – Input Data Bus pin number 6: STS1TXA_D6_1: This input pin along with "STS1TXA_D7_1" and "STS1TXA_D_1[5:0]" function as the "STS-1 Transmit (Add) Telecom Bus – Input Data Bus for Channel 1. The STS-1 Telecom Bus interface will sample and latch this pin upon the falling edge of "STS1TXA_CK_1". **TXHDLCDAT_6_1 (Transmit HDLC block data – Channel 1 – Input data pin 6)** **TXDS3DATA_1 (Transmit DS3 Data – Channel 1)**
B21	STS1TXA_D7_1 TXHDLCDAT_7_1 TXAISEN_1	I	TTL	**Transmit STS-1 Telecom Bus – Channel 1 – Input Data Bus pin number 7:** The exact function of this pin depends upon whether the STS-1 Telecom Bus Interface, associated with Channel 1 is enabled or not. **If STS-1 Telecom Bus (Channel 1) has been enabled** – STS-1 Transmit Telecom Bus – Input Data Bus pin number 7: STS1TXA_D7_1: This input pin along with "STS1TXA_D_1[6:0]" function as the "STS-1 Transmit (Add) Telecom Bus – Input Data Bus for Channel 1. The STS-1 Telecom Bus interface will sample and latch this pin upon the falling edge of "STS1TXA_CK_1". ***Note:*** *This input pin functions as the MSB (Most Significant Bit) of the Transmit (Add) Telecom Bus, for Channel 1.* **TXHDLCDAT_7_1 (Transmit HDLC block data – Channel 1 – Input data pin 7)** **TXAISEN_1 (Transmit AIS Enable – Channel 1)**

AE15	STS1TXA_D0_2 TXHDLCDAT_0_2 TXGFCMSB_2	I/O	TTL/CMOS	**Transmit STS-1 Telecom Bus – Channel 2 – Input Data Bus pin number 0:** The exact function of this pin depends upon whether the STS-1 Telecom Bus Interface, associated with Channel 2 is enabled or not. **If STS-1 Telecom Bus (Channel 2) has been enabled** – STS-1 Transmit Telecom Bus – Input Data Bus pin number 0: This input pin along with "STS1TXA_D_2[7:1]" function as the "STS-1 Transmit (Add) Telecom Bus – Input Data Bus for Channel 2. This particular input pin functions as the LSB (Least Significant Bit) input pin on the Transmit (Add) Telecom Bus – Input Data Bus. The STS-1 Telecom Bus interface will sample and latch this pin upon the falling edge of "STS1TXA_CK_2". The LSB of any byte, which is being input into the "STS-1 Transmit Telecom Bus – Data Bus (for Channel 2) should be input via this pin. **TXHDLCDAT_0_2 (Transmit HDLC block data – Channel 2 – Input data pin 0)** **TXGFCMSB_2 (Transmit GFC MSB Indicator – Channel 2)**
AD15	STS1TXA_D1_2 TXHDLCDAT_1_2 TXGFC_2	I	TTL	**Transmit STS-1 Telecom Bus – Channel 2 – Input Data Bus pin number 1:** The exact function of this pin depends upon whether the STS-1 Telecom Bus Interface, associated with Channel 1 is enabled or not. **If STS-1 Telecom Bus (Channel 2) has been enabled** – STS-1 Transmit Telecom Bus – Input Data Bus pin number 1: This input pin along with "STS1TXA_D_2[7:2]" and "STS1TXA_D0_2 function as the "STS-1 Transmit (Add) Telecom Bus – Input Data Bus for Channel 2. The STS-1 Telecom Bus interface will sample and latch this pin upon the falling edge of "STS1TXA_CK_2". **TXHDLCDAT_1_2 (Transmit HDLC block data – Channel 2 – Input data pin 1)** **TXGFC_2 (Transmit GFC data – Channel 2)**
AC15	STS1TXA_D2_2 TXHDLCDAT_2_2 TXCELLTXED_2	I/O	TTL/CMOS	**Transmit STS-1 Telecom Bus – Channel 2 – Input Data Bus pin number 2:** The exact function of this pin depends upon whether the STS-1 Telecom Bus Interface, associated with Channel 2 is enabled or not. **If STS-1 Telecom Bus (Channel 2) has been enabled –** STS-1 Transmit Telecom Bus – Input Data Bus pin number 2: STS1TXA_D2_2 This input pin along with "STS1TXA_D_2[7:3]" and "STS1TXA_D_2[1:0] function as the "STS-1 Transmit (Add) Telecom Bus – Input Data Bus for Channel 2. The STS-1 Telecom Bus interface will sample and latch this pin upon the falling edge of "STS1TXA_CK_2". **TXHDLCDAT_2_2 (Transmit HDLC block data – Channel 2 – Input data pin 2)** **TXCELLTXED_2 (Cell Transmitted – Channel 2)**

AG16	STS1TXA_D3_2 TXHDLCDAT_3_2 SSI_NEG	I/O	TTL/CMOS	**Transmit STS-1 Telecom Bus – Channel 2 – Input Data Bus pin number 3:** The exact function of this pin depends upon whether the STS-1 Telecom Bus Interface, associated with Channel 2 is enabled or not. **If STS-1 Telecom Bus (Channel 2) has been enabled** – STS-1 Transmit Telecom Bus – Input Data Bus pin number 3: STS1TXA_D3_2: This input pin along with "STS1TXA_D_2[7:4]" and "STS1TXA_D_2[2:0] function as the "STS-1 Transmit (Add) Telecom Bus – Input Data Bus for Channel 2. The STS-1 Telecom Bus interface will sample and latch this pin upon the falling edge of "STS1TXA_CK_2". **TXHDLCDAT_3_2 (Transmit HDLC block data – Channel 2 – Input data pin 3)** **SSI_NEG (Slow Speed Interface Data Negative for Ingress Path)**
AG17	STS1TXA_D4_2 TXHDLCDAT_4_2 TXDS3OHIND_2	I/O	TTL/CMOS	**Transmit STS-1 Telecom Bus – Channel 2 – Input Data Bus pin number 4:** The exact function of this pin depends upon whether the STS-1 Telecom Bus Interface, associated with Channel 2 is enabled or not. **If STS-1 Telecom Bus (Channel 2) has been enabled** – STS-1 Transmit Telecom Bus – Input Data Bus pin number 4: STS1TXA_D4_2: This input pin along with "STS1TXA_D_2[7:5]" and "STS1TXA_D_2[3:0] function as the "STS-1 Transmit (Add) Telecom Bus – Input Data Bus for Channel 2. The STS-1 Telecom Bus interface will sample and latch this pin upon the falling edge of "STS1TXA_CK_2". **TXHDLCDAT_4_2 (Transmit HDLC block data – Channel 2 – Input data pin 4)** **TXDS3OHIND_2 (Transmit DS3 Overhead Indicator – Channel 2)**
AF16	STS1TXA_D5_2 TXHDLCDAT_5_2 TXDS3FP_2	I/O	TTL/CMOS	**Transmit STS-1 Telecom Bus – Channel 2 – Input Data Bus pin number 5:** The exact function of this pin depends upon whether the STS-1 Telecom Bus Interface, associated with Channel 2 is enabled or not. **If STS-1 Telecom Bus (Channel 2) has been enabled** – STS-1 Transmit Telecom Bus – Input Data Bus pin number 5: STS1TXA_D5_2: This input pin along with "STS1TXA_D_2[7:6]" and "STS1TXA_D_2[4:0] function as the "STS-1 Transmit (Add) Telecom Bus – Input Data Bus for Channel 2. The STS-1 Telecom Bus interface will sample and latch this pin upon the falling edge of "STS1TXA_CK_2". **TXHDLCDAT_5_2 (Transmit HDLC block data – Channel 2 – Input data pin 5)** **TXDS3FP_2 (Transmit DS3 Frame Pulse – Channel 2)**

AG18	STS1TXA_D6_2 TXHDLCDAT_6_2 TXDS3DATA_2	I	TTL	**Transmit STS-1 Telecom Bus – Channel 2 – Input Data Bus pin number 6:** The exact function of this pin depends upon whether the STS-1 Telecom Bus Interface, associated with Channel 2 is enabled or not. **If STS-1 Telecom Bus (Channel 2) has been enabled** – STS-1 Transmit Telecom Bus – Input Data Bus pin number 6: STS1TXA_D6_2: This input pin along with "STS1TXA_D7_2" and "STS1TXA_D_2[5:0]" function as the "STS-1 Transmit (Add) Telecom Bus – Input Data Bus for Channel 2. The STS-1 Telecom Bus interface will sample and latch this pin upon the falling edge of "STS1TXA_CK_2". **TXHDLCDAT_6_2 (Transmit HDLC block data – Channel 2 – Input data pin 6)** **TXDS3DATA_2 (Transmit DS3 Data – Channel 2)**

AE16	STS1TXA_D7_2 TXHDLCDAT_7_2 TXAISEN_2	I	TTL	**Transmit STS-1 Telecom Bus – Channel 2 – Input Data Bus pin number 7:** The exact function of this pin depends upon whether the STS-1 Telecom Bus Interface, associated with Channel 2 is enabled or not. **If STS-1 Telecom Bus (Channel 2) has been enabled** – STS-1 Transmit Telecom Bus – Input Data Bus pin number 7: STS1TXA_D7_2: This input pin along with "STS1TXA_D_2[6:0]" function as the "STS-1 Transmit (Add) Telecom Bus – Input Data Bus for Channel 2. The STS-1 Telecom Bus interface will sample and latch this pin upon the falling edge of "STS1TXA_CK_2". ***Note:*** *This input pin functions as the MSB (Most Significant Bit) of the Transmit (Add) Telecom Bus, for Channel 2.* **If STS-1 Telecom Bus (Channel 2) has NOT been enabled:** If STS-1 Telecom Bus (Channel 2) has not been enabled, then this particular pin can be configured to function in either of the following roles. **TXHDLCDAT_7_2 (Transmit HDLC block data – Channel 2 – Input data pin 7 – High Speed HDLC Controller Mode Only)** This input pin will function as a part of the "Transmit HDLC Controller" byte-wide data input bus, whenever the user configures the DS3/E3 Framer block (associated with Channel 2) to operate in the "High-Speed HDLC Controller" Mode. This pin will function as Data Input Pin # 2. **TXAISEN_2 (Transmit AIS Enable – Channel 2)** This input pin permits the user to command the DS3/E3 Frame Generator block (associated with Channel 2) to transmit the DS3/E3 AIS indicator. Pulling this input pin "high" configures the DS3/E3 Frame Generator block to generate and transmit the DS3/E3 AIS indicator. Pulling this input pin "low" configures the DS3/E3 Frame Generator block to transmit normal DS3/E3 data-streams. *NOTE: The user should pull this pin to "GND" for normal operation*
RECEIVE SYSTEM SIDE INTERFACE PINS				

B15 C23 AG13	RxOH_0 RxOH_1 RxOH_2	O	CMOS	**Receive Overhead Data Output Interface – output** This output pin functions as the "Receive Overhead Data" output for the receive system side interface when the XRT94L33 is configured to operate in DS3/E3 mode, however, it functions as the "Receive STS-1 Overhead Data" output when the device is configured to operate in the STS-1 mode. **When configured to operate in DS3/E3 mode:** All overhead bits, which are received via the "Receive Section" of the channel, will be output via this output pin, upon the rising edge of "RxOHClk_n". **When configured to operate in STS-1 mode:** These output pins, along with "RxOHEnable_n", "RxOHClk_n" and "RxOHFrame_n" function as the "Receive STS-1 TOH and POH Output Port". Each bit, within the TOH and POH bytes (within the incoming STS-1 data stream) is updated upon the falling edge of "RxOHClk_n". As a consequence, external circuitry receiving this data, should sample this data upon the rising edge of "RxOHClk_n". ***Notes:*** 1. The external circuitry can determine whether or not it is receiving POH or TOH data via this output pin. The "RxOHEnable_n" output pin will be "high" anytime POH data is being output via these output pins. Conversely, the "RxOHEnable_n" output pin will be "low" anytime TOH data is being output via these output pins. 2. TOH and POH data, associated with Receive STS-1 TOH and POH Processor Block – Channel 0 will be output via the "RxOH_0, and so on.

C15 D21 AF13	RxOHENABLE_0 RxOHENABLE_1 RxOHENABLE_2	O	CMOS	**Receive Overhead Data Output Interface – Enable Output** This output pin functions as the "Receive Overhead Enable" output for the receive system side interface when the XRT94L33 is configured to operate in DS3/E3 mode, however, it functions as the "Receive STS-1 Overhead Data" output when the device is configured to operate in the STS-1 mode. **When configured to operate in DS3/E3 mode:** The channel will assert this output signal for one "RxOHClk_n" period when it is safe for the local terminal equipment to sample the data on the "RxOH_n" output pin. **When configured to operate in STS-1 mode:** These output pins, along with "RxOHClk_n", "RxOHFrame_n" and "RxOH_n" function as the "Receive STS-1 TOH and POH Output Port". These output pins indicate whether POH or TOH data is being output via the "RxOH_n" output pins. These output pins will toggle "high" coincident with when POH data is being output via the "RxOH_n" output pins. Conversely, these output pins will toggle "low" coincident with when TOH data is being output via the "RxOH_n" output pins. These output pins are updated upon the falling edge of "RxOHClk_n". As a consequence, external circuitry, receiving this data, should sample this data upon the rising edge of "RxOHClk_n".
D15 E20 AE13	RxOHCLK_0 RxOHCLK_1 RxOHCLK_2	O	CMOS	**Receive Overhead Data Output Interface – clock** This output pin functions as the "Receive Overhead Clock" output for the receive system side interface when the XRT94L33 is configured to operate in DS3/E3 mode, however, it functions as the "Receive STS-1 Overhead Clock" output when the device is configured to operate in the STS-1 mode. **When configured to operate in DS3/E3 mode:** The channel will output the overhead bits (within the incoming DS3 or E3 frames) via the RxOH_n output pin, upon the falling edge of this clock signal. As a consequence, the user's local terminal equipment should use the rising edge of this clock signal to sample the data on both the "RxOH" and "RxOHFrame" output pins. ***Note:*** *This clock signal is always active.* **When configured to operate in STS-1 mode:** These output pins, along with "RxOH_n", "RxOHFrame_n", and "RxOHEnable_n" function as the "Receive STS-1 TOH and POH Output Port". These output pins function as the "Clock Output" signals for the Receive STS-1 TOH and POH Output Port. The "RxOH_n", "RxSTS1Frame_n" and "RxOHEnable_n" output pins are updated upon the falling edge of this clock signal.

E15 D22 AD13	RxOHFRAME_0 RxOHFRAME_1 RxOHFRAME_2	O	CMOS	**Receive Overhead Data Interface – Framing Pulse indicator** This output pin functions as the "Receive Overhead Clock" output for the receive system side interface when the XRT94L33 is configured to operate in DS3/E3 mode, however, it functions as the "Receive STS-1 Overhead Clock" output when the device is configured to operate in the STS-1 mode. **When configured to operate in DS3/E3 mode:** This output pin pulses "high" whenever the Receive Overhead Data Output Interface block outputs the first overhead bit of a new DS3 or E3 frame. **When configured to operate in STS-1 mode:** These output pins, along with "RxOH_n", "RxOHEnable_n" and "RxOHClk_n" function as the "Receive STS-1 TOH and POH Output Port". These output pins will pulse "high" coincident with either of the following events. When the very first TOH byte (A1), of a given STS-1 frame, is being output via the corresponding "RxOH_n" output pin. When the very first POH byte (J1), of a given STS-1 frame, is being output via the corresponding "RxOH_n" output pin. The external circuitry can determine whether these output pins are pulsing high for the first TOH or POH byte by checking the state of the corresponding "RxOHEnable_n" output pin.
Y26	RxPERR	O	CMOS	**For mapper applications, Please let this pin "float".**
AB27	RxPEOP	O	CMOS	**For mapper applications, Please let this pin "float".**
AA26	RxPDVAL	O	CMOS	**For mapper applications, Please let this pin "float".**
V24	RxMOD_0	O	CMOS	**For mapper applications, Please let this pin "float".**
V25	RxUPRTY/ RxPPRTY	O	CMOS	**For mapper applications, Please let this pin "float".**

U23 W26 U24 AA27 Y27 U25 V26 W27 T23 T24 U26 T25 V27 T26 U27 T27	RxUDATA_0/ RxPDATA_0 RxUDATA_1/ RxPDATA_1 RxUDATA_2/ RxPDATA_2 RxUDATA_3/ RxPDATA_3 RxUDATA_4/ RxPDATA_4 RxUDATA_5/ RxPDATA_5 RxUDATA_6/ RxPDATA_6 RxUDATA_7/ RxPDATA_7 RxUDATA_8/ RxPDATA_8 RxUDATA_9/ RxPDATA_9 RxUDATA_10/ RxPDATA_10 RxUDATA_11/ RxPDATA_11 RxUDATA_12/ RxPDATA_12 RxUDATA_13/ RxPDATA_13 RxUDATA_14/ RxPDATA_14 RxUDATA_15/ RxPDATA_15	O	CMOS	**For mapper applications, Please let these pins "float".**
R23 R24 R25 R26 R27	RxUADDR_0 RxUADDR_1 RxUADDR_2 RxUADDR_3 RxUADDR_4	I	TTL	**For mapper applications, Please connect these pins to GND**
P27	RxUClav/ RxPPA	O	CMOS	**For mapper applications, Please let this pin "float".**
P25	RxUSOC/ RxPSOP/ RxPSOC	O	CMOS	**For mapper applications, Please let this pin "float".**
P23	RxTSX/ RXPSOF	O	CMOS	**For mapper applications, Please let this pin "float".**
P24	RXUENB_L/ RXPENB_L	I	TTL	**For mapper applications, Please connect this pin to VDD**
P26	RXUCLKO/ RXPCLKO	O	CMOS	**For mapper applications, Please let this pin "float".**
N27	RXUCLK/ RXPCLK	I	TTL	**For mapper applications, Please connect this pin to GND**

A16 J23 AC13	EXTLOS_0 EXTLOS_1 EXTLOS_2	I	TTL	**Receive LOS (Loss of Signal) Indicator Input (from the XRT94L33 DS3/E3/STS-1 LIU IC):** This input pin, is intended to be connected to each of the RLOS (Receive Loss of Signal) output pins of the XRT94L33 DS3/E3/STS-1 LIU IC. The user can monitor the state of this input pin by reading the state of Bit 0 (RLOS) within the Line Interface Scan Register (Address = 0xXX, 0xXX). If this input pin is "Low", then it means that the corresponding channel (within the XRT94L33) is currently NOT declaring an LOS condition. However, if this input pin is "high", then it means that this particular channel is currently declaring an LOS condition. ***Note:*** *Asserting this input pin will cause the XRT94L33 Framer/UNI IC to declare an "LOS (Loss of Signal) condition. Therefore, this input pin should not be used as a General Purpose Input pin.*
A14 D20 AE14	RxOOF_0 RxOOF_1 RxOOF_2	O	CMOS	**Receive STS-1/DS3/E3 Out of Frame Indicator** The STS-1/DS3/E3 Receive DS3 Framer will assert this output signal whenever it has declared an "Out of Frame" (OOF) condition with the incoming DS3 frames. This signal is negated when the framer correctly locates the F- and M-bits and regains synchronization with the DS3 frame.
A15 B24 AG14	RxLOS_0 RxLOS_1 RxLOS_2	O	CMOS	**STS-1/DS3/E3 Framer - Loss of Signal Output Indicator:** This pin is asserted when the Receive Section of the channel encounters 180 consecutive 0's (for DS3 applications) or 32 consecutive 0's (for E3 applications) via the RxPOS_n and RxNEG pins. For STS-1 applications, users can set the LOS threshold value in the Receive LOS Threshold register. (RxSTOH_LOS_TH, Address Location: 0xN02E – 0xN02F) This pin will be negated once the Receive DS3/E3 Framer has detected at least 60 "1s" out of 180 consecutive bits (for DS3 applications) or has detected at least four consecutive 32 bit strings of data that contain at least 8 "1s" in the receive path.

STS-1 TELECOM BUS INTERFACE – RECEIVE DIRECTION				
A21	STS1RXD_CK_0 RXVALIDFCS_0 RXGFCCLK_0	O	CMOS	**Receive STS-1/STS-3 Telecom Bus Clock Output – Channel 0;** The exact function of this input pin depends upon whether the "STS-1 Telecom Bus Interface associated with Channel 0" is enabled or not, as described below. **If STS-1 Telecom Bus (Channel 0) has been enabled** – STS-1 Receive Telecom Bus Clock Output – Channel 0; STS1RXD_CK_0: All signals, which are output via the "Receive Telecom Bus – Channel 0" are clocked out upon the rising edge of this clock signal. This includes the following signals. • STS1RXD_D_0[7:0] • STS1RXD_ALARM_0 • STS1RXD_DP_0 • STS1RXD_PL_0 • STS1RXD_C1J1_0 This clock signal will operate at 19.44MHz (For STS-3 mode) or 6.48MHz (Fro STS-1 mode) **RXVALIDFCS_0 (Receive HDLC block valid FCS Indicator – Channel 0)** **RXGFCCLK_0 (Receive ATM GFC clock signal – Channel 0)**

H24	STS1RXD_CK_1 RXVALIDFCS_1 RXGFCCLK_1 TxP_STPA	O	CMOS	**Receive STS-1 Telecom Bus Clock Output – Channel 1;** The exact function of this input pin depends upon whether the "STS-1 Telecom Bus Interface associated with Channel 1" is enabled or not, as described below. **If STS-1 Telecom Bus (Channel 1) has been enabled** – STS-1 Receive Telecom Bus Clock Output – Channel 1; STS1RXD_CK_1: All signals, which are output via the "Receive Telecom Bus – Channel 1" are clocked out upon the rising edge of this clock signal. This includes the following signals. • STS1RXD_D_1[7:0] • STS1RXD_ALARM_1 • STS1RXD_DP_1 • STS1RXD_PL_1 • STS1RXD_C1J1_1 This clock signal will operate at 19.44MHz. (For STS-3 mode) or 6.48MHz (Fro STS-1 mode) **RXVALIDFCS_1 (Receive HDLC block valid FCS Indicator – Channel 1)** **RXGFCCLK_1 (Receive ATM GFC clock signal – Channel 1)** **TxP_STPA (Transmit PPP Level 2 Selected Channel Packet Available)**
AG8	STS1RXD_CK_2 RXVALIDFCS_2 RXGFCCLK_2	O	CMOS	**Receive STS-1 Telecom Bus Clock Output – Channel 2;** The exact function of this input pin depends upon whether the "STS-1 Telecom Bus Interface associated with Channel 2" is enabled or not, as described below. **If STS-1 Telecom Bus (Channel 2) has been enabled** – STS-1 Receive Telecom Bus Clock Output – Channel 2; STS1RXD_CK_2: All signals, which are output via the "Receive Telecom Bus – Channel 2" are clocked out upon the rising edge of this clock signal. This includes the following signals. • STS1RXD_D_2[7:0] • STS1RXD_ALARM_2 • STS1RXD_DP_2 • STS1RXD_PL_2 • STS1RXD_C1J1_2 This clock signal will operate at 19.44MHz. (For STS-3 mode) or 6.48MHz (Fro STS-1 mode) **RXVALIDFCS_2 (Receive HDLC block valid FCS Indicator – Channel 2)** **RXGFCCLK_2 (Receive ATM GFC clock signal – Channel 2)**

A20	STS1RXD_PL_0 RXIDLE_0 RXLCD_0	O	CMOS	**STS-1 Receive (Drop) Telecom Bus – Payload Indicator Output Signal – Channel 0:** The exact function of this output pin depends upon whether the user has enabled or disabled the "STS-1 Telecom Bus Interface block" associated with Channel 0. **If the STS-1 Telecom Bus Interface (associated with Channel 0) is enabled** – STS-1/STS-1 Receive (Drop) Telecom Bus – Payload Indicator Output – STS1RXD_PL_0: This output pin indicates whether or not Transport Overhead bytes are being output via the "STS1RXD_D_0[7:0]" output pins. This output pin is pulled "low" for the duration that the STS-1 Receive Telecom Bus is transmitting a Transport Overhead byte via the "STS1RXD_D_0[7:0]" output pins. Conversely, this output pin is pulled "high" for the duration that the STS-1 Receive Telecom Bus is transmitting something other than a Transport Overhead byte via the "STS1RXD_D_0[7:0]" output pins. **RXIDLE_0 (Receive HDLC block idle indicator – Channel 0)** **RXLCD_0 (Receive Cell Processor Loss of Cell Delineation – Channel 0)**
D26	STS1RXD_PL_1 RXIDLE_1 RXLCD_1	O	CMOS	**STS-1 Receive (Drop) Telecom Bus – Payload Indicator Output Signal – Channel 1:** The exact function of this output pin depends upon whether the user has enabled or disabled the "STS-1 Telecom Bus Interface block" associated with Channel 1. **If the STS-1 Telecom Bus Interface (associated with Channel 1) is enabled –** STS-1/STS-1 Receive (Drop) Telecom Bus – Payload Indicator Output – STS1RXD_PL_1: This output pin indicates whether or not Transport Overhead bytes are being output via the "STS1RXD_D_1[7:0]" output pins. This output pin is pulled "low" for the duration that the STS-1 Receive Telecom Bus is transmitting a Transport Overhead byte via the "STS1RXD_D_1[7:0]" output pins. Conversely, this output pin is pulled "high" for the duration that the STS-1 Receive Telecom Bus is transmitting something other than a Transport Overhead byte via the "STS1RXD_D_1[7:0]" output pins. **RXIDLE_1 (Receive HDLC block idle indicator – Channel 1)** **RXLCD_1 (Receive Cell Processor Loss of Cell Delineation – Channel 1)**

AE11	STS1RXD_PL_2 RXIDLE_2 RXLCD_2	O	CMOS	**STS-1 Receive (Drop) Telecom Bus – Payload Indicator Output Signal – Channel 2:** The exact function of this output pin depends upon whether the user has enabled or disabled the "STS-1 Telecom Bus Interface block" associated with Channel 2. **If the STS-1 Telecom Bus Interface (associated with Channel 2) is enabled** – STS-1/STS-1 Receive (Drop) Telecom Bus – Payload Indicator Output – STS1RXD_PL_2: This output pin indicates whether or not Transport Overhead bytes are being output via the "STS1RXD_D_2[7:0]" output pins. This output pin is pulled "low" for the duration that the STS-1 Receive Telecom Bus is transmitting a Transport Overhead byte via the "STS1RXD_D_2[7:0]" output pins. Conversely, this output pin is pulled "high" for the duration that the STS-1 Receive Telecom Bus is transmitting something other than a Transport Overhead byte via the "STS1RXD_D_2[7:0]" output pins. **RXIDLE_2 (Receive HDLC block idle indicator – Channel 2)** **RXLCD_2 (Receive Cell Processor Loss of Cell Delineation – Channel 2)**

C17	STS1RXD_C1J1_0 TXDS3LINECLK_0	O	CMOS	**STS-1 Receive Telecom Bus - C1/J1 Byte Phase Indicator Output Signal – Channel 0:** The exact function of this output pin depends upon whether the STS-1 Telecom Bus Interface for Channel 0 has been enabled or not. **If STS-1 Telecom Bus (Channel 0) has been enabled** – STS-1 Receive Telecom Bus – C1/J1 Byte Phase Indicator Output Signal: This output pin pulses "high" under the following two conditions. Whenever the C1 byte is being output via the "STS1RXD_D_0[7:0]" output, and Whenever the J1 byte is being output via the "STS1RXD_D_0[7:0]" output. ***Notes:*** 1. The STS-1 Receive (Drop) Telecom Bus (associated with Channel 0) will indicate that it is transmitting the C1 byte (via the STS1RXD_D_0[7:0] output pins), by pulsing this output pin "HIGH" (for one period of "STS1RXD_CK_0") and keeping the "STS1RXD_PL_0" output pin pulled "LOW. 2. The STS-1 Receive (Drop) Telecom Bus (associated with Channel 0) will indicate that it is transmitting the J1 byte (via the STS1RXD_D_0[7:0] output pins), by pulsing this output pin "HIGH" (for one period of "STS1RXD_CK_0") while the "STS1TXD_PL_0" output pin is pulled "HIGH". **TXDS3LINECLK_0 (Transmit DS3/E3/STS-1 line clock to LIU – Channel 0)**

E25	STS1RXD_C1J1_1 TXDS3LINECLK_1	O	CMOS	**STS-1 Receive Telecom Bus - C1/J1 Byte Phase Indicator Output Signal – Channel 1:** The exact function of this output pin depends upon whether the STS-1 Telecom Bus Interface for Channel 1 has been enabled or not. **If STS-1 Telecom Bus (Channel 1) has been enabled** – STS-1 Receive Telecom Bus – C1/J1 Byte Phase Indicator Output Signal: This output pin pulses "high" under the following two conditions. Whenever the C1 byte is being output via the "STS1RXD_D_1[7:0]" output, and Whenever the J1 byte is being output via the "STS1RXD_D_1[7:0]" output. ***Notes:*** 1. The STS-1 Receive (Drop) Telecom Bus (associated with Channel 1) will indicate that it is transmitting the C1 byte (via the STS1RXD_D_1[7:0] output pins), by pulsing this output pin "HIGH" (for one period of "STS1RXD_CK_1") and keeping the "STS1RXD_PL_1" output pin pulled "LOW. 2. The STS-1 Receive (Drop) Telecom Bus (associated with Channel 1) will indicate that it is transmitting the J1 byte (via the STS1RXD_D_1[7:0] output pins), by pulsing this output pin "HIGH" (for one period of "STS1RXD_CK_1") while the "STS1TXD_PL_1" output pin is pulled "HIGH". **TXDS3LINECLK_1 (Transmit DS3/E3/STS-1 line clock to LIU – Channel 1)**

AF10	STS1RXD_C1J1_2 TXDS3LINECLK_2	O	CMOS	**STS-1 Receive Telecom Bus - C1/J1 Byte Phase Indicator Output Signal – Channel 2:** The exact function of this output pin depends upon whether the STS-1 Telecom Bus Interface for Channel 2 has been enabled or not. **If STS-1 Telecom Bus (Channel 2) has been enabled** – STS-1 Receive Telecom Bus – C1/J1 Byte Phase Indicator Output Signal: This output pin pulses "high" under the following two conditions. Whenever the C1 byte is being output via the "STS1RXD_D_2[7:0]" output, and Whenever the J1 byte is being output via the "STS1RXD_D_2[7:0]" output. ***Notes:*** 1. The STS-1 Receive (Drop) Telecom Bus (associated with Channel 2) will indicate that it is transmitting the C1 byte (via the STS1RXD_D_2[7:0] output pins), by pulsing this output pin "HIGH" (for one period of "STS1RXD_CK_2") and keeping the "STS1RXD_PL_2" output pin pulled "LOW. 2. The STS-1 Receive (Drop) Telecom Bus (associated with Channel 2) will indicate that it is transmitting the J1 byte (via the STS1RXD_D_2[7:0] output pins), by pulsing this output pin "HIGH" (for one period of "STS1RXD_CK_2") while the "STS1TXD_PL_2" output pin is pulled "HIGH". **TXDS3LINECLK_2 (Transmit DS3/E3/STS-1 line clock to LIU – Channel 2)**

B18	STS1RXD_DP_0 TXDS3POS_0	O	CMOS	**STS-1 Receive (Drop) Telecom Bus – Parity Output pin – Channel 0:** The exact function of this output pin depends upon whether the STS-1 Telecom Bus Interface for Channel 0 has been enabled or not. **If STS-1 Telecom Bus (Channel 0) has been enabled** – STS-1 Receive Telecom Bus – Parity Output pin: This output pin can be configured to function as one of the following. The EVEN or ODD parity value of the bits which are output via the "STS1RXD_D_0[7:0]" output pins. The EVEN or ODD parity value of the bits which are being output via the "STS1RXD_D_0[7:0]" output pins and the states of the "STS1RXD_PL_0" and "STS1RXD_C1J1_0" output pins. This output pin will ultimately be used (by "drop-side" circuitry) to verify the verify of the data which is output via the "STS-1 Telecom Bus Interface associated with Channel 0. ***Note:*** *The user can make any one of these configuration selections by writing the appropriate value into the "Telecom Bus Control" Register (Address Location = 0x013B).* **TXDS3POS_0 (Transmit DS3/E3/STS-1 line data positive to LIU– Channel 0)**
G24	STS1RXD_DP_1 TXDS3POS_1	O	CMOS	**STS-1 Receive (Drop) Telecom Bus – Parity Output pin – Channel 1:** The exact function of this output pin depends upon whether the STS-1 Telecom Bus Interface for Channel 1 has been enabled or not. **If STS-1 Telecom Bus (Channel 1) has been enabled** – STS-1 Receive Telecom Bus – Parity Output pin: This output pin can be configured to function as one of the following. The EVEN or ODD parity value of the bits output via the "STS1RXD_D_1[7:0]" output pins. The EVEN or ODD parity value of the bits being output via the "STS1RXD_D_1[7:0]" output pins and the states of the "STS1RXD_PL_1" and "STS1RXD_C1J1_1" output pins. This output pin will ultimately be used (by "drop-side" circuitry) to verify of the data which is output via the "STS-1 Telecom Bus Interface associated with Channel 1. ***Note:*** *The user can make any one of these configuration selections by writing the appropriate value into the "Telecom Bus Control" Register (Address Location = 0x013A).* **TXDS3POS_1 (Transmit DS3/E3/STS-1 line data positive to LIU– Channel 1)**

AG9	STS1RXD_DP_2 TXDS3POS_2	O	CMOS	**STS-1 Receive (Drop) Telecom Bus – Parity Output pin – Channel 2:** The exact function of this output pin depends upon whether the STS-1 Telecom Bus Interface for Channel 2 has been enabled or not. **If STS-1 Telecom Bus (Channel 2) has been enabled** – STS-1 Receive Telecom Bus – Parity Output pin: This output pin can be configured to function as one of the following. The EVEN or ODD parity value of the bits output via the "STS1RXD_D_2[7:0]" output pins. The EVEN or ODD parity value of the bits being output via the "STS1RXD_D_2[7:0]" output pins and the states of the "STS1RXD_PL_2" and "STS1RXD_C1J1_2" output pins. This output pin will ultimately be used (by "drop-side" circuitry) to verify the verify of the data which is output via the "STS-1 Telecom Bus Interface associated with Channel 2. ***Note:*** *The user can make any one of these configuration selections by writing the appropriate value into the "Telecom Bus Control" Register (Address Location = 0x0139).* **TXDS3POS_2 (Transmit DS3/E3/STS-1 line data positive to LIU– Channel 2)**
A19	STS1RXD_ALARM_0 TXDS3NEG_0/	O	CMOS	**STS-1 Receive (Drop) Telecom Bus – Alarm Indicator Output signal – Channel 0:** The exact function of this output pin depends upon whether the STS-1 Telecom Bus Interface for Channel 0 has been enabled or not. **If STS-1 Telecom Bus (Channel 0) has been enabled** – STS-1 Receive Telecom Bus – Alarm Indicator Output signal: This output pin pulses "high", coincident with any STS-1 signal (that is being output via the "STS1RXD_D_0[7:0]" output pins) that is carrying an AIS-P indicator. This output pin is "low" for all other conditions. **TXDS3NEG_0 (Transmit DS3/E3 line data negative to LIU – Channel 0)**
H23	STS1RXD_ALARM_1 TXDS3NEG_1/	O	CMOS	**STS-1 Receive (Drop) Telecom Bus – Alarm Indicator Output signal – Channel 1:** The exact function of this output pin depends upon whether the STS-1 Telecom Bus Interface for Channel 1 has been enabled or not. **If STS-1 Telecom Bus (Channel 1) has been enabled** – STS-1 Receive Telecom Bus – Alarm Indicator Output signal: This output pin pulses "high", coincident with any STS-1 signal (that is being output via the "STS1RXD_D_1[7:0]" output pins) that is carrying an AIS-P indicator. This output pin is "low" for all other conditions. **TXDS3NEG_1 (Transmit DS3/E3 line data negative to LIU – Channel 1)**

AB12	STS1RXD_ALARM_2 TXDS3NEG_2/	O	CMOS	**STS-1 Receive (Drop) Telecom Bus – Alarm Indicator Output signal – Channel 2:** The exact function of this output pin depends upon whether the STS-1 Telecom Bus Interface for Channel 2 has been enabled or not. **If STS-1 Telecom Bus (Channel 2) has been enabled** – STS-1 Receive Telecom Bus – Alarm Indicator Output signal: This output pin pulses "high", coincident with any STS-1 signal (that is being output via the "STS1RXD_D_2[7:0]" output pins) that is carrying an AIS-P indicator. This output pin is "low" for all other conditions. **TXDS3NEG_2 (Transmit DS3/E3 line data negative to LIU – Channel 2)**
F16	STS1RXD_D0_0 RXHDLCDAT_0_0 RXGFCMSB_0	O	CMOS	**Receive STS-1 Telecom Bus – Channel 0 – Output Data Bus pin number 0:** The exact function of this output pin depends upon whether the STS-1 Telecom Bus Interface, associated with Channel 0 is enabled or not. **If STS-1 Telecom Bus (Channel 0) has been enabled** – STS-1 Receive Telecom Bus – Output Data bus pin number 0: STS1RXD_D0_0 This output pin along with "STS1RXD_D_0[7:1]" function as the "STS-1 Receive (Drop) Telecom Bus – Output Data Bus for Channel 0. The STS-1 Telecom Bus Interface will update the data via this output upon the rising edge of "STS1RXD_CK_0:. ***Note:*** *This input pin functions as the LSB (Least Significant Bit) of the Receive (Drop) Telecom Bus for Channel 0.* **RXHDLCDAT_0_0 (Receive HDLC block data output – Channel 0 – Output Data Bus pin 0)** **RXGFCMSB_0 (Receive GFC MSB Indicator – Channel 0)**
E16	STS1RXD_D1_0 RXHDLCDAT_1_0 RXGFC_0	O	CMOS	**Receive STS-1 Telecom Bus – Channel 0 – Output Data Bus pin number 1:** The exact function of this output pin depends upon whether the STS-1 Telecom Bus Interface, associated with Channel 0 is enabled or not. **If STS-1 Telecom Bus (Channel 0) has been enabled** – STS-1 Receive Telecom Bus – Output Data bus pin number 1: STS1RXD_D1_0 This output pin along with "STS1RXD_D_0[7:2]" and "STS1RXD_D0_0 function as the "STS-1 Receive (Drop) Telecom Bus – Output Data Bus for Channel 0. The STS-1 Telecom Bus Interface will update the data via this output upon the rising edge of "STS1RXD_CK_0:. **RXHDLCDAT_1_0 (Receive HDLC block data output – Channel 0 – Output Data Bus pin 1):** **RXGFC_0 (Receive GFC output data – Channel 0)**

D16	STS1RXD_D2_0 RXHDLCDAT_2_0 RXCELLRXED_0	O	CMOS	**Receive STS-1 Telecom Bus – Channel 0 – Output Data Bus pin number 2:** The exact function of this output pin depends upon whether the STS-1 Telecom Bus Interface, associated with Channel 0 is enabled or not. **If STS-1 Telecom Bus (Channel 0) has been enabled –** STS-1 Receive Telecom Bus – Output Data bus pin number 2: STS1RXD_D2_0 This output pin along with "STS1RxD_D_0[7:3]" and "STS1RxD_D_0[1:0]" function as the "STS-3/STM-1 Receive (Drop) Telecom Bus – Output Data Bus for Channel 0. The STS-3/STM-1 Telecom Bus Interface will update the data via this output upon the rising edge of "STS1RxD_CK_0:. **RXHDLCDAT_2_0 (Receive HDLC block data output – Channel 0 – Output Data Bus pin 2)** **RXCELLRXED_0 (Receive cell received indicator – Channel 0)**
B17	STS1RXD_D3_0 RXHDLCDAT_3_0 SSE_CLK	O O IO O	CMOS CMOS TTL/CMOS CMOS	**Receive STS-1 Telecom Bus – Channel 0 – Output Data Bus pin number 3:** The exact function of this output pin depends upon whether the STS-1 Telecom Bus Interface, associated with Channel 0 is enabled or not. **If STS-1 Telecom Bus (Channel 0) has been enabled** – STS-1 Receive Telecom Bus – Output Data bus pin number 3: STS1RXD_D3_0 This output pin along with "STS1RXD_D_0[7:4]" and "STS1RXD_D_0[2:0]" function as the "STS-1 Receive (Drop) Telecom Bus – Output Data Bus for Channel 0. The STS-1 Telecom Bus Interface will update the data via this output upon the rising edge of "STS1RXD_CK_0:. **RXHDLCDAT_3_0 (Receive HDLC block data output – Channel 0 – Output Data Bus pin 3)** **SSE_CLK (Slow Speed Clock Interface for Egress Path)**
C16	STS1RXD_D4_0 RXHDLCDAT_4_0 RXOHIND_0	O	CMOS	**Receive STS-1 Telecom Bus – Channel 0 – Output Data Bus pin number 4:** The exact function of this output pin depends upon whether the STS-1 Telecom Bus Interface, associated with Channel 0 is enabled or not. **If STS-1 Telecom Bus (Channel 0) has been enabled** – STS-1 Receive Telecom Bus – Output Data bus pin number 4: STS1RXD_D4_0 This output pin along with "STS1RXD_D_0[7:5]" and "STS1RXD_D_0[3:0]" function as the "STS-1 Receive (Drop) Telecom Bus – Output Data Bus for Channel 0. The STS-1 Telecom Bus Interface will update the data via this output upon the rising edge of "STS1RXD_CK_0:. **RXHDLCDAT_4_0 (Receive HDLC block data output – Channel 0 – Output Data Bus pin 4)** **RXOHIND_0 (Receive Overhead Indicator – Channel 0)**

A18	STS1RXD_D5_0 RXHDLCDAT_5_0 RXDS3FP_0	O	CMOS	**Receive STS-1 Telecom Bus – Channel 0 – Output Data Bus pin number 5:** The exact function of this output pin depends upon whether the STS-1 Telecom Bus Interface, associated with Channel 0 is enabled or not. **If STS-1 Telecom Bus (Channel 0) has been enabled** – STS-1 Receive Telecom Bus – Output Data bus pin number 5: STS1RXD_D5_0 This output pin along with "STS1RXD_D_0[7:6]" and "STS1RXD_D_0[4:0]" function as the "STS-1 Receive (Drop) Telecom Bus – Output Data Bus for Channel 0. The STS-1 Telecom Bus Interface will update the data via this output upon the rising edge of "STS1RXD_CK_0:. **RXHDLCDAT_5_0 (Receive HDLC block data output – Channel 0 – Output Data Bus pin 5)** **RXDS3FP_0 (Receive DS3 frame pulse – Channel 0)**
B16	STS1RXD_D6_0 RXHDLCDAT_6_0 RXDS3DATA_0	O	CMOS	**Receive STS-1 Telecom Bus – Channel 0 – Output Data Bus pin number 6:** The exact function of this output pin depends upon whether the STS-1 Telecom Bus Interface, associated with Channel 0 is enabled or not. **If STS-1 Telecom Bus (Channel 0) has been enabled** – STS-1 Receive Telecom Bus – Output Data bus pin number 6: STS1RXD_D6_0 This output pin along with "STS1RXD_D7_0" and "STS1RXD_D_0[5:0]" function as the "STS-1 Receive (Drop) Telecom Bus – Output Data Bus for Channel 0. The STS-1 Telecom Bus Interface will update the data via this output upon the rising edge of "STS1RXD_CK_0:. **RXHDLCDAT_6_0 (Receive HDLC block data output – Channel 0 – Output Data Bus pin 6)** **RXDS3DATA_0 (Receive DS3 data – Channel 0)**
A17	STS1RXD_D7_0 RXHDLCDAT_7_0 RXDS3CLK_0	O	CMOS	**Receive STS-1 Telecom Bus – Channel 0 – Output Data Bus pin number 7:** The exact function of this output pin depends upon whether the STS-1 Telecom Bus Interface, associated with Channel 0 is enabled or not. **If STS-1 Telecom Bus (Channel 0) has been enabled** – STS-1 Receive Telecom Bus – Output Data bus pin number 7: STS1RXD_D7_0 This output pin along with "STS1RXD_D_0[6:0]" function as the "STS-1 Receive (Drop) Telecom Bus – Output Data Bus for Channel 0. The STS-1 Telecom Bus Interface will update the data via this output upon the rising edge of "STS1RXD_CK_0:. ***Note:*** *This output pin functions as the MSB (Most Significant Bit) for the STS-1 Receive (Drop) Telecom Bus Interface – Output Data Bus (Channel 0).* **RXHDLCDAT_7_0 (Receive HDLC block data output – Channel 0 – Output Data Bus pin 7)** **RXDS3CLK_0 (Receive DS3 clock – Channel 0)**

F24	STS1RXD_D0_1 RXHDLCDAT_0_1 RXGFCMSB_1	O	CMOS	**Receive STS-1 Telecom Bus – Channel 1 – Output Data Bus pin number 0**: The exact function of this output pin depends upon whether the STS-1 Telecom Bus Interface, associated with Channel 1 is enabled or not. **If STS-1 Telecom Bus (Channel 1) has been enabled** – STS-1 Receive Telecom Bus – Output Data bus pin number 0: STS1RXD_D0_1 This output pin along with "STS1RXD_D_1[7:1]" function as the "STS-1 Receive (Drop) Telecom Bus – Output Data Bus for Channel 1. The STS-1 Telecom Bus Interface will update the data via this output upon the rising edge of "STS1RXD_CK_1. ***Note:*** *This input pin functions as the LSB (Least Significant Bit) of the Receive (Drop) Telecom Bus for Channel 1.* **RXHDLCDAT_0_1 (Receive HDLC block data output – Channel 1 – Output Data Bus pin 0)** **RXGFCMSB_1 (Receive GFC MSB Indicator – Channel 1)**
H22	STS1RXD_D1_1 RXHDLCDAT_1_1 RXGFC_1	O	CMOS	**Receive STS-1 Telecom Bus – Channel 1 – Output Data Bus pin number 1:** The exact function of this output pin depends upon whether the STS-1 Telecom Bus Interface, associated with Channel 1 is enabled or not. **If STS-1 Telecom Bus (Channel 1) has been enabled** – STS-1 Receive Telecom Bus – Output Data bus pin number 1: STS1RXD_D1_1 This output pin along with "STS1RXD_D_1[7:2]" and "STS1RXD_D0_1 function as the "STS-1 Receive (Drop) Telecom Bus – Output Data Bus for Channel 1. The STS-1 Telecom Bus Interface will update the data via this output upon the rising edge of "STS1RXD_CK_1. **RXHDLCDAT_1_1 (Receive HDLC block data output – Channel 1 – Output Data Bus pin 1)** **RXGFC_1 (Receive GFC output data – Channel 1)**
D25	STS1RXD_D2_1 RXHDLCDAT_2_1 RXCELLRXED_1	O	CMOS	**Receive STS-1 Telecom Bus – Channel 1 – Output Data Bus pin number 2:** The exact function of this output pin depends upon whether the STS-1 Telecom Bus Interface, associated with Channel 1 is enabled or not. **If STS-1 Telecom Bus (Channel 1) has been enabled** – STS-1 Receive Telecom Bus – Output Data bus pin number 2: STS1RXD_D2_1 This output pin along with "STS1RXD_D_1[7:3]" and "STS1RXD_D_1[1:0]" function as the "STS-1 Receive (Drop) Telecom Bus – Output Data Bus for Channel 1. The STS-1 Telecom Bus Interface will update the data via this output upon the rising edge of "STS1RXD_CK_1. **RXHDLCDAT_2_1 (Receive HDLC block data output – Channel 1 – Output Data Bus pin 2)** **RXCELLRXED_1 (Receive cell received indicator – Channel 1)**

G23	STS1RXD_D3_1 RXHDLCDAT_3_1 SSE_POS	O O IO O	CMOS CMOS TTL/CMOS CMOS	**Receive STS-1 Telecom Bus – Channel 1 – Output Data Bus pin number 3:** The exact function of this output pin depends upon whether the STS-1 Telecom Bus Interface, associated with Channel 1 is enabled or not. **If STS-1 Telecom Bus (Channel 1) has been enabled** – STS-1 Receive Telecom Bus – Output Data bus pin number 3: STS1RXD_D3_1 This output pin along with "STS1RXD_D_1[7:4]" and "STS1RXD_D_1[2:0]" function as the "STS-1 Receive (Drop) Telecom Bus – Output Data Bus for Channel 1. The STS-1 Telecom Bus Interface will update the data via this output upon the rising edge of "STS1RXD_CK_1. **RXHDLCDAT_3_1 (Receive HDLC block data output – Channel 1 – Output Data Bus pin 3)** **SSE_POS (Slow Speed Interface Data Positive for Egress Path)**
D23	STS1RXD_D4_1 RXHDLCDAT_4_1 RXOHIND_1	O	CMOS	**Receive STS-1 Telecom Bus – Channel 1 – Output Data Bus pin number 4:** The exact function of this output pin depends upon whether the STS-1 Telecom Bus Interface, associated with Channel 1 is enabled or not. **If STS-1 Telecom Bus (Channel 1) has been enabled** – STS-1 Receive Telecom Bus – Output Data bus pin number 4: STS1RXD_D4_1 This output pin along with "STS1RXD_D_1[7:5]" and "STS1RXD_D_1[3:0]" function as the "STS-1 Receive (Drop) Telecom Bus – Output Data Bus for Channel 1. The STS-1 Telecom Bus Interface will update the data via this output upon the rising edge of "STS1RXD_CK_1. **RXHDLCDAT_4_1 (Receive HDLC block data output – Channel 1 – Output Data Bus pin 4)** **RXOHIND_1 (Receive Overhead Indicator – Channel 1)**
E21	STS1RXD_D5_1 RXHDLCDAT_5_1 RXDS3FP_1	O	CMOS	**Receive STS-1 Telecom Bus – Channel 1 – Output Data Bus pin number 5:** The exact function of this output pin depends upon whether the STS-1 Telecom Bus Interface, associated with Channel 1 is enabled or not. **If STS-1 Telecom Bus (Channel 1) has been enabled** – STS-1 Receive Telecom Bus – Output Data bus pin number 5: STS1RXD_D5_1 This output pin along with "STS1RXD_D_1[7:6]" and "STS1RXD_D_1[4:0]" function as the "STS-1 Receive (Drop) Telecom Bus – Output Data Bus for Channel 1. The STS-1 Telecom Bus Interface will update the data via this output upon the rising edge of "STS1RXD_CK_1. **RXHDLCDAT_5_1 (Receive HDLC block data output – Channel 1 – Output Data Bus pin 5)** **RXDS3FP_1 (Receive DS3 frame pulse – Channel 1)**

C24	STS1RXD_D6_1 RXHDLCDAT_6_1 RXDS3DATA_1	O	CMOS	**Receive STS-1 Telecom Bus – Channel 1 – Output Data Bus pin number 6:** The exact function of this output pin depends upon whether the STS-1 Telecom Bus Interface, associated with Channel 1 is enabled or not. **If STS-1 Telecom Bus (Channel 1) has been enabled** – STS-1 Receive Telecom Bus – Output Data bus pin number 6: STS1RXD_D6_1 This output pin along with "STS1RXD_D7_1" and "STS1RXD_D_1[5:0]" function as the "STS-1 Receive (Drop) Telecom Bus – Output Data Bus for Channel 1. The STS-1 Telecom Bus Interface will update the data via this output upon the rising edge of "STS1RXD_CK_1. **RXHDLCDAT_6_1 (Receive HDLC block data output – Channel 1 – Output Data Bus pin 6):** **RXDS3DATA_1 (Receive DS3 data – Channel 1):**
F20	STS1RXD_D7_1 RXHDLCDAT_7_1 RXDS3CLK_1	O	CMOS	**Receive STS-1 Telecom Bus – Channel 1 – Output Data Bus pin number 7:** The exact function of this output pin depends upon whether the STS-1 Telecom Bus Interface, associated with Channel 1 is enabled or not. **If STS-1 Telecom Bus (Channel 1) has been enabled** – STS-1 Receive Telecom Bus – Output Data bus pin number 7: STS1RXD_D7_1 This output pin along with "STS1RXD_D_1[6:0]" function as the "STS-1 Receive (Drop) Telecom Bus – Output Data Bus for Channel 1. The STS-1 Telecom Bus Interface will update the data via this output upon the rising edge of "STS1RXD_CK_1. ***Note:*** *This output pin functions as the MSB (Most Significant Bit) for the STS-1 Receive (Drop) Telecom Bus Interface – Output Data Bus (Channel 1).* **RXHDLCDAT_7_1 (Receive HDLC block data output – Channel 1 – Output Data Bus pin 7)** **RXDS3CLK_1 (Receive DS3 clock – Channel 1)**

AC12	STS1RXD_D0_2 RXHDLCDAT_0_2 RXGFCMSB_2	O	CMOS	**Receive STS-1 Telecom Bus – Channel 2 – Output Data Bus pin number 0:** The exact function of this output pin depends upon whether the STS-1 Telecom Bus Interface, associated with Channel 2 is enabled or not. **If STS-1 Telecom Bus (Channel 2) has been enabled** – STS-1 Receive Telecom Bus – Output Data bus pin number 0: STS1RXD_D0_2 This output pin along with "STS1RXD_D_2[7:1]" function as the "STS-1 Receive (Drop) Telecom Bus – Output Data Bus for Channel 2. The STS-1 Telecom Bus Interface will update the data via this output upon the rising edge of "STS1RXD_CK_2. ***Note:*** *This input pin functions as the LSB (Least Significant Bit) of the Receive (Drop) Telecom Bus for Channel 2.* **RXHDLCDAT_0_2 (Receive HDLC block data output – Channel 2 – Output Data Bus pin 0)** **RXGFCMSB_2 (Receive GFC MSB Indicator – Channel 2)**
AD12	STS1RXD_D1_2 RXHDLCDAT_1_2 RXGFC_2	O	CMOS	**Receive STS-1 Telecom Bus – Channel 2 – Output Data Bus pin number 1:** The exact function of this output pin depends upon whether the STS-1 Telecom Bus Interface, associated with Channel 2 is enabled or not. **If STS-1 Telecom Bus (Channel 2) has been enabled** – STS-1 Receive Telecom Bus – Output Data bus pin number 1: STS1RXD_D1_2 This output pin along with "STS1RXD_D_2[7:2]" and "STS1RXD_D0_2 function as the "STS-1 Receive (Drop) Telecom Bus – Output Data Bus for Channel 2. The STS-1 Telecom Bus Interface will update the data via this output upon the rising edge of "STS1RXD_CK_2. **RXHDLCDAT_1_2 (Receive HDLC block data output – Channel 2 – Output Data Bus pin 1)** **RXGFC_2 (Receive GFC output data – Channel 2)**
AF11	STS1RXD_D2_2 RXHDLCDAT_2_2 RXCELLRXED_2	O	CMOS	**Receive STS-1 Telecom Bus – Channel 2 – Output Data Bus pin number 2:** The exact function of this output pin depends upon whether the STS-1 Telecom Bus Interface, associated with Channel 2 is enabled or not. **If STS-1 Telecom Bus (Channel 2) has been enabled** – STS-1 Receive Telecom Bus – Output Data bus pin number 2: STS1RXD_D2_2 This output pin along with "STS1RXD_D_2[7:3]" and "STS1RXD_D_2[1:0]" function as the "STS-1 Receive (Drop) Telecom Bus – Output Data Bus for Channel 2. The STS-1 Telecom Bus Interface will update the data via this output upon the rising edge of "STS1RXD_CK_2. **RXHDLCDAT_2_2 (Receive HDLC block data output – Channel 2 – Output Data Bus pin 2)** **RXCELLRXED_2 (Receive cell received indicator – Channel 2)**

AE12	STS1RXD_D3_2 RXHDLCDAT_3_2 SSE_NEG	O O IO O	CMOS CMOS TTL/CMOS CMOS	**Receive STS-1 Telecom Bus – Channel 2 – Output Data Bus pin number 3:** The exact function of this output pin depends upon whether the STS-1 Telecom Bus Interface, associated with Channel 2 is enabled or not. **If STS-1 Telecom Bus (Channel 2) has been enabled** – STS-1 Receive Telecom Bus – Output Data bus pin number 3: STS1RXD_D3_2 This output pin along with "STS1RXD_D_2[7:4]" and "STS1RXD_D_2[2:0]" function as the "STS-1 Receive (Drop) Telecom Bus – Output Data Bus for Channel 2. The STS-1 Telecom Bus Interface will update the data via this output upon the rising edge of "STS1RXD_CK_2. **RXHDLCDAT_3_2 (Receive HDLC block data output – Channel 2 – Output Data Bus pin 3)** **SSE_NEG (Slow Speed Interface Data Negative for Egress Path)**
AG10	STS1RXD_D4_2 RXHDLCDAT_4_2 RXOHIND_2	O	CMOS	**Receive STS-1 Telecom Bus – Channel 2 – Output Data Bus pin number 4:** The exact function of this output pin depends upon whether the STS-1 Telecom Bus Interface, associated with Channel 2 is enabled or not. **If STS-1 Telecom Bus (Channel 2) has been enabled** – STS-1 Receive Telecom Bus – Output Data bus pin number 4: STS1RXD_D4_2 This output pin along with "STS1RXD_D_2[7:5]" and "STS1RXD_D_2[3:0]" function as the "STS-1 Receive (Drop) Telecom Bus – Output Data Bus for Channel 2. The STS-1 Telecom Bus Interface will update the data via this output upon the rising edge of "STS1RXD_CK_2. **RXHDLCDAT_4_2 (Receive HDLC block data output – Channel 2 – Output Data Bus pin 4)** **RXOHIND_2 (Receive Overhead Indicator – Channel 2)**
AF12	STS1RXD_D5_2 RXHDLCDAT_5_2 RXDS3FP_2	O	CMOS	**Receive STS-1 Telecom Bus – Channel 2 – Output Data Bus pin number 5:** The exact function of this output pin depends upon whether the STS-1 Telecom Bus Interface, associated with Channel 2 is enabled or not. **If STS-1 Telecom Bus (Channel 2) has been enabled** – STS-1 Receive Telecom Bus – Output Data bus pin number 5: STS1RXD_D5_2 This output pin along with "STS1RXD_D_2[7:6]" and "STS1RXD_D_2[4:0]" function as the "STS-1 Receive (Drop) Telecom Bus – Output Data Bus for Channel 2. The STS-1 Telecom Bus Interface will update the data via this output upon the rising edge of "STS1RXD_CK_2. **RXHDLCDAT_5_2 (Receive HDLC block data output – Channel 2 – Output Data Bus pin5):** This output pin along with RxHDLCDat_ **RXDS3FP_2 (Receive DS3 frame pulse – Channel 2)**

AG11	STS1RXD_D6_2 RXHDLCDAT_6_2 RXDS3DATA_2	O	CMOS	**Receive STS-1 Telecom Bus – Channel 2 – Output Data Bus pin number 6:** The exact function of this output pin depends upon whether the STS-1 Telecom Bus Interface, associated with Channel 2 is enabled or not. **If STS-1 Telecom Bus (Channel 2) has been enabled** – STS-1 Receive Telecom Bus – Output Data bus pin number 6: STS1RXD_D6_2 This output pin along with "STS1RXD_D7_2" and "STS1RXD_D_2[5:0]" function as the "STS-1 Receive (Drop) Telecom Bus – Output Data Bus for Channel 2. The STS-1 Telecom Bus Interface will update the data via this output upon the rising edge of "STS1RXD_CK_2. **RXHDLCDAT_6_2 (Receive HDLC block data output – Channel 2 – Output Data Bus pin 6)** **RXDS3DATA_2 (Receive DS3 data – Channel 2)**
AG12	STS1RXD_D7_2 RXHDLCDAT_7_2 RXDS3CLK_2	O	CMOS	**Receive STS-1 Telecom Bus – Channel 2 – Output Data Bus pin number 7:** The exact function of this output pin depends upon whether the STS-1 Telecom Bus Interface, associated with Channel 2 is enabled or not. **If STS-1 Telecom Bus (Channel 2) has been enabled** – STS-1 Receive Telecom Bus – Output Data bus pin number 7: STS1RXD_D7_2 This output pin along with "STS1RXD_D_2[6:0]" function as the "STS-1 Receive (Drop) Telecom Bus – Output Data Bus for Channel 2. The STS-1 Telecom Bus Interface will update the data via this output upon the rising edge of "STS1RXD_CK_2. ***Note:*** *This output pin functions as the MSB (Most Significant Bit) for the STS-1 Receive (Drop) Telecom Bus Interface – Output Data Bus (Channel 2).* **RXHDLCDAT_7_2 (Receive HDLC block data output – Channel 2 – Output Data Bus pin 7)** **RXDS3CLK_2 (Receive DS3 clock – Channel 2)**

RECEIVE TRANSPORT OVERHEAD INTERFACE				
AD5	RxTOHClk	O	CMOS	**Receive TOH Output Port – Clock Output:** This output pin, along with "RxTOH, RxTOHValid and "RxTOHFrame" function as the "Receive TOH Output Port". The Receive TOH Output Port permits the user to obtain the value of the TOH Bytes, within the incoming STS-3/STM-1 signal. This output pin provides the user with a clock signal. If the "RxTOHValid" output pin is "HIGH", then the contents of the "TOH" bytes, within the incoming STS-3 data-stream will be serially output via the "RxTOH" output. This data will be updated upon the falling edge of this clock signal. Therefore, the user is advised to sample the data (at the "RxTOH" output pin) upon the rising edge of this clock output signal.
AC7	RxTOHValid	O	CMOS	**Receive TOH Output Port – TOH Valid (or READY) indicator:** This output pin, along with "RxTOH" and "RxTOHFrame" function as the "Receive TOH Output Port". This output pin will toggle "HIGH" whenever valid "TOH" data is being output via the "RxTOH" output pin.
AE4	RxTOH	O	CMOS	**Receive TOH Output port – Output pin:** This output pin, along with "RxTOHClk", RxTOHValid" and "RxTOHFrame" function as the "Receive TOH Output port. All TOH data that resides within the incoming STS-3 data-stream will be output via this output pin. The "RxTOHValid" output pin will toggle high, coincident with anytime a bit (from the Receive STS-3 TOH data) is being output via this output pin. The "RxTOHFrame" output pin will pulse "high" (for eight periods of "RxTOHClk") coincident to when the A1 byte is being output via this output pin. Data, on this output pin, is updated upon the falling edge of "RxTOHClk".
AB8	RxTOHFrame	O	CMOS	**Receive TOH Output Port – STS-3/STM-1 Frame Indicator:** This output pin, along with the "RxTOHClk", "RxTOHValid" and "RxTOH" output pins function as the "Receive TOH Output port". This output pin will pulse "high", for one period of "RxTOHClk", one "RxTOHClk" period prior to the very first "TOH" bit (of a given STS-3 frame) being output via the "RxTOH" output pin.

AD7	RxLDCCVAL	O	CMOS	**Receive – Line DCC Output Port – DCC Value Indicator Output pin:** This output pin, along with the "RxTOHClk" and the "RxLDCC" output pins function as the "Receive Line DCC" output port of the XRT94L33. This output pin pulses "High" coincident to when the "Receive Line DCC" output port outputs a DCC bit via the "RxLDCC" output pin. This output pin is updated upon the falling edge of "RxTOHClk". The Line DCC HDLC Controller circuitry that is interfaced to this output pin, the "RxLDCC" and the "RxTOHClk" pins is suppose to do the following. It should continuously sample and monitor the state of this output pin upon the rising edge of "RxTOHClk". Anytime the "Line DCC HDLC" circuitry samples this output pin being "HIGH", it should sample and latch the data on the "RxLDCC" output pin (as a valid Line DCC bit) into the "Line DCC HDLC" circuitry.
AE5	RxLDCC	O	CMOS	**Receive – Line DCC Output Port – Output Pin:** This output pin, along with "RxLDCCVAL" and the "RxTOHClk" output pins function as the "Receive Line DCC" output port of the XRT94L33. This pin outputs the contents of the Line DCC (e.g., the D4, D5, D6, D7, D8, D9, D10, D11 and D12 bytes), within the incoming STS-3 data-stream. The Receive Line DCC Output port will assert the "RxLDCCVAL" output pin, in order to indicate that the data, residing on the "RxLDCC" output pin is a valid Line DCC byte. The Receive Line DCC output port will update the "RxLDCCVAL" and the "RxLDCC" output pins upon the falling edge of the "RxTOHClk" output pin. The Line DCC HDLC circuitry that is interfaced to this output pin, the "RxLDCCVAL" and the "RxTOHClk" pins is suppose to do the following. It should continuously sample and monitor the state of the "RxLDCCVAL" output pin upon the rising edge of "RxTOHClk". Anytime the "Line DCC HDLC" circuitry samples the "RxLDCCVAL" output pin "HIGH", it should sample and latch the contents of this output pin (as a valid Line DCC bit) into the "Line DCC HDLC" circuitry.
AD8	RxE1F1E2FP	O	CMOS	**Receive – Order-Wire Output Port – Frame Boundary Indicator:** This output pin, along with "RxE1F1E2", "RxE1F1E2Val" and the "RxTOHClk" output pins function as the "Receive Order-Wire Output port of the XRT94L33. This output pin pulses "high" (for one period of "RxTOHClk") coincident to when the very first bit (of the E1 byte) is being output vi the "RxE1F1E2" output pin.

AC9	RxE1F1E2	O	CMOS	**Receive – Order-Wire Output Port – Output Pin:** This output pin, along with "RxE1F1E2Val", "RxE1F1F2FP, and the "RxTOHClk" output pins function as the "Receive Order-Wire Output Port of the XRT94L33. This pin outputs the contents of the "Order-Wire" bytes (e.g., the E1, F1 and E2 bytes) within the incoming STS-3 data-stream. The Receive Order-Wire Output port will pulse the "RxE1F1E2FP" output pin "high" (for one period of "RxTOHClk") coincident to when the very first bit (of the E1 byte) is being output via the "RxE1F1E2" output pin. Additionally, the Receive Order-Wire Output port will also assert the "RxE1F1E2Val" output pin, in order to indicate that the data, residing on the "RxE1F1E2" output pin is valid "Order-Wire" byte. The Receive Order-Wire output port will update the "RxE1F1E2Val", the "RxE1F1E2FP" and the "RxE1F1E2" output pins upon the falling edge of the "RxTOHClk" output pin. The "Receive Order-Wire" circuitry that is interfaced to this output pin, and the "RxE1F1E2Val", the "RxE1F1E2" and the "RxTOHClk" pins is suppose to do the following. It should continuously sample and monitor the state of the "RxE1F1E2Val" and "RxE1F1E2FP" output pins upon the rising edge of "RxTOHClk". Anytime the "Order-wire" circuitry samples the "RxE1F1E2Val" and "RxE1F1E2FP output pins "HIGH, it should begin to sample and latch the contents of this output pin (as a valid "Order-Wire" bit) into the "Order-Wire" circuitry. The "Order-Wire" circuitry should continue to sample and latch the contents of the output pin until the "RxE1F2E2Val" output pin is sampled "low".
AC8	RxSDCC	O	CMOS	**Receive – Section DCC Output Port – Output Pin:** This output pin, along with "RxSDCCVAL" and the "RxTOHClk" output pins function as the "Receive Section DCC" output port of the XRT94L33. This pin outputs the contents of the Section DCC (e.g., the D1, D2 and D3 bytes), within the incoming STS-3 data-stream. The Receive Section DCC Output port will assert the "RxSDCCVAL" output pin, in order to indicate that the data, residing on the "RxSDCC" output pin is a valid Section DCC byte. The Receive Section DCC output port will update the "RxSDCCVAL" and the "RxSDCC" output pins upon the falling edge of the "RxTOHClk" output pin. The Section DCC HDLC circuitry that is interfaced to this output pin, the "RxSDCCVAL" and the "RxTOHClk" pins is suppose to do the following. It should continuously sample and monitor the state of the "RxSDCCVAL" output pin upon the rising edge of "RxTOHClk". Anytime the "Section DCC HDLC" circuitry samples the "RxSDCCVAL" output pin "HIGH", it should sample and latch the contents of this output pin (as a valid Section DCC bit) into the "Section DCC HDLC" circuitry.

AD6	RxSDCCVAL	O	CMOS	**Receive – Section DCC Output Port – DCC Value Indicator Output pin:** This output pin, along with the "RxTOHClk" and the "RxSDCC" output pins function as the "Receive Section DCC" output port of the XRT94L33. This output pin pulses "High" coincident to when the "Receive Section DCC" output port outputs a DCC bit via the "RxSDCC" output pin. This output pin is updated upon the falling edge of "RxTOHClk". The Section DCC HDLC Controller circuitry that is interfaced to this output pin, the "RxSDCC" and the "RxTOHClk" pins is suppose to do the following. It should continuously sample and monitor the state of this output pin upon the rising edge of "RxTOHClk". Anytime the "Section DCC HDLC" circuitry samples this output pin being "HIGH", it should sample and latch the data on the "RxSDCC" output pin (as a valid Section DCC bit) into the "Section DCC HDLC" circuitry.
AF4	RxE1F1E2VAL	O	CMOS	**Receive – Order Wire Output Port – E1F1E2 Value Indicator Output Pin:** This output pin, along with the "RxTOHClk", "RxE1F1E2FP", "RxE1F1E2" and "RxTOHClk" output pins function as the "Receive – Order Wire Output Port" of the XRT94L33. This output pin pulses "high" coincident to when the "Receive – Order Wire" output port outputs the contents of an E1, F1 or E2 byte, via the "RxE1F1E2" output pin. This output pin is updated upon the falling edge of "RxTOHClk". The "Receive Order-Wire" circuitry, that is interfaced to this output pin, the "RxE1F1E2" and the "RxTOHClk" pins is suppose to do the following. It should continuously sample and monitor the state of this output pin upon the rising edge of "RxTOHClk". Anytime the "Receive Order-Wire" circuitry samples this output pin being "high", it should sample and latch the data on the "RxE1F1E2" output pin (as a valid Order-wire bit) into the "Receive Order-Wire" circuitry.
AE6	RXPOH	O	CMOS	**Receive AU-4/VC-4/STS-3c Mapper POH Processor Block – Path Overhead Output Port – Output Pin:** This output pin, along with the "RxPOHClk", "RxPOHFrame" and "RxPOHValid" function as the "AU-4/VC-4 Mapper POH Processor block – POH Output port. These pins serially output the POH data that have been received by the Receive AU-4/VC-4 Mapper POH Processor block (via the "incoming" STS-3 data-stream). Each bit, within the POH bytes is updated (via these output pins) upon the falling edge of "RxPOHClk". As a consequence, external circuitry receiving this data, should sample this data upon the rising edge of "RxPOHClk".

AG4	RXPOHCLK	O	CMOS	**Receive AU-4/VC-4/STS-3c Mapper POH Processor Block – Path Overhead Output Port – Clock Output Signal:** This output pin, along with "RxPOH", "RxPOHFrame" and "RxPOHValid" function as the "AU-4/VC-4 Mapper POH Processor block – POH Output Port. These output pins function as the "Clock Output" signals for the "AU-4/VC-4 Mapper POH Processor Block– POH Output Port. The "RxPOH", "RxPOHFrame" and "RxPOHValid" output pins are updated upon the falling edge of this clock signal. As a consequence, the external circuitry should sample these signals upon the rising edge of this clock signal.
AE7	RXPOHFRAME	O	CMOS	**Receive AU-4/VC-4/STS-3c Mapper POH Processor Block – Path Overhead Output Port – Frame Boundary Indicator:** These output pins, along with the "RxPOH", RxPOHClk" and "RxPOHValid" output pins function as the "AU-4/VC-4 Mapper POH Processor Block – Path Overhead Output Port. These output pins will pulse "high" coincident with the very first POH byte (J1), of a given STS-1 frame, is being output via the corresponding "RxPOH" output pin.
AD9	RXPOHVALID	O	CMOS	**Receive AU-4/VC-4/STS-3c Mapper POH Processor Block – Path Overhead Output Port – Valid POH Data Indicator:** These output pins, along with "RxPOH", "RxPOHClk" and "RxPOHFrame" function as the "AU-4/VC-4 Mapper POH Processor block – Path Overhead Output port. These output pins will toggle "high" coincident with when valid POH data is being output via the "RxPOH" output pins. This output is updated upon the falling edge of RxPOHClk. Hence, external circuitry should sample these signals upon rising edge of "RxPOHClk".
AF5 AG5 AF8	RxPOH_0 RxPOH_1 RxPOH_2	O	CMOS	**Receive SONET POH Processor Block – Path Overhead Output Port – Output Pin:** These output pins, along with the "RxPOHClk_n", "RxPOHFrame_n" and "RxPOHValid_n" function as the "Receive SONET POH Processor block – POH Output port. These pins serially output the POH data that have been received by each of the Receive SONET POH Processor blocks (via the "incoming" STS-3 data-stream). Each bit, within the POH bytes is updated (via these output pins) upon the falling edge of "RxPOHClk_n". As a consequence, external circuitry receiving this data, should sample this data upon the rising edge of "RxPOHClk_n".
AE8 AE9 AG6	RxPOHClk_0 RxPOHClk_1 RxPOHClk_2	O	CMOS	**Receive SONET POH Processor Block – Path Overhead Output Port – Clock Output Signal:** These output pins, along with "RxPOH_n", "RxPOHFrame_n" and "RxPOHValid_n" function as the "Receive SONET POH Processor block – POH Output Port. These output pins function as the "Clock Output" signals for the "Receive SONET POH Processor block – POH Output Port. The "RxPOH_n", "RxPOHFrame_n" and "RxPOHValid_n" output pins are updated upon the falling edge of this clock signal. As a consequence, the external circuitry should sample these signals upon the rising edge of this clock signal.

AF6 AD10 AE10	RxPOHFrame_0 RxPOHFrame_1 RxPOHFrame_2	O	CMOS	**Receive SONET POH Processor Block – Path Overhead Output Port – Frame Boundary Indicator:** These output pins, along with the "RxPOH_n", RxPOHClk_n" and "RxPOHValid_n" output pins function as the "Receive SONET POH Processor Block – Path Overhead Output Port. These output pins will pulse "high" coincident with the very first POH byte (J1), of a given STS-1 frame, is being output via the corresponding "RxPOH_n" output pin.
AC10 AF7 AC11	RxPOHValid_0 RxPOHValid_1 RxPOHValid_2	O	CMOS	**Receive SONET POH Processor Block – Path Overhead Output Port – Valid POH Data Indicator:** These output pins, along with "RxPOH_n", "RxPOHClk_n" and "RxPOHFrame_n" function as the "Receive SONET POH Processor block – Path Overhead Output port. These output pins will toggle "high" coincident with when valid POH data is being output via the "RxPOH_n" output pins. This output is updated upon the falling edge of RxPOHClk_n. Hence, external circuitry should sample these signals upon rising edge of "RxPOHClk_n".
AD11	LOF	O	CMOS	**Receive STS-3 LOF (Loss of Frame) Indicator:** This output pin indicates whether or not the Receive STS-3 TOH Processor block (within the device) is currently declaring the LOF defect condition as described below. LOW – Indicates that the Receive STS-3 TOH Processor block is NOT currently declaring the LOF defect condition. HIGH – Indicates that the Receive STS-3 TOH Processor block is currently declaring the LOF defect condition.
AF9	SEF	O	CMOS	**Receive STS-3 SEF (Severed Errored Frame) Indicator:** This output pin indicates whether or not the Receive STS-3 TOH Processor block (within the device) is currently declaring the SEF defect condition as described below. LOW – Indicates that the Receive STS-3 TOH Processor block is NOT currently declaring the SEF defect condition. HIGH – Indicates that the Receive STS-3 TOH Processor block is currently declaring the SEF defect condition.
AG7	LOS	O	CMOS	**Receive STS-3 LOS (Loss of Signal) Defect Indicator:** This output pin indicates whether or not the Receive STS-3 TOH Processor block (within the device) is currently declaring the LOS defect condition as described below. LOW – Indicates that the Receive STS-3 TOH Processor block is NOT currently declaring the LOS defect condition. HIGH – Indicates that the Receive STS-3 TOH Processor block is currently declaring the LOS defect condition.
GENERAL PURPOSE INPUT/OUTPUT				

W25	GPI0_0	I/O	TTL/CMOS	**General Purpose Input/Output pin:** This input pin can be configured to function as either an input or output pin by writing the appropriate value into Bit 0 (GPIO_DIR_0), within the "Operation General Purpose Input/Output Direction Register – 0" (Address Location = 0x014B). If this pin is configured to be an input pin the state of this pin can be monitored by reading the state of Bit 0 (GPIO_0) within the "Operation General Purpose Input/Output Register – Byte 0" (Address Location = 0x0147). If this pin is configured to be an output pin the state of this pin can be controlled by writing the appropriate value into Bit 0 (GPIO_0) within the "Operation General Purpose Input/Output Register – Byte 0" (Address Location = 0x0147).
AC27	GPIO_1	I/O	TTL/CMOS	**General Purpose Input/Output pin** This input pin can be configured to function as either an input or output pin by writing the appropriate value into Bit 1 (GPIO_DIR_1), within the "Operation General Purpose Input/Output Direction Register – 0" (Address Location = 0x014B). If this pin is configured to be an input pin, then the state of this pin can be monitored by reading the state of Bit 1 (GPIO_1) within the "Operation General Purpose Input/Output Register – Byte 0" (Address Location = 0x0147). If this pin is configured to be an output pin, then the state of this pin can be controlled by writing the appropriate value into Bit 1 (GPIO_1) within the "Operation General Purpose Input/Output Register – Byte 0" (Address Location = 0x0147).
V23	GPIO_2	I/O	TTL/CMOS	**General Purpose Input/Output pin** This input pin can be configured to function as either an input or output pin by writing the appropriate value into Bit 2 (GPIO_DIR_2), within the "Operation General Purpose Input/Output Direction Register – 0" (Address Location = 0x014B). If this pin is configured to be an input pin, then the state of this pin can be monitored by reading the state of Bit 2 (GPIO_2) within the "Operation General Purpose Input/Output Register – Byte 0" (Address Location = 0x0147). If this pin is configured to be an output pin, then the state of this pin can be controlled by writing the appropriate value into Bit 2 (GPIO_2) within the "Operation General Purpose Input/Output Register – Byte 0" (Address Location = 0x0147).

AB26	GPIO_3	I/O	TTL/CMOS	**General Purpose Input/Output pin** This input pin can be configured to function as either an input or output pin by writing the appropriate value into Bit 3 (GPIO_DIR_3), within the "Operation General Purpose Input/Output Direction Register – 0" (Address Location = 0x014B). If this pin is configured to be an input pin, then the state of this pin can be monitored by reading the state of Bit 3 (GPIO_3) within the "Operation General Purpose Input/Output Register – Byte 0" (Address Location = 0x0147). If this pin is configured to be an output pin, then the state of this pin can be controlled by writing the appropriate value into Bit 3 (GPIO_3) within the "Operation General Purpose Input/Output Register – Byte 0" (Address Location = 0x0147).
Y25	GPIO_4	I/O	TTL/CMOS	**General Purpose Input/Output pin** This input pin can be configured to function as either an input or output pin by writing the appropriate value into Bit 4 (GPIO_DIR_4), within the "Operation General Purpose Input/Output Direction Register – 0" (Address Location = 0x014B). If this pin is configured to be an input pin, then the state of this pin can be monitored by reading the state of Bit 4 (GPIO_4) within the "Operation General Purpose Input/Output Register – Byte 0" (Address Location = 0x0147). If this pin is configured to be an output pin, then the state of this pin can be controlled by writing the appropriate value into Bit 4 (GPIO_4) within the "Operation General Purpose Input/Output Register – Byte 0" (Address Location = 0x0147).
AC26	GPIO_5	I/O	TTL/CMOS	**General Purpose Input/Output pin** This input pin can be configured to function as either an input or output pin by writing the appropriate value into Bit 35(GPIO_DIR_5), within the "Operation General Purpose Input/Output Direction Register – 0" (Address Location = 0x014B). If this pin is configured to be an input pin, then the state of this pin can be monitored by reading the state of Bit 5 (GPIO_5) within the "Operation General Purpose Input/Output Register – Byte 0" (Address Location = 0x0147). If this pin is configured to be an output pin, then the state of this pin can be controlled by writing the appropriate value into Bit 5 (GPIO_5) within the "Operation General Purpose Input/Output Register – Byte 0" (Address Location = 0x0147).

W24	GPIO_6	I/O	TTL/CMOS	**General Purpose Input/Output pin** This input pin can be configured to function as either an input or output pin by writing the appropriate value into Bit 6 (GPIO_DIR_6), within the "Operation General Purpose Input/Output Direction Register – 0" (Address Location = 0x014B). If this pin is configured to be an input pin, then the state of this pin can be monitored by reading the state of Bit 6 (GPIO_6) within the "Operation General Purpose Input/Output Register – Byte 0" (Address Location = 0x0147). If this pin is configured to be an output pin, then the state of this pin can be controlled by writing the appropriate value into Bit 6 (GPIO_6) within the "Operation General Purpose Input/Output Register – Byte 0" (Address Location = 0x0147).
AA25	GPIO_7	I/O	TTL/CMOS	**General Purpose Input/Output pin** This input pin can be configured to function as either an input or output pin by writing the appropriate value into Bit 7 (GPIO_DIR_7), within the "Operation General Purpose Input/Output Direction Register – 0" (Address Location = 0x014B). If this pin is configured to be an input pin, then the state of this pin can be monitored by reading the state of Bit 7 (GPIO_7) within the "Operation General Purpose Input/Output Register – Byte 0" (Address Location = 0x0147). If this pin is configured to be an output pin, then the state of this pin can be controlled by writing the appropriate value into Bit 7 (GPIO_7) within the "Operation General Purpose Input/Output Register – Byte 0" (Address Location = 0x0147).

CLOCK INPUTS				
E7	REFCLK34	I	TTL	**E3 Reference Clock Input for the Jitter Attenuator within the DS3/E3 Mapper Block:** To operate any of the channels (within the XRT94L33) in the E3 Mode, apply a clock signal with a frequency of 34.368±20ppm to this input pin. This input pin functions as the timing reference for the DS3/E3/STS-1 Jitter Attenuator (within the DS3/E3 Mapper block) for E3 applications. ***Note:*** *Connect this pin to GND if none of the channels of the XRT94L33 are to be operated in the E3 or if the XRT94L33 is to be operated in the SFM mode.*

D5	REFCLK51	I	TTL	**STS-1 Reference Clock Input for the Jitter Attenuator within the DS3/E3 Mapper Block.** To operate any of the channels (within the XRT94L33) in the STS-1/STM-0 Mode, apply a clock signal with a frequency of 51.84MHz±20ppm to this input pin. This input pin functions as the timing reference for the DS3/E3/STS-1 Jitter Attenuator (within the DS3/E3 Mapper block) for STS-1 applications. ***Notes:*** *If the user intends to operate the XRT94L33 in the SFM Mode, apply a 12.288MHz±20ppm clock signal to this input pin.* *If the user does not intend to operate any of the channels in the STS-1/STM-0 Mode, connect this input pin to GND*.
F7	REFCLK45	I	TTL	**DS3 Reference Clock Input for the Jitter Attenuator within the DS3/E3 Mapper Block:** To operate any of the channels of the XRT94L33 in the DS3 Mode, apply a clock signal with a frequency of 44.736±20ppm to this input pin. This input pin functions as the timing reference for the DS3/E3/STS-1 Jitter Attenuator (within the DS3/E3 Mapper block) for DS3 applications. If the user does not intend to operate any of the three (3) channels within the XRT94L33 in the DS3 Mode, or if the user intends to configure the XRT94L33 to operate in the SFM Mode, then tie this input pin to GND.
BOUNDARY SCAN				
F5	TDO	O	CMOS	**Test Data Out: Boundary Scan Test data output**
F4	TDI	I	TTL	**TEST Data In: Boundary Scan Test data input** ***Note:*** *This input pin should be pulled "Low" for normal operation.*
D3	TRST	I	TTL	**JTAG Test Reset Input**
E4	TCK	I	TTL	**Test clock: Boundary Scan clock input** ***Note:*** *This input pin should be pulled "Low" for normal operation.*
E5	TMS	I	TTL	**Test Mode Select: Boundary Scan Mode Select input** ***Note:*** This *input pin should be pulled "Low" for normal operation.*
FILTERING CAPACITORS				
U6	RXCAPP	I	ANALOG	**External Loop Capacitor for Receive PLL:** This pin connects to the positive side of the external capacitor, which is used to minimize jitter peaking.
U5	RXCAPN	I	ANALOG	**External Loop Capacitor for Receive PLL:** This pin connects to the negative side of the external capacitor, which is used to minimize jitter peaking.

W6	RXCAPP_R	I	ANAL0OG	**External Redundant Loop Capacitor for Receive PLL:** This pin connects to the positive side of the external capacitor, which is used to minimize jitter peaking.
W5	RXCAPN_R	I	ANALOG	**External Redundant Loop Capacitor for Receive PLL:** This pin connects to the negative side of the external capacitor, which is used to minimize jitter peaking.
MISCELLANEOUS PINS				
H5	REFSEL_L	I	TTL	**Clock Synthesizer Block Select:** This input pin permits the user to configure the "Transmit SONET" circuitry (within the XRT94L33) to use either of the following clock signals as its timing source. a. The "Directly-Applied" 19.44MHz clock signal, which is applied to the REFTTL input pin (P1) or, b. The output of the "Clock Synthesizer" block (within the chip). Setting this input pin "HIGH" configures the "Transmit SONET" circuitry within the XRT94L33 to use the "Clock Synthesizer" block as its timing source. In this mode, the user can supply either a 19.44MHz, 38.88MHz, 51.84MHz or 77.76MHz clock signal to the REFTTL input pin. Setting this input pin "LOW" by-passes the "Clock Synthesizer" block. In this case, the user MUST supply a 19.44MHz clock signal to the REFTTL input pin in order to insure proper performance.
K4	SFM	I	TTL	**Single Frequency Mode (SFM) Select:** This input pin permits the user to configure the three Jitter Attenuator blocks within the XRT94L33 to operate in the Single-Frequency Mode (SFM). If the XRT94L33 has been configured to operate in the SFM Mode, then the user only needs to supply a 12.288MHz clock signal to the REFCLK51 input pin. In this case, the user does not need to supply a 44.736MHz clock signal to the REFCLK45 input pin, nor a 34.368MHz clock signal to the REFCLK34 input pin. The SFM PLL (within the XRT94L33) will internally synthesize the appropriate 44.736MHz, 34.368MHz or 51.84MHz clock signals, and will route these signals to the appropriate channels (within the chip) depending upon the data rate that they are configured to operate in. Setting this input pin to a logic "LOW" disables the Single-Frequency Mode. In this mode, the user must supply all of the appropriate frequencies to the REFCLK34, REFCLK45 and REFCLK51 input pins. Setting this input pin to a logic "HIGH" configures the XRT94L33 to operate in the Single-Frequency Mode.
J3	Test Mode	I	TTL	**Test Mode Input Pin:** User should connect this input pin "LOW" for normal operation.
G2	FL_TSTCLK	O	CMOS	**JA Testing Clock:** This pin is used for JA testing purposes.
J2	ANALOG	O	ANALOG	**Analog Output Pin:** This output analog pin is used for testing purposes.

N1	VDCTST1	O	ANALOG	**DC Test Pin:** This pin is used for internal DC test, for example, it can be used to test for DC current, DC voltage.
N2	VDCTST2	O	ANALOG	**DC Test Pin:** This pin is used for internal DC test, for example, it can be used to test for DC current, DC voltage.

NO-CONNECT PINS				
K1	N/C			
AA1	N/C			
V3	N/C			
AB1	N/C			
AA2	N/C			
AC1	N/C			
R1	N/C			
AB2	N/C			
AC2	N/C			
T1	N/C			
AC4	N/C			
AB5	N/C			
AD4	N/C			
AC5	N/C			
AB7	N/C			
AC6	N/C			
AC22	N/C			
AD24	N/C			
AB21	N/C			
AC23	N/C			
AB23	N/C			
AC24	N/C			
AA23	N/C			
E24	N/C			
F23	N/C			
D24	N/C			
E23	N/C			
F21	N/C			
E22	N/C			

VDD (3.3V)				
N23 N25 V5 H2 L2 K3 H1 L5 U4 N3 T5 M5	Analog VDD Pins	_		
U3 R2 R6 C2 C1 J6 K6 W3 Y3 AE1 AE2 AF3 AB9 AB10 AB11 AB17 AB18 AB19 AF25 AE26 W22 V22 U22 L22 K22 J22 C27 C26 B25 A25 F19 F18 F17 F11 F10 F9 A3 B3	Digital VDD			

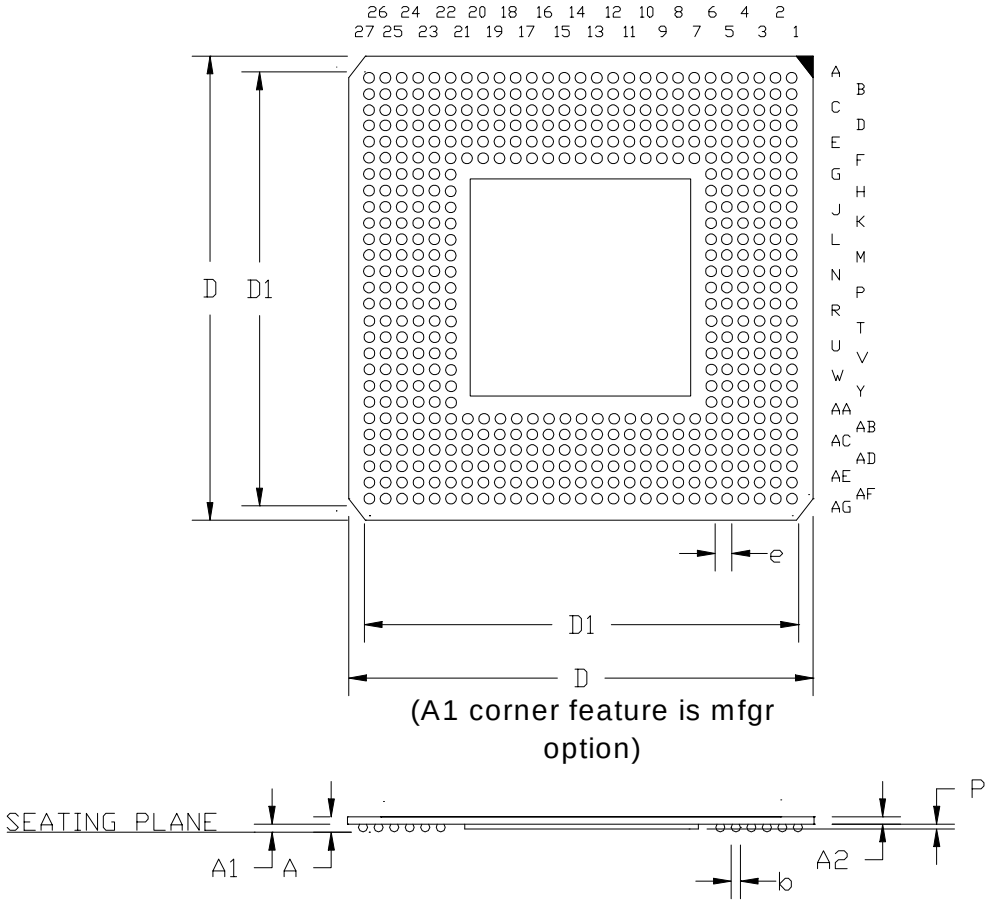
D4 C4				

GROUND				
G6 C3 A1 B1 AF1 AF2 AA6 AB6 AE3 AG1 AG2 AB13 AB14 AB15 AG26 AF26 AB22 AA22 AE25 AG27 AF27 T22 R22 P22 N22 M22 B27 B26 G22 F22 C25 A27 A26 F15 F14 F13 A2 B2 F6 V2 W4 Y6 Y5 Y4 E6 V4 R5 R3 P4	Digital Ground			

V6 L6 T4 N24 N26 R4 F1 K2 G1 L1 M6 N4 T6 J1	Analog Ground			

Package Outline Drawing

504 Tape Ball Grid Array
(35 mm x 35 mm - TBGA)
Bottom View



Note: The control dimension is in millimeter.

	INCHES		MILLIMETERS	
SYMBOL	**MIN**	**MAX**	**MIN**	**MAX**
A	0.051	0.067	1.30	1.70
A1	0.020	0.028	0.50	0.70
A2	0.031	0.039	0.80	1.00
D	1.370	1.386	34.80	35.20
D1	1.300 BSC		33.02 BSC	
b	0.024	0.035	0.60	0.90
e	0.050 BSC		1.27 BSC	
P	0.006	0.012	0.15	0.30

NOTES:

Rev. 2.0.0 – Pinlist and package outline information only supplied in this document.

NOTICE

Datasheet November 2006