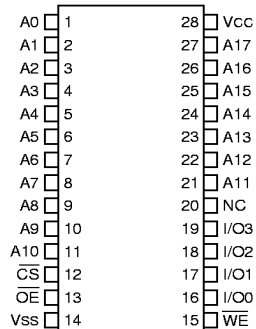




256Kx4 SRAM MONOLITHIC

PIN CONFIGURATION TOP VIEW



PIN DESCRIPTION

A0-17	Address Inputs
I/O0-3	Data Input/Output
\overline{CS}	Chip Select
\overline{OE}	Output Enable
\overline{WE}	Write Enable
Vcc	+5.0V Power
Vss	Ground
NC	Not Connected

FEATURES

- Access Times 25, 35, 45ns
- MIL-STD-883 Compliant Devices Available
- Packaging
 - JEDEC Standard 28 lead, Hermetic Ceramic SOJ (Package 103)
- Commercial, Industrial and Military Temperature Ranges
- Organized as 256K x 4
- 5 Volt Power Supply
- Low Power CMOS
- TTL Compatible Inputs and Outputs
- 2V Data Retention Devices also Available for Battery Back-Up Operation



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T _A	-55	+125	°C
Storage Temperature	T _{STG}	-65	+150	°C
Signal Voltage Relative to GND	V _G	-0.5	V _{CC} +0.5	V
Junction Temperature	T _J		150	°C
Supply Voltage	V _{CC}	-0.5	7.0	V

TRUTH TABLE

\overline{CS}	\overline{OE}	\overline{WE}	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active
L	H	H	Out Disable	High Z	Active

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V _{CC}	4.5	5.5	V
Input High Voltage	V _{IH}	2.2	V _{CC} + 0.3	V
Input Low Voltage	V _{IL}	-0.5	+0.8	V
Operating Temp. (Mil.)	T _A	-55	+125	°C

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Condition	Max	Unit
Input capacitance	C _{IN}	V _{IN} = 0V, f = 1.0MHz	15	pF
Output capacitance	C _{OUT}	V _{OUT} = 0V, f = 1.0MHz	15	pF

This parameter is guaranteed by design but not tested.

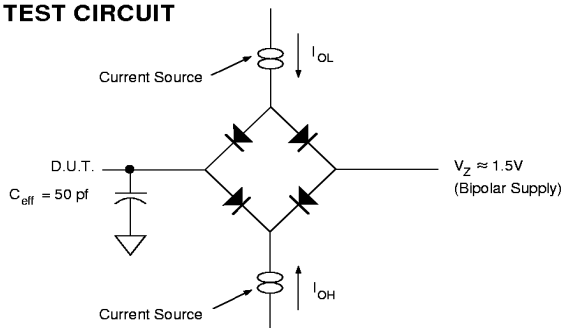
DC CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Sym	Conditions			Units
			Min	Max	
Input Leakage Current	I _{LI}	V _{CC} = 5.5, V _{IN} = GND to V _{CC}		10	μA
Output Leakage Current	I _{LO}	\overline{CS} = V _{IH} , \overline{OE} = V _{IH} , V _{OUT} = GND to V _{CC}		10	μA
Operating Supply Current	I _{CC}	\overline{CS} = V _{IL} , \overline{OE} = V _{IH} , f = 5MHz, V _{CC} = 5.5		110	mA
Standby Current	I _{SB}	\overline{CS} = V _{IH} , \overline{OE} = V _{IH} , f = 5MHz		30	mA
Output Low Voltage	V _{OL}	I _{OL} = 8mA, V _{CC} = 4.5		0.4	V
Output High Voltage	V _{OH}	I _{OH} = -4.0mA, V _{CC} = 4.5	2.4		V

NOTE: DC test conditions: V_{IH} = V_{CC} - 0.3V, V_{IL} = 0.3V

AC TEST CIRCUIT



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V _{IL} = 0, V _{IH} = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:

V_Z is programmable from -2V to +7V.
 I_{OL} & I_{OH} programmable from 0 to 16mA.
 Tester Impedance Z₀ = 75 Ω.
 V_Z is typically the midpoint of V_{OH} and V_{OL}.
 I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
 ATE tester includes jig capacitance.

**AC CHARACTERISTICS**(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	-25		-35		-45		Units
		Min	Max	Min	Max	Min	Max	
Read Cycle								
Read Cycle Time	t _{RC}	25		35		45		ns
Address Access Time	t _{AA}		25		35		45	ns
Output Hold from Address Change	t _{OH}	0		0		0		ns
Chip Select Access Time	t _{ACS}		25		35		45	ns
Output Enable to Output Valid	t _{OE}		13		15		20	ns
Chip Select to Output in Low Z	t _{CLZ} ¹	5		5		5		ns
Output Enable to Output in Low Z	t _{OLZ} ¹	5		5		5		ns
Chip Disable to Output in High Z	t _{CHZ} ¹		15		15		15	ns
Output Disable to Output in High Z	t _{OHZ} ¹		15		15		15	ns

1. This parameter is guaranteed by design but not tested.

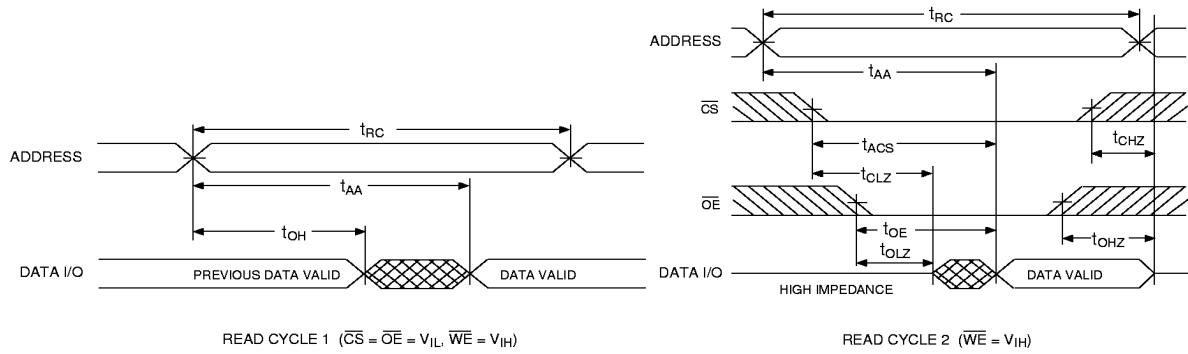
AC CHARACTERISTICS(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	-25		-35		-45		Units
		Min	Max	Min	Max	Min	Max	
Write Cycle								
Write Cycle Time	t _{WC}	25		35		45		ns
Chip Select to End of Write	t _{CW}	20		25		30		ns
Address Valid to End of Write	t _{AW}	20		25		30		ns
Data Valid to End of Write	t _{DW}	15		20		25		ns
Write Pulse Width	t _{WP}	20		25		30		ns
Address Setup Time	t _{AS}	2		2		2		ns
Address Hold Time	t _{AH}	0		0		0		ns
Output Active from End of Write	t _{OW} ¹	5		5		5		ns
Write Enable to Output in High Z	t _{WHZ} ¹	0	10	0	15	0	20	ns
Data Hold Time	t _{DH}	0		0		0		ns

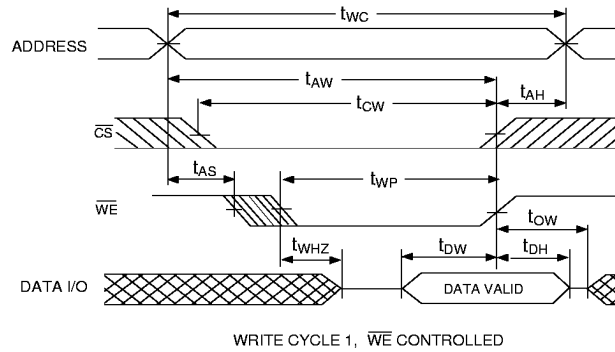
1. This parameter is guaranteed by design but not tested.



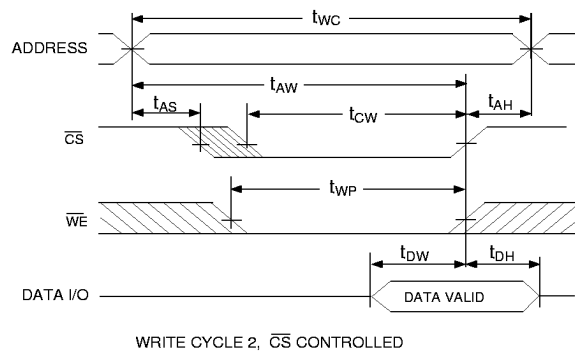
TIMING WAVEFORM - READ CYCLE



WRITE CYCLE - \overline{WE} CONTROLLED

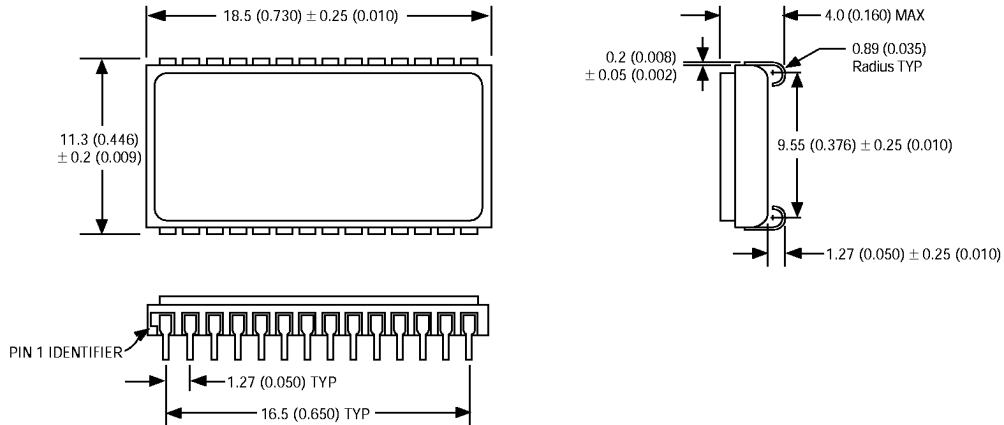


WRITE CYCLE - \overline{CS} CONTROLLED





PACKAGE 103: 28 LEAD, CERAMIC SOJ



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION

W M S 256K 4 - XXX DS X X

LEAD FINISH:

- Blank = Gold plated leads
- A = Solder dip leads

DEVICE GRADE:

- M = Military Screened -55°C to +125°C
- I = Industrial -40°C to +85°C
- C = Commercial 0°C to +70°C

PACKAGE:

- DS = 28 Lead Ceramic SOJ (Package 103)

ACCESS TIME (ns)

ORGANIZATION, 256K x 4

SRAM

MONOLITHIC

WHITE MICROELECTRONICS