PERICOM

Fast CMOS 18-Bit Registered Transceivers

Product Features:

- Supports Mixed Signal Mode Operation
  - 5 Volt Input.
  - 5 Volt Output (when connected to a 5 Volt Bus).
  - Can serve as a 5 volt to 3 volt translator.
- Advanced Low Power CMOS Operation.
- Low Standby Current (Low power CMOS, not Bi-CMOS, so output drive transistors do not require bipolar standby current levels). Typical standby power 1 mW.
- Excellent output drive capability: Balanced drives (24 mA sink and source). Compatible with LVC™ class of products.
- Pin and functional compatible: Industry standard double-density pinouts.
- Low ground bounce outputs, hysteresis on all inputs.
- ESD Protection exceeds 2000 volts.
- Packaged in 56-pin plastic TSSOP and SSOP

Product Description:

Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

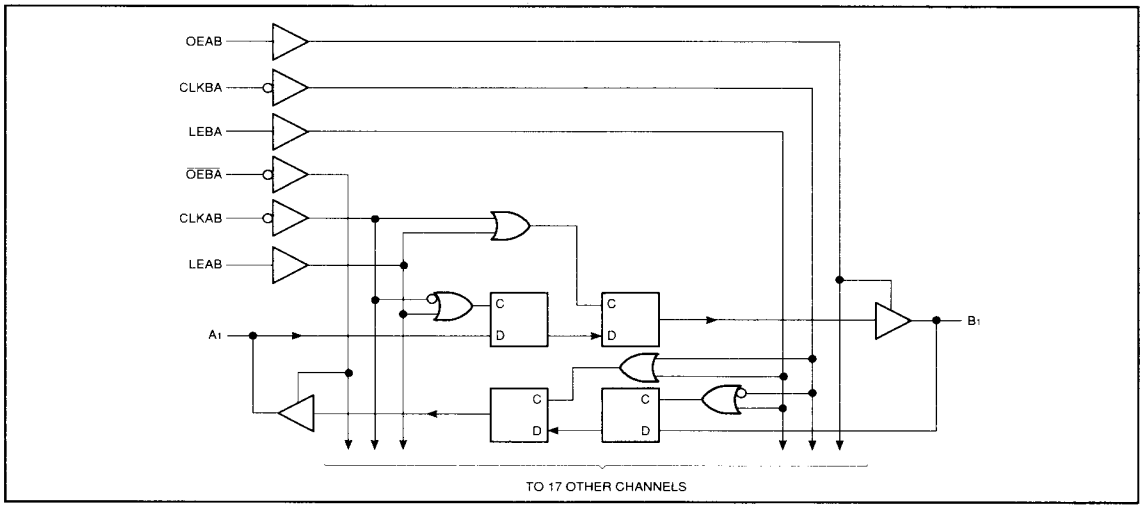
The PI74FCT163501 is 18-bit are registered bus transceivers designed with D-type latches and flip-flops to allow data flow in transparent, latched, and clocked modes. The Output Enable (OEAB and $\overline{\text{OEBA}}$, Latch Enable (LEAB and LEBA) and Clock (CLKAB and CLKBA) inputs control the data flow in each direction. When LEAB is HIGH, the device operates in transparent mode for A-to-B data flow. When LEAB is LOW, the A data is latched if CLKAB is held at a HIGH or LOW logic level. The A bus data is stored in the latch/flip-flop on the HIGH-to-LOW transition of CLKAB, if LEAB is LOW. OEAB performs the output enable function on the B port. Data flow from B port to A port is similar using $\overline{\text{OEBA}}$, LEBA and CLKBA. These high-speed, low power devices offer a flow-through organization for ease of board layout.

The PI74FCT163501 can be driven from either 3.3 V or 5.0 V devices allowing this device to be used as a translator in a mixed 3.3/5.0 V system.

All products are available in 56-pin 240 mil wide plastic TSSOP and 300 mil wide plastic SSOP packages.

5

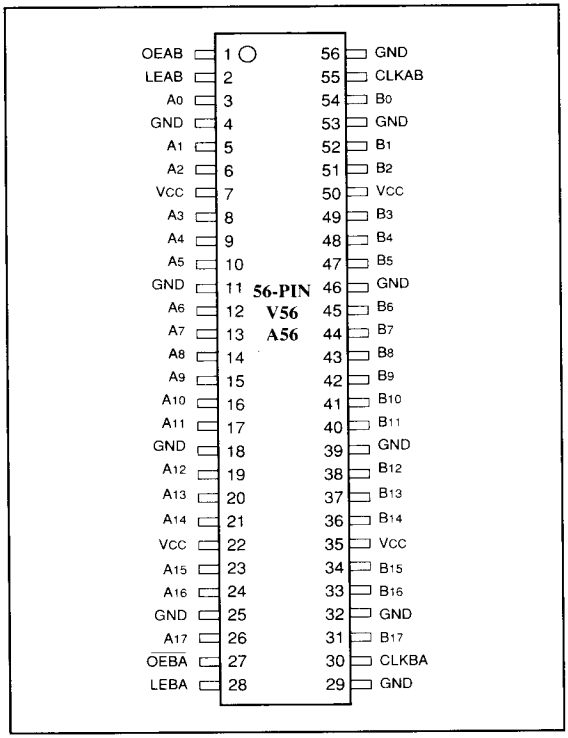
Logic Block Diagram



Product Pin Description

Pin Name	Description
OEAB	A-to-B Output Enable Input
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
CLKAB	A-to-B Clock Input
CLKBA	B-to-A Clock Input
Ax	A-to-B Data Inputs or B-to-A 3-State Outputs
Bx	B-to-A Data Inputs or A-to-B 3-State Outputs
GND	Ground
Vcc	Power

Product Pin Configuration



Truth Table[1,4]

Inputs				Outputs
OEAB	LEAB	CLKAB	Ax	Bx
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↓	L	L
H	L	↓	H	H
H	L	H	X	B[2]
H	L	L	X	B[3]

NOTES:
1. A-toB data flow is shown. B-to-A data flow is similar but uses $\overline{OEBA}$, LEBA, and CLKBA.
2. Output level before the indicated steady-state input conditions were established.
3. Output level before the indicated steady-state input conditions were established, provided that CLKAB was LOW before LEAB went LOW.
4. H = High Voltage Level
   L = Low Voltage Level
   Z = High Impedance
   ↓ = HIGH-to-LOW Transition

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–55°C to +125°C
Ambient Temperature with Power Applied	–40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	–0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	–0.5V to Vcc
DC Input Voltage	–0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	1.0W

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, T_A = –40°C to +85°C, V_{CC} = 3.3V ± 0.3V)

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
V_{IH}	Input HIGH Voltage (Input pins)	Guaranteed Logic HIGH Level		2.2		5.5	V
	Input HIGH Voltage (I/O pins)			2.0		5.5	V
V_{IL}	Input LOW Voltage (Input and I/O pins)	Guaranteed Logic LOW Level		–0.5		0.8	V
I_{IH}	Input HIGH Current (Input pins)	V_{CC} = Max.	V_{IN} = 5.5V			±5	µA
	Input HIGH Current (I/O pins)	V_{CC} = Max.	V_{IN} = V_{CC}			15	µA
I_{IL}	Input LOW Current (Input pins)	V_{CC} = Max.	V_{IN} = GND			±5	µA
	Input LOW Current (I/O pins)	V_{CC} = Max.	V_{IN} = GND			15	µA
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_{OUT} = V_{CC}			10	µA
I_{OZL}	(3-State Output pins)	V_{CC} = Max.	V_{OUT} = GND			10	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18 mA				–1.2	V
I_{ODH}	Output HIGH Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		–36		–110	mA
I_{ODL}	Output LOW Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		50		200	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –0.1mA	Vcc-0.2			V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –8mA	2.4			V
			I_{OH} = –24mA	2.0			V
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 0.1mA			0.2	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA			0.4	V
			I_{OL} = 24mA			0.5	V
I_{OS}	Short Circuit Current[4]	V_{CC} = Max.[3], V_{OUT} = GND		–60	–135	–240	mA
I_{OFF}		V_{CC} = 0V, V_{IN} or V_{OUT} = 4.5V				100	µA
V_H	Input Hysteresis				150		mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}				1.5	mA

Notes:
1. For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 3.3, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.

Power Supply Characteristics

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
ΔI_{CC}	Quiescent Power Supply Current	V_{CC} = Max.	$V_{IN} = V_{CC} - 0.6$[3]		2.0	30	µA
	TTL Inputs HIGH		V_{IN} = 2.4 V[3]		70	500	µA
I_{CCD}	Dynamic Power Supply[4]	V_{CC} = Max., Outputs Open $x\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ V_{IN} = GND		50	75	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_i = 10 MHz 50% Duty Cycle $x\overline{OE}$ = GND One Bit Toggling	$V_{IN} = V_{CC} - 0.6V$ V_{IN} = GND		0.6	2.3	mA
			V_{IN} = 2.4 V V_{IN} = GND		0.6	2.5	
		V_{CC} = Max., Outputs Open f_i = 2.5 MHz 50% Duty Cycle $x\overline{OE}$ = GND 16 Bits Toggling	$V_{IN} = V_{CC} - 0.6V$ V_{IN} = GND		2.1	4.7[5]	
			V_{IN} = 2.4 V V_{IN} = GND		2.6	8.5[5]	

Notes:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
2. Typical values are at Vcc = 3.3 V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4 V); all other inputs at Vcc or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

PI74FCT163501 Switching Characteristics over Operating Range

Parameters	Description	Conditions[1]	FCT163501T Com. Min	FCT163501T Com. Max	Unit
t_{MAX}	CLKAB or CLKBA frequency	C_L = 50 pF	—	150	MHz
t_{PLH} t_{PHL}	Propagation Delay Ax to Bx or Ax to Bx	R_L = 501 Ω	1.5	5.1	ns
t_{PLH} t_{PHL}	Propagation Delay LEBA to Ax, LEAB to Bx		1.5	5.6	ns
t_{PLH} t_{PHL}	Propagation Delay CLKBA to Ax, CLKAB to Bx		1.5	5.6	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEBA}$ to Ax, OEAB to Bx		1.5	6.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEBA}$ to Ax, OEAB to Bx		1.5	5.6	ns
t_{SU}	Setup Time HIGH or LOW Ax to CLKAB, Bx to CLKBA		3.0	—	ns
t_H	Hold Time HIGH or LOW Ax to CLKAB, Bx to CLKBA		0	—	ns
t_{SU}	Setup Time HIGH or LOW Ax to LEAB, Bx to LEBA — Clock HIGH		3.0	—	ns
	Clock LOW		1.5	—	ns
t_H	Hold Time HIGH or LOW Ax to LEAB, Bx to LEBA		1.5	—	ns
t_W	LEAB or LEBA Pulse Width HIGH[3]		3.0	—	ns
t_W	CLKAB or CLKBA Pulse Width HIGH of LOW[3]		3.0	—	ns
$t_{SK(O)}$	Output Skew[4]		—	0.5	ns

Notes:
1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.
4. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Capacitance (T_A = 25°C, f = 1 MHz)

Parameters[1]	Description	Test Conditions	Typ	Max.	Units
C_{IN}	Input Capacitance	V_{IN} = 0 V	4.5	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	5.5	8	pF

Note:
1. This parameter is determined by device characterization but is not production tested.